A Half-Shared Transimpedance Amplifier Architecture for High-throughput CMOS Bioelectronics

Geoffrey Mulberry
Department of Electrical and Computer Engineering
University of Central Florida
Orlando Fl, United States of America
gmulberry@knights.ucf.edu

Kevin A. White
Department of Electrical and Computer Engineering
University of Central Florida
Orlando Fl, United States of America
kwhite64@knights.ucf.edu

Brian N. Kim
Department of Electrical and Computer Engineering
University of Central Florida
Orlando Fl, United States of America
brian.kim@ucf.edu

Abstract— **A common problem in single-cell measurement is the low-throughput nature of measurements. Monolithic CMOS microsystems have enabled many parallel measurements to take place simultaneously to increase throughput due to the integration of electrodes and amplifiers into a single chip. This paper explores a CMOS chip containing an array of 1024 parallel transimpedance amplifiers that takes advantage of a "half-shared" operational amplifier architecture. This architecture splits a traditional 5-transistor operational amplifier into two, the inverting half and the non-inverting half. Splitting an amplifier into two allows for the non-inverting half to be "shared" with several inverting halves, reducing the die area required for each individual amplifier. This allows for an increased number of amplifiers to be embedded into the same chip; in this case, 32 amplifiers are able to fit in the same space as 17 traditional 5-transistor operational amplifiers. The amplifiers exhibit low mismatch of 1.65 mV across the entire 1024 amplifier array, as well as high linearity in transimpedance gain. The technique will enable larger arrays to be created in future designs to allow electrophysiologists, among others, access to even higher-throughput measurement tools.**

Index Terms— **amperometric sensors, biosensors, CMOS analog integrated circuits, electrophysiology, operational amplifiers**

I. Introduction

A transimpedance amplifier (TIA) is commonly used in bioelectronics to measure currents in biological applications as well as at the single-cell level [1]–[3]. They traditionally consist of an operational amplifier (OPA) using resistive feedback to hold an electrode at a reference voltage and transform the current into the electrode into a voltage measurement. For high-throughput measurements from many cells simultaneously, a larger number of parallel electrodes and amplifiers is required. Thus, it is advantageous to minimize the size requirements of the TIAs if increased throughput is desired. One approach for minimization of TIAs is the "half-shared" structure of OPA, which is explored in this paper.

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Numerous devices have been designed using similar half-shared structures, ranging from tens to thousands of amplifiers [4]–[6]. The design principle of a half-shared OPA is to allow for the inverting half to be shared between multiple OPAs, reducing the required die area for multiple OPAs by a factor of two. In an effort to have a high bandwidth, a folded-cascode architecture was used for the early half-shared amplifiers [1]. The folded-cascode architecture achieves wide dynamic range and bandwidth at the cost of high power and area consumption. However, if used for most electrophysiology applications, the required bandwidth is small (< 20 kHz). Many CMOS detector arrays operate well below 20 kHz, usually in the 10 kHz region [4], [7]. This low bandwidth is easily obtained with a traditional five transistor (5T) OPA, further eliminating any benefits to the folded-cascode architecture. Thus, the 5T OPA design is adapted in this paper to minimize the power and area consumption.

For this work, a CMOS chip [8] was fabricated on a common 0.35 μm 4M2P process and used to study the effects of the 5T half-shared OPA structure. The design of the TIAs, OPAs, and array will be discussed in detail. Briefly, the array consists of a 32 × 32 grid of array elements for a total of 1024. Each array element consists of a TIA based on the half-shared OPA design that is reconfigurable for several modes of operation and test cases. Other than the half-shared OPA architecture, each TIA is completely independent from the others, enabling 1024 simultaneous parallel single-cell measurements.

II. TIA and Array Design

This section explores the design of the individual array elements as well as the half-shared OPA architecture and the array's structure.

A. Array elements

Fig. 1 shows the schematic for one of the 1024 half-shared TIA array elements, which is based on an integrating capacitor rather than resistive feedback to further save space. Each consists of 11 MOSFETs, a half-shared OPA, an SRAM and two capacitors. M_1 forms half of a current mirror used to set a

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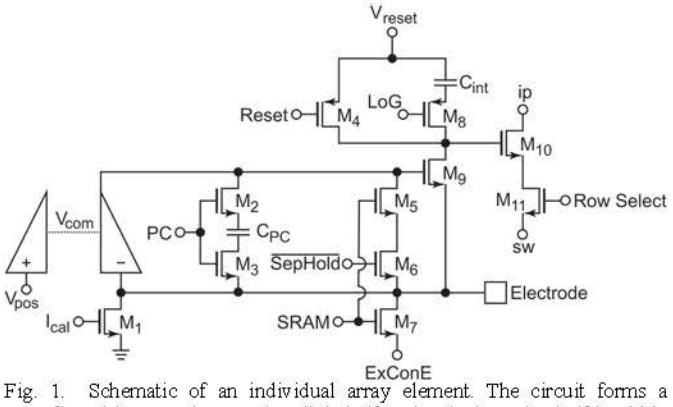

Fig. 1. Schematic of an individual array element. The circuit forms a reconfigurable TIA. The OPA is split in half so that the inverting half is within each array element while the non-inverting half is separated so it can be shared with other amplifiers.

baseline current through the TIA via I_{cal}. Optional phase compensation is enabled when PC is high by turning on switches, M_2 and M_3, which inserts C_{PC} into the feedback loop. M_4 is used as a switch to reset the integration capacitance. The integration capacitance is formed by either parasitic capacitance in high-gain mode, or by C_{int} in low-gain mode by setting LoG (**Lo**w-**G**ain) low, which turns on switch M_8. Switch M_7 allows for the connection to an external electrode, ExConE, when the SRAM is set high. The SRAM serves a dual purpose by allowing the OPA to be in the unity-gain configuration when $\overline{\text{SepHold}}$ is high and the SRAM is high. This turns on both M_5 and M_6, shorting the inverting input of the OPA to the output. M_9 provides a feedback path for the OPA, while allowing current to travel through to the integration capacitance. When the Row Select is high, switch M_{11} is turned on, and an OPA is formed in the output buffers, using M_{10} as one of its differential input transistors. All transistors acting as switches are the minimum dimension. M_9 and M_{10} are square for the best matching characteristics.

B. Half-shared OPA structure

The key feature of the compact size of this array is the half-shared architecture implemented within the OPAs. In a traditional 5T OPA used in the negative feedback configuration, redundancies occur for parallel amplifiers when voltage on the non-inverting inputs are the same. To aid with the explanation of this concept, the schematic of a four-way half-shared OPA is shown in Fig. 2. Here, M_1-M_5 form a traditional 5T OPA, where M_3 provides a bias current for the differential pair, M_2 and M_5, and M_1 and M_4 form a current mirror for the differential pair. The gate of M_2 is the non-inverting input while the gate of M_5 is the inverting input. The output is taken at the drains of M_4 and M_5.

If a second 5T OPA is desired, the addition of 5 transistors would be required. This is true except in the case where V_{pos} and the bias current are the same for the two OPAs. In this case, the addition of only 2 transistors is required due to the fact that V_{mir} and V_{com} can be shared between the two OPAs. In this example, the two transistors required are M_6 and M_7. M_6 acts as the current mirror for M_7, whose gate is the second inverting input. This concept can be extended to any amount of additional OPAs. In this case, four are used with the addition of $M_{8\text{-}9}$ and

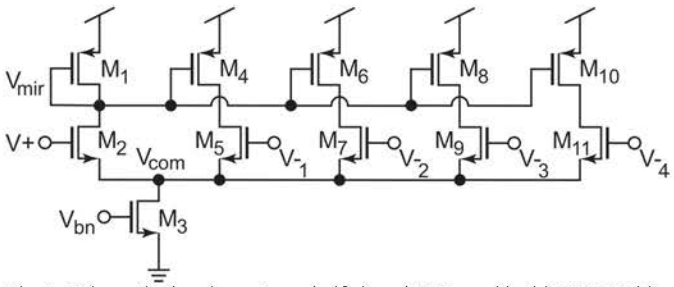

Fig. 2. Schematic showing a 4-way half-shared OPA used in this CMOS chip. Transistors M_1-M_5 form a traditional 5T OPA, transistors M_6-M_7, M_8-M_9, and M_{10}-M_{11} form inverting halves of additional OPAs.

$M_{10\text{-}11}$. An important design requirement is that, for this architecture to work properly, transistors M_1, M_4, M_6, M_8, and M_{10} must all be matched sizes, as well as transistors M_2, M_5, M_7, M_9, and M_{11}. More than four OPA halves can be shared at the expense of decreased dynamic range caused by the additional current required to flow through biasing transistor M_3. Increased drain current will increase the drain to source potential of the transistor. Thus for the input transistors to have sufficiently high gate to source potential, the lower bound on the input dynamic range must also increase with each additional OPA half. In this study, four halves are shared as a compromise between die area and dynamic range.

For this array design, each array element was set to be 30 × 30 μm. Each transistor for the OPAs is sized at 10 × 10 μm. Thus, the gates of the transistors alone for a single OPA require 500 μm^2 or 55.8% of the 900 μm^2 available for each array element. This would leave insufficient area for the remaining circuitry shown in Fig. 1. Without the half-shared architecture, the circuitry would not be able to fit in the desired space, reducing the number of parallel amplifiers embedded into the CMOS chip. However, with the half-shared structure, only 2 OPA transistors must fit into each array element, requiring 200 μm^2 or 22.2% of the array element area, allowing for the addition of the extra circuitry.

C. Array design using half-shared structure

The CMOS chip used during this study uses the half-shared structure to its advantage by densely packing 1024 fully-independent TIAs into a single chip. The arrangement of these

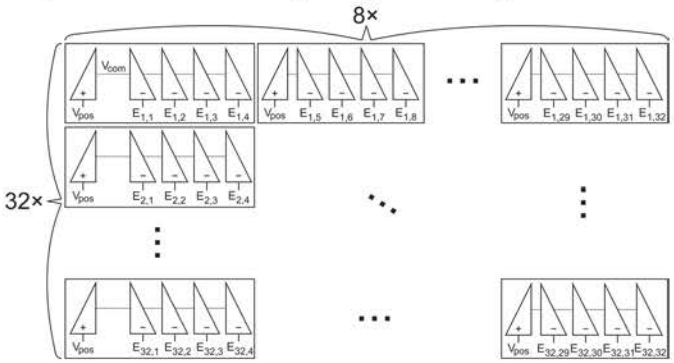

Fig. 3. Block diagram of the chip containing 1024 half-shared TIA array element. Each block is a group of four amplifiers adopting the half-shared architecture as shown in Fig. 2 to save die area while increasing the number of on-chip amplifiers. The array is eight blocks of four amplifiers wide and 32 rows tall for a total of 1024 electrodes and amplifiers. Each electrode is labeled with its *x*- and *y*- coordinate position as their indices.

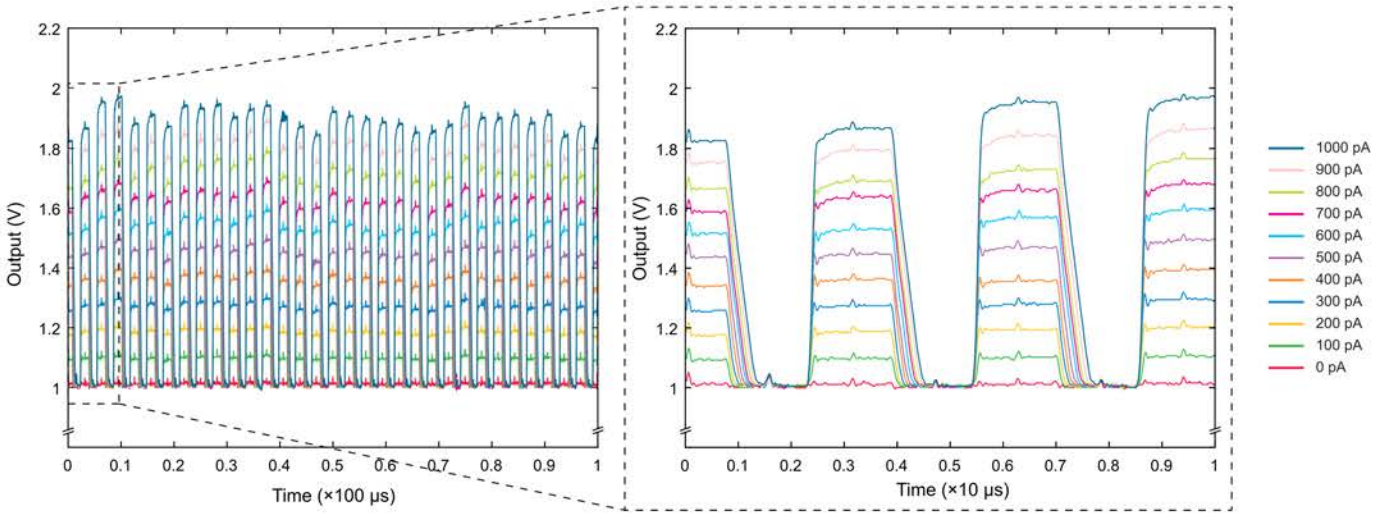

Fig. 4. Left: Output waveforms for a single column measurement showing the 32 outputs for various I_{cal} input currents. Right: Magnified view of the first 4 outputs from the same recording.

TIAs is shown in Fig. 3. The 1024 amplifiers are arranged into a 32 × 32 grid. Along the rows, every four amplifiers are part of a group utilizing the half-shared architecture for a total of eight half-shared blocks per row. This arrangement of half-shared blocks manages to fit 32 TIAs in the same space that could fit only 17 traditional TIAs using 5T OPAs. This arrangement provides an effective way to increase throughput of parallel cellular measurements. Even though there are eight positive halves of OPA in each row, all of the V_{pos} terminals are connected together. This allows for a global V_{pos} terminal to set the voltage present at all electrodes for performing current measurements in an electrolytic solution, such as single-cell electrophysiology and amperometry experiments. Entire rows of 32 TIAs are read out row after row. While one row is being read, the other 31 are performing integration of their electrode currents, enabling 1024 simultaneous measurements.

III. Results

Several experiments have been performed using the described CMOS chip to determine the effectiveness of the half-shared architecture. Some of the measurements shown here are a representative column output, linearity in current-to-voltage conversion, mismatch of the individual amplifiers, bandwidth, and gain.

A. *Transimpedance Measurement*

To study the half-shared TIA's current-to-voltage conversion performance, the amplifiers were set to low gain mode and the outputs were recorded from a single column at several values using the external I_{cal} input ranging from 0 to 1000 pA. The results from this transimpedance measurement are displayed in Fig. 4. Each trace represents the voltage recording from a single column. The square pulses are the result of the correlated double sampling (CDS) output stage where each row is measured at both the reset and the output value to remove the offset of the amplifier circuits. The plot on the left shows the output voltage of a single column measurement (the 32 TIAs in that column) for each of the various I_{cal} input currents. The inset plot on the left is a magnification of the same recording to more clearly show the well-defined and linearly-spaced output voltages for the first four TIAs in the column.

B. *Linearity*

To extract the TIA's linearity performance, data was taken from the transimpedance recording used in Fig. 4 and used to create the voltage versus current plot shown in Fig 5. The results from each of the 32 TIAs' outputs were used to create a linear fit of V_{out} against I_{cal}. The resulting fit has an R^2 value of 0.994, indicating a high-quality linear performance of the TIAs.

C. *Mismatch*

The mismatch between the transistor's sizes in the OPA can cause a voltage mismatch between the inverting and non-inverting inputs when there is a negative feedback. To test this,

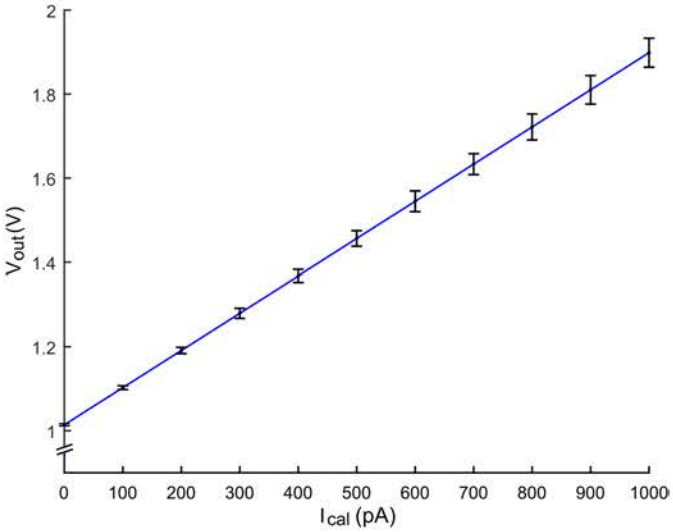

Fig. 5. Linearity of the TIAs. The R^2 value of the linear fit is 0.994, indicating a high-quality linear performance. The error bars indicate the standard deviation of the output voltage of all 32 TIAs in the recording.

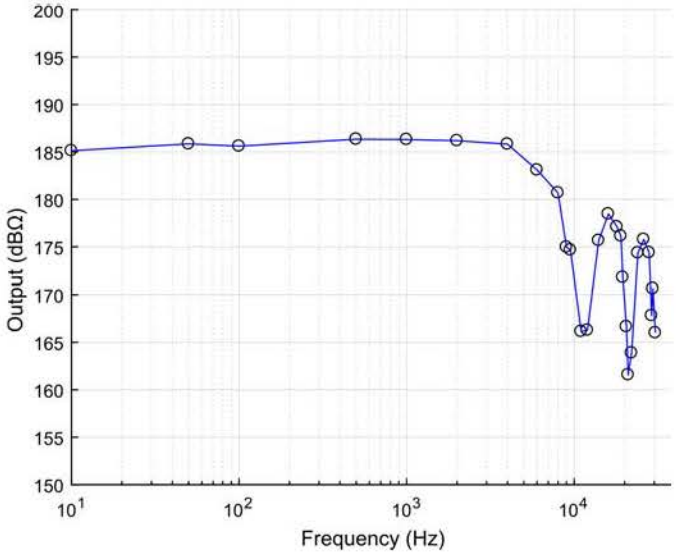

Fig. 6. Frequency response of the TIA showing $sinc^2()$ response caused by the integration performed at 10 kHz. The measurement used a 55.2-nA bias current.

the array elements are designed to enable a unity gain mode and have external electrode connections so that a simple mismatch measurement could be performed. In unity gain mode, the OPA's output is tied directly to the inverting input, the non-inverting input is held at a reference voltage, V_{pos}, and the output voltage is measured at the ExConE. If the OPAs operate in an ideal fashion with no mismatch, every OPA should produce exactly V_{pos} at their outputs. To perform this experiment in a well-controlled fashion, a LabVIEW program is made to control a National Instruments data acquisition system. This automates the programming of SRAMs and measurement of each array element's output one at a time in the shortest possible time. Timing is important for this measurement so that the effect of environmental variables such as temperature do not deviate throughout the course of the measurement. The mismatch measurement results in a mean output voltage of 1.005 V and a mismatch of 1.65 mV.

D. Bandwidth and Gain

The bandwidth of the half-shared TIA is measured using a ~55 nA bias current for each TIA. Phase compensation is also enabled. V_{pos} is set to 1 V. A TIA was set to connect to ExConE and the ExConE terminal was connected through a 1 MΩ resistor to a National Instruments data acquisition unit, allowing for the generation of both a DC electrode current as well as an AC sinusoid to be applied to the amplifier. Various frequencies were input and the outputs were measured and converted to transimpedance gain as shown in Fig. 6. When clocked at 10 kHz, the TIA produces the expected ~4.4 kHz bandwidth with a passband gain of ~185 dBΩ, as well as the expected $sinc^2()$ aliasing sidelobes caused by the integration period.

IV. Conclusion

The presented method for reducing die area required for OPAs in TIAs by half-sharing is an effective technique. The half-shared amplifier's characteristics, including transimpedance gain, matching, as well as linearity, are tested in this paper. A four half-shared OPA scheme has proven to enable the miniaturization of 32 TIAs into the same space that would traditionally only be able to fit 17 of the same type. This enables future chips to be designed with an even higher number of electrodes and amplifiers for high-throughput cellular measurements. For future work, this chip will be further tested for other characteristics such as gain calibration, crosstalk, and noise.

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