Experimental Demonstration of Ferroelectric Spiking Neurons for Unsupervised Clustering

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Abstract—We report the first experimental demonstration of ferroelectric field-effect transistor (FEFET) based spiking neurons. A unique feature of the ferroelectric (FE) neuron demonstrated herein is the availability of both excitatory and inhibitory input connections in the compact 1T-1FEFET structure, which is also reported for the first time for any neuron implementations. Such dual neuron functionality is a key requirement for bio-mimetic neural networks and represents a breakthrough for implementation of the third generation spiking neural networks (SNNs)—also reported herein for unsupervised learning and clustering on real world data for the first time. The key to our demonstration is the careful design of two important device level features: (1) abrupt hysteretic transitions of the FEFET with no stable states therein, and (2) the dynamic tunability of the FEFET hysteresis by bias conditions which allows for the inhibition functionality. Experimentally calibrated, multi-domain Preisach based FEFET models were used to accurately simulate the FE neurons and project their performance at scaled nodes. We also implement an SNN for unsupervised clustering and benchmark the network performance across analog CMOS and emerging technologies and observe (1) unification of excitatory and inhibitory neural connections, (2) STDP based learning, (3) lowest reported power (3.6nW) during classification, and (4) a classification accuracy of 93%.

I. Introduction

In spite of staggering successes of deep neural networks (DNNs), the second generation of neural networks (NNs), we have come to the realization that true advances in cognitive systems will require autonomous agents to learn from the environment without the need for labelled data. Unsupervised learning provides such a paradigm. In particular, unsupervised learning and clustering in spiking neural networks (SNNs)–which represent the third generation of NNs–emulate neural properties via their coupled dynamics. Recent advances in neurosciences as well as estimation theory have revealed the advantages of data-encoding through spike-timing: compactness, sparsity, and the ability to learn via local updates only (STDP), all of which have led to efficient hardware implementations of *at-scale* SNNs [1,2].

In parallel, emerging nanodevices such as resistive RAMs, memristors, spin and metal-insulator transition devices offer significant benefits in terms of power, performance and area as physical hardware platforms for implementing NNs—thanks to their unique properties that are not intrinsic to the CMOS technology. A template leaky-integrate-and-fire (LIF) neuron implemented with any of these technologies provides promising opportunities, but they all suffer from a fundamental shortcoming. All these neurons are excitatory, which means that inputs coming to these neurons result in a spike generation. However, it is well known in neurobiology and also in biomimetic neuromorphic architectures that excitatory neurons need to be paired with inhibitory connections to enable homeostasis, high accuracy in unsupervised learning and increased sparsity in spiking–all of which are essential to implement functionally correct and efficient compute models.

In this paper, we introduce ferroelectric field-effect transistor (FEFET) as the underlying device technology for implementing SNNs, and demonstrate, for the first time, ferroelectric spiking neurons—the functional unit of SNNs—with built-in excitatory (exc.) and inhibitory (inh.) input connections, which (1) inherently demonstrate bio-mimetic dynamics, and (2) leads to compact and efficient implementation of neurons and hence the synaptic weights.

II. Experimental Demonstration of Ferroelectric Neuron

The core structure of the FE neuron consists of a ferroelectric FET (FEFET) and a MOSFET (the discharge FET) (fig. 1(a)). An important feature of our demonstration is that, FEFET being a three terminal neuromorphic device with an intrinsic transistor gain, allows for handling both excitatory and inhibitory input connections in this simple, area efficient two transistor neuron structure. The excitatory and the inhibitory inputs (V_x and V_i, respectively) are connected to the gate terminals of the discharge FET (V_{GM}) and FEFET (V_{GF}), respectively, through respective leaky integrators (fig. 2(a)). The output of neuron V_N is at the voltage across the capacitor C which is digitized by an inverter at V_O. The FEFET was consists of a L_G=80 nm n-FinFET with 14 fins with its gate terminal connected to an epitaxial 100 nm thick $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) ferroelectric. The key to our demonstration of spike generation and inhibition in FE neuron is twofold: (1) the existence of abrupt transitions in the hysteresis edges of the current-voltage characteristics of our FEFET much below the thermal limit with

no stable states therein, and (2) the dynamic tunability of the location and the width of the FEFET hysteresis by bias conditions which allows for inhibition—both of which are achieved by careful design of the experiments (Fig. 2(a)).

To explain the operating principle, we refer to the load-line analysis shown in fig. 3(b). Fig. 3(b) plots the measured d.c. drain current of the FEFET I_{DF} as a function of its source voltage (V_N) while keeping the gate and drain voltages (V_{GF} and V_D) fixed. Also plotted in fig. 3(b) are the output characteristics of the discharge FET (I_{DM}-V_N curves at different V_{GM}).

Resting state: When at rest (no exc. V_x and inh. V_i input spikes, V_{GM} and V_{GF} are constant), the operating point of the system is the intersection of the I_{DF}-V_N (FEFET) and I_{DM}-V_N (discharge FET) curves which is point F in fig. 3(b).

Neuron firing: Upon the arrival of an exc. spike train at V_x, V_{GM} reaches the threshold (V_{GM}=1.15 V for V_{GF}=1 V as in fig. 3(b)) for firing when the corresponding I_{DM}-V_N curve intersects the abrupt transition regions of the I_{DF}-V_N curve of the FEFET. Note that there are no stable states in these transition regions, and hence, the system oscillates through the loop ABCD in fig. 3(b) [3]. Fig. 4(a) shows the measured waveform of the neuron output voltage V_N in response to an exc. input spike train V_x. of period T= 28 ms and no inh. input spikes (thereby, V_{GF}=1 V). Output spikes have a period of 27.9 ms. During this input spike train, V_{GM} varies between 1.225 V and 1.425 V (corresponding load-lines drawn in fig. 3(b)). In the zoomed-in version of the output spikes in fig. 4(a), note that the capacitor C is discharged during the transition A→B through the discharge FET, and during C→D, the FEFET charges the capacitor C. Fig. 4(b) shows the evolution of the V_N waveform as the exc. input spike period T is changed from 26 ms to 300 ms. The decrease of the period decreases the output firing rate and at T=300 ms, no firing is observed.

Neuron Inhibition: Fig. 5(a) shows the measured neuron output voltage waveform V_N and the digital output voltage V_O in response to an exc. input V_x spike train of period T=32 ms starting at t=0 and an inh. input V_i spike train of duration 0.18 s starting at t=1.025 s. When both exc. and inh. inputs spikes are present, the output spikes are inhibited and the average voltage level of V_N moves to a higher value. The digitized outputs are also shown in fig. 4(a). The key to neuron inhibition is the fact that the hysteresis in the I_{DF}-V_N curve (FEFET) becomes narrower and shifts to the right when V_{GF} increases (fig. 3(b)). This effect arises due to that the location and the width of the hysteresis in I_D-V_{GS} curve of the FEFET depends on the value of V_D (fig. 2(a)). Moreover, the hysteretic transition is actually not abrupt enough when V_{GF}=1.6V to travel around the hysteresis. The inh. input V_i spikes raise V_{GF} from 1 V to 1.6 V; the corresponding the I_{DF}-V_N curve with V_{GF}=1.6 V is shown in fig. 3(b). The I_{DM}-V_N curves corresponding to V_{GM} swing (1.225 V to 1.425 V) intersects to the I_{DF}-V_N curve at V_{GF}=1.6 V at point S and P where hysteretic transition is not steep enough. As such, in this case, the neuron does not fire, and V_N moves back and forth between S and P. Fig. 5(b) shows that a relatively large, single exc. input V_x pulse can generate a series of chirped output spike train which is inhibited when an inh. input V_i pulse arrives (fig. 5(c)).

III. SPICE Simulation & Performance Projection

A SPICE model for the FEFET was developed using multi-domain Preisach model [4] (fig. 6(a)) and calibrated with experimental results by considering the device geometry, measured FE hysteresis loop, and parasitic capacitances (fig. 6(b)). An accurate and quantitative agreement between the simulated and experimentally measured FE neuron waveforms and the rate coding is observed in fig. 6(d) and 6(e), respectively. The performance of a scaled FE neuron was projected at the 45 nm node using the PTM 45nm model (PSD shown in fig. 6(f)). The scaled 45 nm node FE neuron dissipates 0.36 nJ/cycle which is an improvement of 390x compared to the experimental one (0.13 μJ per cycle). The SPICE FE Neuron model was also used to simulate a specific topology of neuromorphic networks (Fig. 6(g) and 6(f)) which is used to implement and benchmark the spiking neural network (SNN) described in section IV.

IV. SNN Implementation and Benchmarking

The experimentally calibrated SPICE models have been used to evaluate network performance for unsupervised learning. We emulate the dynamics of a fully connected network (Fig. 7a) with 784 input neurons, 400 excitatory and 400 inhibitory neurons. We apply images from the MNIST data-set and use STDP to learn synaptic weights over. Fig. 7(b) illustrates how the network performs unsupervised clustering over the data-set over training examples and clusters become stronger as training progresses. This is also reflected in Fig. 7(c) and (d) where the square of the change of weights decreases and the classification and clustering accuracy increases. We benchmark the network performance across analog CMOS and emerging technologies and observe (1) unification of excitatory and inhibitory neural connections, (2) STDP based learning, (3) lowest reported power (3.6nW) during classification, and (4) a classification accuracy of 93%.

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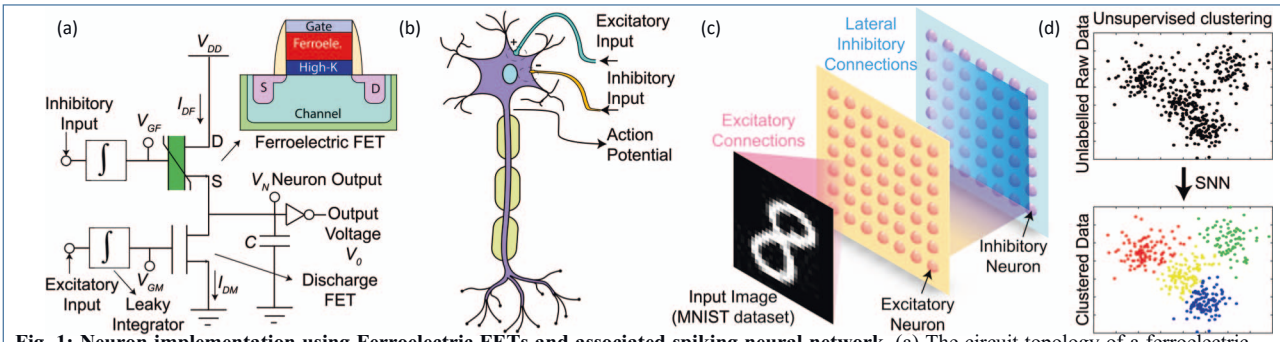


Fig. 1: Neuron implementation using Ferroelectric FETs and associated spiking neural network. (a) The circuit topology of a ferroelectric spiking neuron with excitatory and inhibitory inputs. (b) A biological neuron. (c) A schematic representation of spiking neural network (SNN) with an excitatory and an inhibitory neuron layer. (d) The concept of unsupervised clustering on unlabeled, raw data using an SNN .

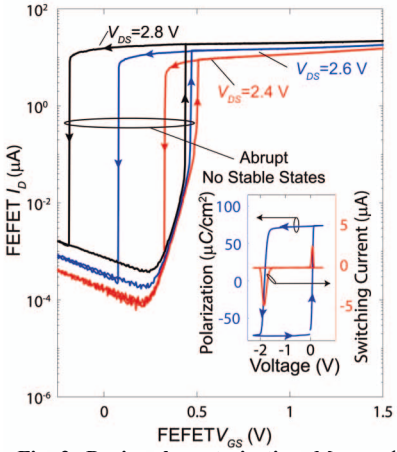


Fig. 2: Device characterization. Measured d.c. I_D-V_{GS} characteristics of the FEFET. Polarization-voltage and switching current-voltage characteristics of epitaxial PZT ferroelectric in the FEFET structure at 150 Hz (inset). The transitions for V_{DS}=2.6V and 2.8V are abrupt. However, for V_{DS}=2.4V, only the downward transition is abrupt.

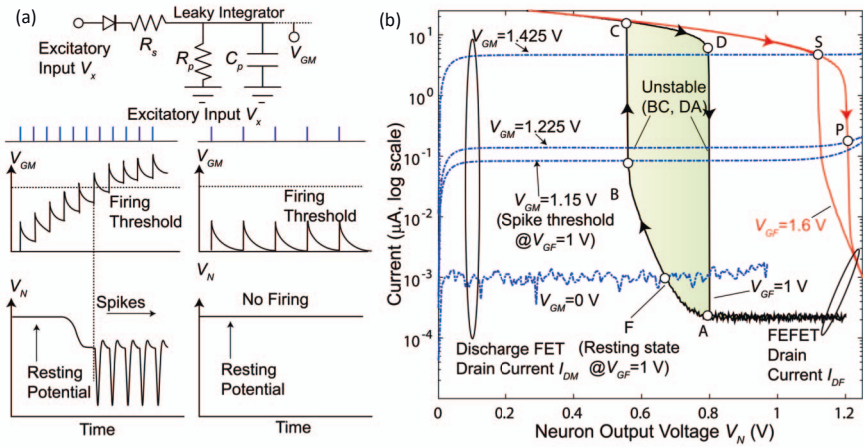


Fig. 3: Operating principle and Load line analysis of the experimental ferroelectric neuron (a) Operating principle of the ferroelectric neuron and circuit diagram of the leaky integrator. (b) Load-line analysis. Measured d.c. I_D-V_N characteristics of FEFET at V_{GF}=1 V and 1.6 V and V_D=V_{DD}=3.3 V and output characteristic (I_M-V_S) of the discharge FET. At V_{GF}=1.6 V, the hysteresis in I_D-V_S characteristics shifts to the right compared to that at V_{GF}=1 V. The neuron generates spikes when the discharge FET load lines intersect the FEFET I_D-V_S curves in the unstable transition regions (i.e., BC and DA @V_{GF}=1 V). For V_{GF}=1.6V, the hysteretic transition is not abrupt enough to travel around the hysteresis (*i.e.*, move back and forth between S and P).

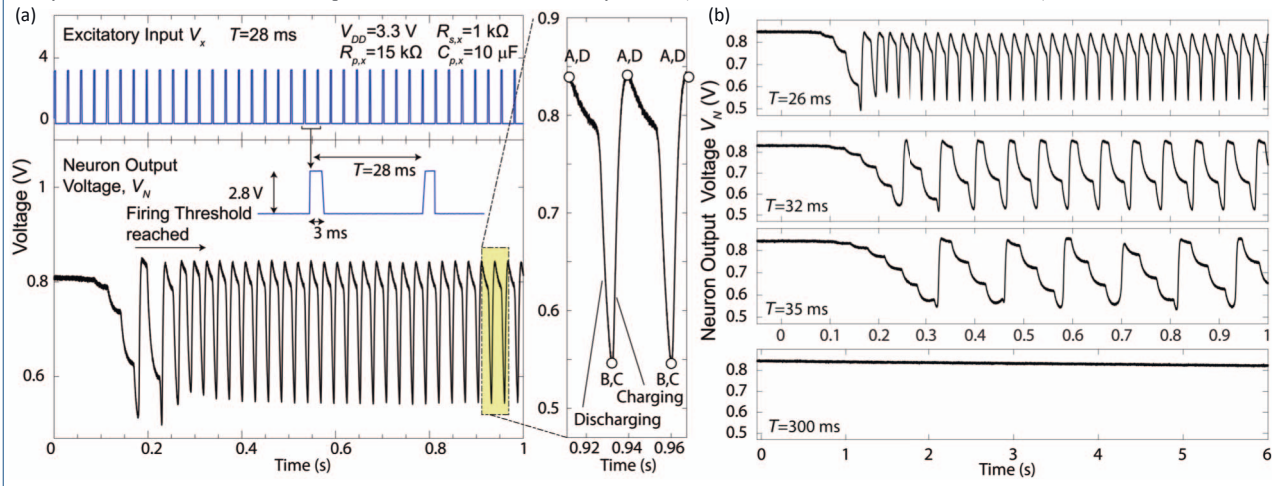


Fig. 4: Experimental demonstration of a ferroelectric neuron. (a) Measured waveforms of the excitatory input V_x and the neuron output voltage V_N in response to excitatory input V_x spike train with period T=28 ms and no inhibitory input spikes at V_i. The output spikes have a reverse polarity compared to the usual polarity of biological neurons. The output spike period is 27.9 ms. Also shown in a zoomed in version of two spikes. During a spike, the state of the FEFET approximately traverses the path ABCD as shown in the load line analysis shown in fig. 3(b). (b) The neuron output voltage V_N in response to excitatory input spike trains with periods T=26, 32, 35, and 300 ms and no inhibitory input spikes. The output spike period is 24.8, 63.8, 114.1 ms for T=26, 32, 35 ms, respectively. The neuron do not output any spikes for T>100 ms.

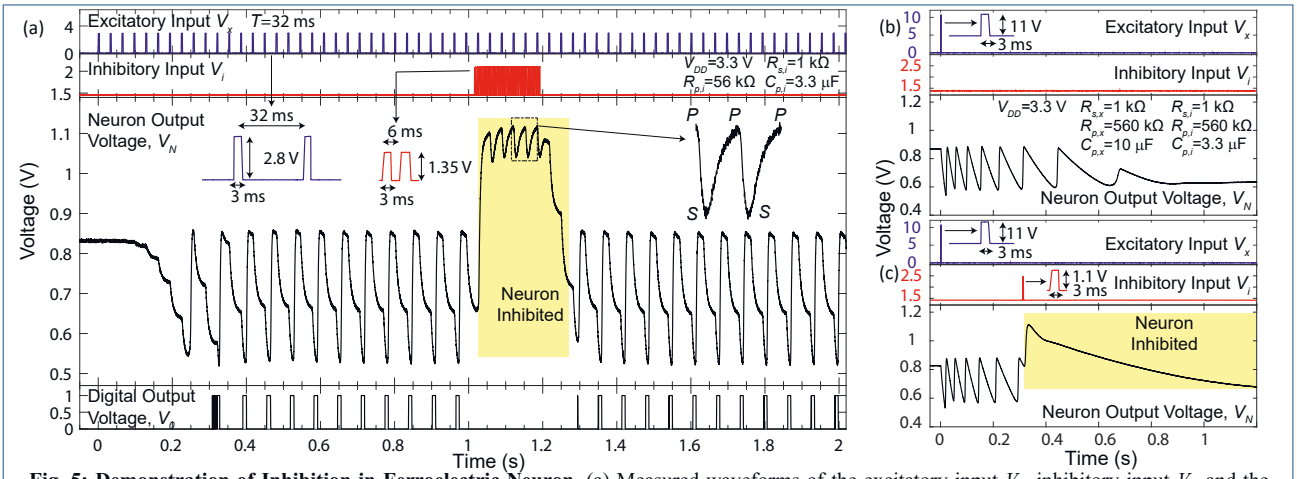


Fig. 5: Demonstration of Inhibition in Ferroelectric Neuron. (a) Measured waveforms of the excitatory input V_x, inhibitory input V_i, and the neuron output voltage V_N in response to excitatory input spike train with period T=32 ms and inhibitory input spike train of 0.18 s duration starting at t=1.025 s. When both inhibitory and excitatory input is present, the neuron do not fire and do not generate any spikes. The crests and troughs of the inhibited neuron output correspond to point S and P in the load-line analysis shown in Fig. 2(b). (b,c) A large spike in the excitatory input V_x generates a chirped output spike train (fig. c) which is be inhibited when an inhibitory pulse at V_i is arrives during this spiking mode (fig. c).

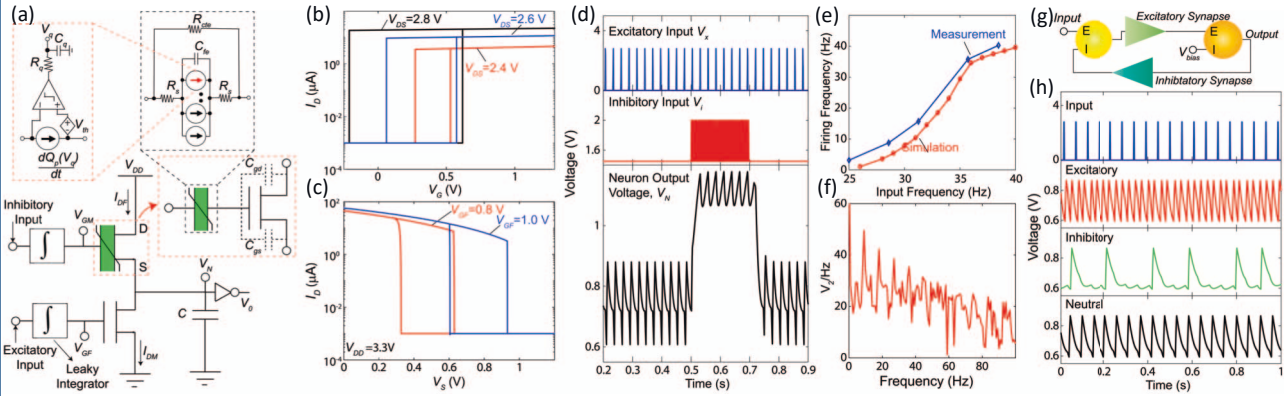
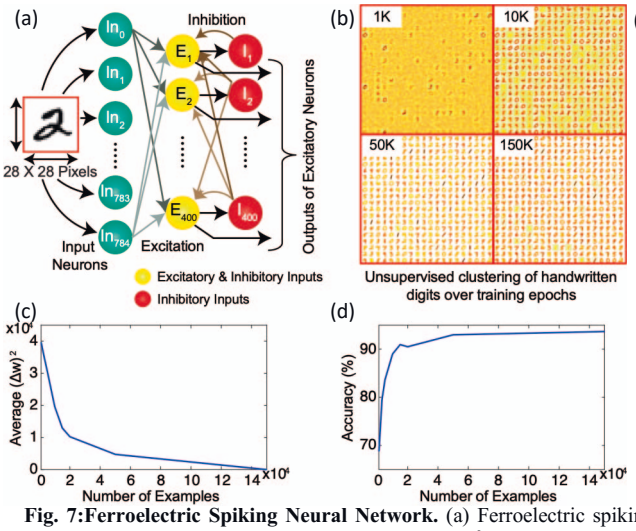


Fig. 6: SPICE Simulation of Ferroelectric Neuron. (a) SPICE model of the FE neuron. (b, c, d) Simulated the I_D-V_G (b) and I_D-V_S (c) characteristics for the FEFET and the neuron waveforms (c) under similar experimental conditions presented in Fig. 5(a) showing reasonable agreement between experiment and simulation. (e) Input Frequency versus firing frequency of the neuron. (f) Simulated power spectrum density of a FE neuron projected at 45 nm node. (g,h) The neuromorphic topology of interconnected neurons (g) used in SNN simulation in Fig. 7 and its SPICE simulated behavior (h) when either of the excitatory (red) and inhibitory (green) connections are active or both of them are neutral (black).



(e)

	[5]	[6]	[7]	Current work
Technology	CMOS Analog, Mixed Signal		Emerging Technology	
Neuron Type	LIF	Multiply-Accumulate	LIF	LIF
Network Type	Spiking	Non-spiking	Spiking	Spiking
Data Encoding Architecture	Spike Timing	Multi-level perceptron	Spiking Rate	Spike Timing
Input Type	Excitatory	Excitatory	Excitatory	Excitatory & Inhibitory
Device Count	15 T	64 T	1T - 1 VO_2	1T - 1 FEFET
Synapse Requirements	Positive and Negative Weights	Positive and Negative Weights	Positive and Negative Weights	Positive Weights
Training & Classification	Unsupervised	Reinforcement	Supervised	Unsupervised
Power	10 nW	125 nW	Not reported	3.6 nW

Fig. 7:Ferroelectric Spiking Neural Network. (a) Ferroelectric spiking neural network architecture. (b) Illustration of MINST over training epochs of 1k, 10k, 50k, and 150k. (c,d) Average $(\Delta w)^2$ (c) and %accuracy (d) versus number of examples. (e) Benchmark table.