Scalable Forming and Flash Light Sintering of Polymer-Supported Interconnects for Surface-Conformal Electronics

Harish Devaraj
Department of Mechanical and Aerospace Engineering,
Rutgers University,
98 Brett Road,
Piscataway, NJ 08854
e-mail: harish.devaraj@rutgers.edu

Rajiv Malhotra[1]
Department of Mechanical and Aerospace Engineering,
Rutgers University,
98 Brett Road,
Piscataway, NJ 08854
e-mail: rajiv.malhotra@rutgers.edu

Conformally integrating conductive circuits with rigid 3D surfaces is a key need for smart materials and structures. This paper investigates sequential thermoforming and flash light sintering (FLS) of conductive silver (Ag) nanowire (NW) interconnects printed on planar polymer sheets. The resulting interconnect–polymer assemblies are thus preshaped to the desired 3D geometry and can be robustly attached to the surface. This conformal circuit integration approach avoids interconnect delamination in manual conformation of planar flexible electronics, eliminates heating of the 3D object in direct conformal printing, and enables easy circuit replacement. The interconnect resistance increases after thermoforming, but critically, is reduced significantly by subsequent FLS. The resistance depends nonlinearly on the forming strain, interconnect thickness, and FLS fluence. The underlying physics behind these observations are uncovered by understanding interconnect morphology and temperature evolution during the process. With the optimal parameters found here, this process achieves interconnect resistance of <10 Ω/cm within 90.8 s at 100% maximum strain over a 1 square inch forming area. The application of this process for complex surfaces is demonstrated via a simple conformal LED-lighting circuit. The potential of this approach to enable surface size and material insensitivity, robust integration, and easy replaceability for conformal circuit fabrication is discussed. [DOI: 10.1115/1.4042610]

Introduction

Integration of electronics with rigid 3D surfaces has been used to combine antennas, displays, sensors, and other functional devices with 3D objects for creating smart structures [1–4]. A critical enabler for this technology is the integration of electrically conductive interconnects on 3D surfaces [2,4–7], which can be combined with pick-and-place methods for integrating other active devices. Currently, such integration is performed either by mechanical conformation of printed circuits on flexible polymers with the surface or by conformal 3D printing of nanomaterial-based circuit patterns directly on the surface. The mechanical conformation approach can cause interconnect delamination and cracking, leading to significant loss in conductivity [8]. Past studies have attempted to alleviate this issue by tailoring the microscale shape of the interconnects [3,9] or by interfacial modifications of the printed nanomaterials [10–12]. However, these approaches are more suitable for smooth convex surface features. For example, conformation of a planar polymer-circuit assembly with a concave cavity or corner requires significant mechanical handling of the assembly, which can damage the circuits.

In contrast, conformal 3D printing of nanoparticle pastes can fabricate such conformal circuits without mechanical conformation, while retaining high geometric versatility and eliminating the need for expensive vacuum deposition [4]. This approach has seen considerable interest, including the commercial development of the conformal aerosol-jet printing (AJP) method [13]. However, this process still suffers from the following issues. Typically, the 3D object and the conformally printed circuits are heated together in oven to fuse the printed nanoparticles and achieve low electrical resistance. There is a trade-off between sintering time and temperature in this sintering step. This sintering can be performed at high temperatures if a short sintering time of a few minutes is needed (e.g., ≈250–350 °C [2]) or for a longer time if lower sintering temperatures are desired (e.g., 150 °C for 30 min [14] or 80 °C to 1 h [4]). Therefore, this step either limits the material of the 3D object that can be used, if shorter higher temperature sintering is used, or limits the process throughput if longer lower temperature sintering is used. Further, the use of oven in this sintering step limits the usable size and material of the 3D object. Laser sintering of the printed interconnects alleviates direct heating of the bulk of the 3D object but can still cause significant indirect heating of the 3D surface, requiring the use of more expensive thermally tolerant materials for the 3D object. Also, both the conformal printing process and the laser sintering process are time-consuming due their serial-writing nature. Furthermore, replacement of the direct written circuits requires the entire 3D object to be shipped to the production facility for remanufacturing. This can be a significant logistical issue where large 3D objects are involved.

Overall, the above issues constrain current conformal integration of circuits to niche applications characterized by limited size and material type of the 3D surfaces and limited circuit replaceability. Thus, there is a need for an approach that simultaneously avoids mechanical conformation of planar electronics, enables robust integration of the circuit with the desired surface, avoids direct heating of the 3D surface, and allows circuit replacement without involving the 3D object. To overcome these issues, the following paradigm has been proposed for separating the fabrication of 3D conformal circuits from their integration with the desired surface. In this paradigm (Fig. 1), nanomaterial-based interconnects are printed on planar polymer substrates, the printed interconnect–polymer assembly is formed to the shape of the desired surface, and the shaped assembly is adhesively attached to the 3D surface. This paradigm can simultaneously eliminate direct heating of the 3D object, enable robust assembly by preshaping the polymer to preferentially conform to the desired surface form, and allow easy detachment and reattachment of assemblies for replacement. The key bottleneck is that forming of the planar interconnect–polymer assembly will increase electrical resistance significantly [8], which must be compensated for by another processing step. Further, while the established large-area printing methods can be used to scalably print

[1]Corresponding author.

Manuscript received October 8, 2018; final manuscript received January 8, 2019; published online February 28, 2019. Assoc. Editor: Y. Lawrence Yao.

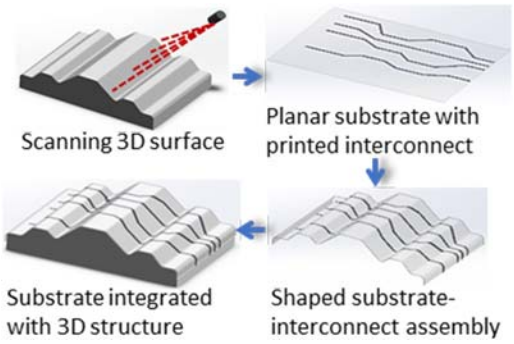

Fig. 1 Potential paradigm for integration of conformal circuits with rigid 3D surfaces

the planar circuits [15–22], the forming and the subsequent processing steps must be scalable, if this integration approach is to be amenable with large surfaces.

To meet this need, we investigate sequential thermoforming [23–25] and flash light sintering (FLS) [26–29] of planarly printed silver (Ag) nanowire (NW) interconnects on planar polycarbonate (PC) sheets. In this process, Ag NW inks (Fig. 2(*a*)) are printed on a PC sheet to fabricate planar interconnects (Fig. 2(*b*)). This planar assembly is thermoformed into the desired surface geometry by heating the interconnect–polymer assembly and pressing it mechanically onto a mold of desired shape (Fig. 2(*c*)). Thermoforming is a well-established and scalable process for shaping thermoplastic sheets into highly complex shapes. However, there is little work on investigating the change in conductivity of nanomaterial structures printed on the polymer during this process. This formed interconnect–polymer assembly is then subjected to FLS (Fig. 2(*d*)). In FLS, pulsed light (continuous energy spectrum from 400 to 700 nm) from a xenon lamp is incident on the NWs. This light is absorbed by the NWs selectively due to plasmonic effects resulting in localized heating, neck growth at the contacts between NWs, and an increase in conductivity of the printed structure. The simultaneously high sintering speed (milliseconds), large-area (e.g., greater than 1 ft × 0.75 in. optical footprint here), and low substrate damage in FLS provide significant advantages over oven and laser sintering [29–35]. Significant past work on FLS has demonstrated sintering of metallic (Ag [34], Ni [36], and Cu [37,38]), semiconductive (CdS [39], CuS [40], CdTe [41], and TiO_2 [42]), and thermoelectric (bismuth telluride [43]) thin and thick films. However, most work in FLS has been performed for interconnects on flat substrates. There is little investigation of how FLS affects electrical resistance in 3D interconnects, as is the case in our process. The scalability of planar printing, thermoforming, and FLS also provide inherent scalability to the proposed process. However, there has been no investigation of whether FLS can sufficiently compensate for the increase in resistance inevitable in the thermoforming step.

This paper develops the above proposed process and characterizes the associated process–structure–property relationships. The dependence of interconnect resistance on the forming strain and FLS fluence is characterized. The changes in the interconnect morphology due to thermoforming and FLS are examined. Thermal analysis of FLS is performed to understand spatial temperature evolution during the process. These efforts uncover the physical mechanisms underlying the observed process–structure–property relationships. The process capability is further demonstrated via a simple conformal LED-lighting circuit for complex 3D surfaces. The impact of this new process and integration paradigm on enhancing scalability and versatility in conformal circuit manufacturing is discussed.

Methods

Experimental Methods. Ag NWs (150 μm length, 100 nm diameter, ACS Materials) were suspended in ethanol at 5 mg/ml concentration without any dispersant to prepare a stable ink, as shown in Fig. 2(*a*). Wide-area AJP with a mask was used to deposit the ink on 500 μm thick PC sheets, as demonstrated in Fig. 2(*b*). We note that printing NWs of this concentration and size has also been performed by large-area print heads without a mask [21,22]. During printing, the sample stage was preheated to 70 °C to quickly evaporate the ethanol. For process characterization, the printed pattern was a straight interconnect with larger pads at each end. The liquid flowrate was controlled by a feeder and an atomizer. The feeder contained a syringe pump that pumped the Ag NW ink with a volumetric flowrate of 1.5 ml/min. The atomizer used compressed air supply at 0.5 psi to aerosolize the ink. The deposition path was controlled by a three-axis stage, with the polymer substrate mounted on an *X*–*Y* stage and the aerosol nozzle mounted on the *Z*-axis above it. The nozzle height (i.e., *Z*-axis position) was fixed at 35 mm above the substrate. Once the aerosol jet was turned on, the in-plane motion of the polymer was controlled by proportional integral derivative controllers for the *X*–*Y* axis with inbuilt G-code software from the stage supplier (Zaber Inc.). The end points of the interconnect, i.e., the two points at the ends of the interconnect pads, were specified, and linear interpolation was used to deposit the ink in a straight line between the two points. Thus, the *X*–*Y* stage simply moved back and forth in a straight line to deposit the desired number of passes. This deposition approach deposited 0.04 ml of the ink per pass of the aerosol nozzle. After the interconnect pattern was deposited, the printed substrate was taken out of the AJP stage and the mask was removed from the substrate. The number of printing passes varied from 100, 140, and 180 to obtain interconnects of varying thicknesses.

The interconnect–PC assembly was then thermoformed by heating it above the polymer's glass-transition temperature (T_g), as shown in Fig. 2(*c*). The T_g for PC was measured using differential scanning calorimetry as 153 °C, which is within the range of 145–155 °C in the previous study [44]. During our experiments, the polymer substrate was heated to 200 °C before forming (as measured by a thermal camera), and the total thermoforming time was 90 s. The molds were fabricated with polyetherimide using stereolithography-based 3D printing. Molds with a circular cap cross section (Fig. 3(*a*)) characterized by a maximum mold angle θ_m

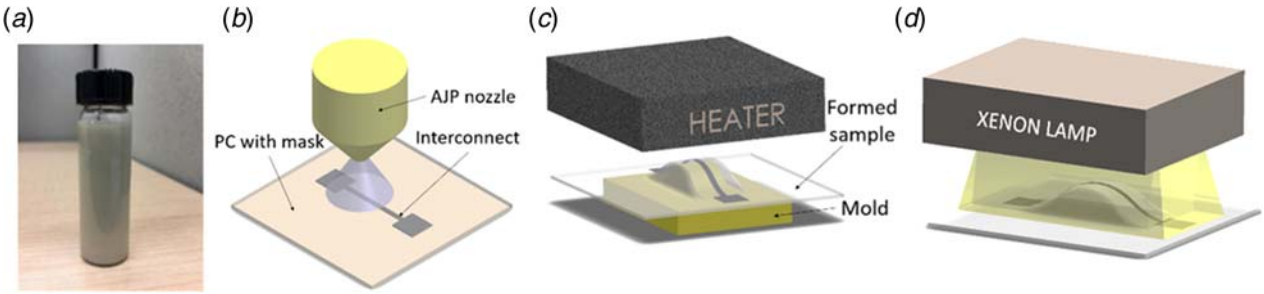

Fig. 2 (*a*) Silver nanowire ink used in this work; schematics of (*b*) AJP, (*c*) thermoforming, and (*d*) FLS

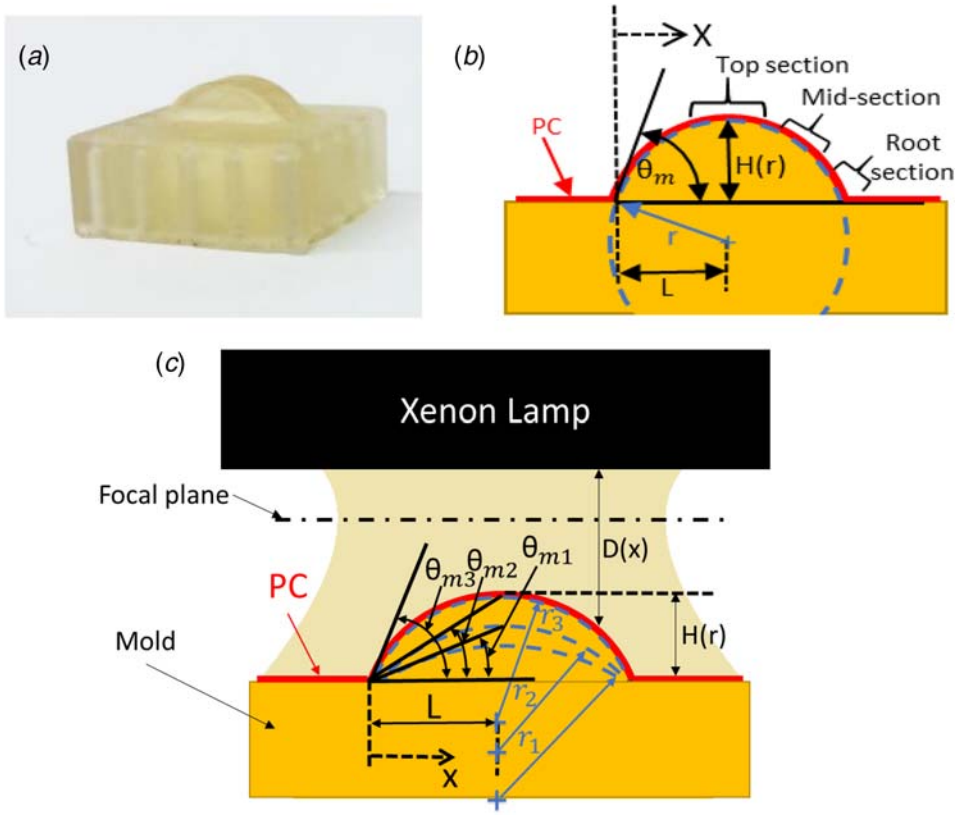

Fig. 3 (*a*) Mold ($\theta_m = 100\%$) used to characterize the effect of thermoforming, (*b*) mold terminology, and (c) schematic of spatially varying irradiance during FLS of the interconnect–polymer assembly

(Fig. 3(*b*)) were used to characterize the effect of thermoforming on resistance. The interconnect was aligned to be along the centerline of the bump in the mold, so that primarily uniaxial strain was imposed on the interconnect. Thus, the strain was maximum at the root section of the mold and lowest at the top section of the mold (Fig. 3(*b*)). The ε maximum nominal strain on the polymer ε_m can be written as shown in Eq. (1) and varied from 30% to 190% by fixing mold width L (7.25 mm) and changing mold radius r to change θ_m from 40 deg to 70 deg. Since L and r were fixed, the total mold height H (Fig. 3(*c*)) increased with θ_m as $H = r(1 - \cos\theta_m)$.

$$\varepsilon_m = 1/\cos\theta_m - 1 = 1/\sqrt{\left[1 - \left(\frac{L}{r}\right)^2\right]} - 1 \tag{1}$$

$$Q = \sum_{\lambda=400\text{ nm}}^{\lambda=700\text{ nm}} \frac{P_a(\lambda)}{P_i(\lambda)} x\, X(\lambda) x \left(\frac{1}{D^2}\right)\left(\frac{V}{3120}\right)^{2.4} \tag{2}$$

This thermoformed assembly was subjected to FLS (Sinteron 3000 system; Xenon Corporation), as shown in Fig. 2(*d*). This lamp has a minimum optical footprint, and therefore working area, of 1 ft × 0.75 in. The thermal power density Q absorbed at an arbitrary location on the 3D interconnect was obtained as shown in Eq. (2). In Eq. (2), Q depends on distance D from the surface of the lamp, where $D \geq$ distance of the focal plane from lamp surface (Fig. 3(*c*)); the fraction of total optical irradiance at given wavelength λ, i.e., $X(\lambda)$; ratio of absorbed power $P_a(\lambda)$ to incident power $P_i(\lambda)$ on the interconnect; and the lamp voltage V in kV. The term $(V/3120)^{2.4}$ denotes the total optical irradiance at a given voltage at the focal plane (1 in. from the lamp surface), as specified by the manufacturer. The optical irradiance from the lamp and this approach to quantify optical energy absorbed by the deposited nanoparticles have been validated and successfully used in previous works on FLS [28,29,45]. The base of the formed PC was fixed at 1.5 in. away from the surface of the lamp, and the lamp voltage was fixed at 3 kV. The optical fluence at the PC base varied, as shown in Table 1, for a total of three optical pulses and a maximum FLS time of 1.7 s. The line resistance of the interconnect was measured by attaching copper tape with highly conductive silver paste to the end pads of the interconnects, and then attaching the copper tape to a Keithley sourcemeter using alligator clips. The use of the conductive silver paste reduces issues with contact resistance between the copper tape and the interconnect. This approach to measure line resistance in conformal interconnects has also been used in the past work in conformal nanoparticle printing [4]. The interconnect morphology was analyzed via scanning electron micrography (SEM; Zeiss Sigma Field Emission 8100). The optical absorption of the deposited Ag NWs was measured using an UV–vis spectrophotometer equipped with an integrating sphere, for use in the thermal analysis of FLS.

Computational Methods. A thermal finite element analysis (FEA) was implemented in COMSOL to understand how the nonplanarity of the interconnect in our process influences temperature

Table 1 FLS parameters

Parameter	Optical fluence at PC base		
	1 J/cm^2	3 J/cm^2	5 J/cm^2
On-time, t (μs)	143	430	715
Off-time (ms)	100	283	560

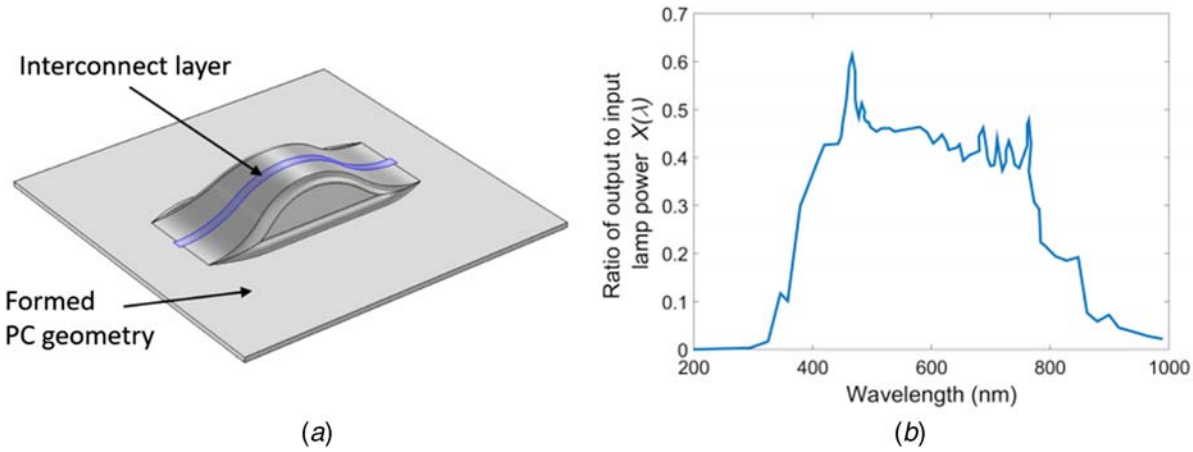

Fig. 4 Thermal model with formed PC geometry for $\varepsilon_m = 100\%$ and the interconnect layer

evolution during FLS. The formed PC geometry with $\varepsilon_m = 100\%$ was used with the interconnect modeled as a thin layer, as shown in Fig. 4(*a*). A spatially varying heat source was specified on the interconnect, based on Eq. (2), with $X(\lambda)$ obtained from the xenon lamp spectrum supplied by the manufacturer (Fig. 4(*b*)). The optical absorption curves of the silver layer were obtained from the above described spectrophotometry. The heat source was applied only to the thin Ag interconnect domain since the PC used here is visibly transparent, resulting in negligible optical absorption of the xenon lamp light. The thermal properties of this thin layer were assumed to be temperature-invariant and equivalent to that of the bulk material for simplicity. Although this assumption will not yield a quantitatively exact temperature evolution, it provides qualitative insights into temperature gradients without the significant complications of coupling densification and thermal properties [29]. The thermal properties used in the model are described in Table 2. Convective heat transfer boundary condition (convective coefficient, 5 W/m^2 K) was included at all the surfaces, except the lower surface of the PC, which had a constant temperature of 25 °C. This lower surface boundary condition reflects the fact that we had a gray metal substrate below the polymer, which absorbed light but was also thermally connected to the larger metallic structure of the setup, which we assumed acted like a heat sink to quickly conduct away the heat and keep the lower surface at room temperature. A square waveform with a 10% rise-time and 10% decay-time was used for temporal evolution of the pulse irradiance during the pulse on time, since this has shown good ability to predict temperature evolution in our past work on FLS [28,29,45].

Results and Discussion

Figure 5(*a*) shows a planar interconnect after aerosol-jet printing. The line width was 750 μm, and the thickness was measured by SEM to be 400, 600, and 800 nm for 100, 140, and 180 passes respectively. The corresponding as-deposited resistance was 7.8, 7.1, and 5.2 Ω/cm, respectively, due to the increased interconnect thickness [46]. In this work, we use line resistance rather than bulk resistivity for two reasons. First, the line resistance and the change in it after thermoforming and FLS are of chief interest to a circuit designer who wants to understand the resistance along the surface of the formed interconnect–polymer assembly. Thus, line resistance has been often reported when considering conformally printed interconnects [4]. Second, since the strain across the interconnect is not uniform (as mentioned in the Experimental Methods section), the thickness is expected to change smoothly across the interconnect length. This makes it difficult to quantify resistance as a single resistivity value. Figure 5(*b*) shows thermoformed samples with different forming angles θ_m. Figures 5(*c*) and 5(*d*) show how resistance changes due to thermoforming and FLS fluence. The means and standard deviations for these plots were obtained from at least three samples for each fluence and θ_m. The standard deviations of the post-FLS samples in these plots are not shown for purposes of clarity or are not visible in some cases. However, we note that the standard deviation of the post-FLS samples was not greater than 0.7 Ω/cm. The resistance of the copper tape and silver paste was measured by joining a copper tape (of same length as used in measurements) end-to-end to another copper tape with the silver paste and then measuring the resistance across this assembly. Since this resistance was around 1.3 Ω, the copper tape and epoxy contributed no more than 8% of the measured total resistance in any stage of the process, for any of the cases considered here. Thus, the copper tape and silver paste had very little influence on the measured line resistance.

Table 2 Thermal properties used in finite element analysis

Property	Silver	Polycarbonate
Thermal conductivity (W/m K)	419	0.22
Density (kg/m^3)	10,491	1200
Heat capacity (J/kg K)	234	1300

These plots lead to the following interesting observations. In general, the resistance increases significantly after thermoforming but also decreases significantly after FLS. As shown in Fig. 5(*d*), at pulse fluence of 3 J/cm^2, the post-FLS resistance is 25% lower than the as-deposited resistance for $\varepsilon_m = 30\%$ and 55%, comparable for $\varepsilon_m = 100\%$, and about 38% higher for $\varepsilon_m = 190\%$. Thus, FLS plays the key role of compensating for the increase in resistance after thermoforming. The typical resistance achieved by vacuum deposition in planar electronics (≈7.5 Ω/cm for few 100 nm thickness, [4]) is lower than the maximum post-FLS resistance here (≈12 Ω/cm at $\varepsilon_m = 190\%$), but it is similar to that achieved at lower ε_m.

In Fig. 5(*d*), the change in resistance after thermoforming is similar at lower ε_m (30% and 55%) but increases substantially at higher ε_m (100% and 190%). The reason for this difference can be observed from SEM images at the root and the top section of the interconnects, as shown in Fig. 6. A greater number of microcracks, across the line width, are formed at the root of the interconnect than at the top (Figs. 6(*a*) and 6(*b*)). This is due to greater strain at the root section than at the top section. The orientation of these cracks is consistent with our assumption of primarily uniaxial plane strain along the interconnect length, since previous studies have shown that in metal films on polymers subject to stretching, the film develops cracks perpendicular to the tensile direction [47,48]. These cracks reduce the effective electrical percolation

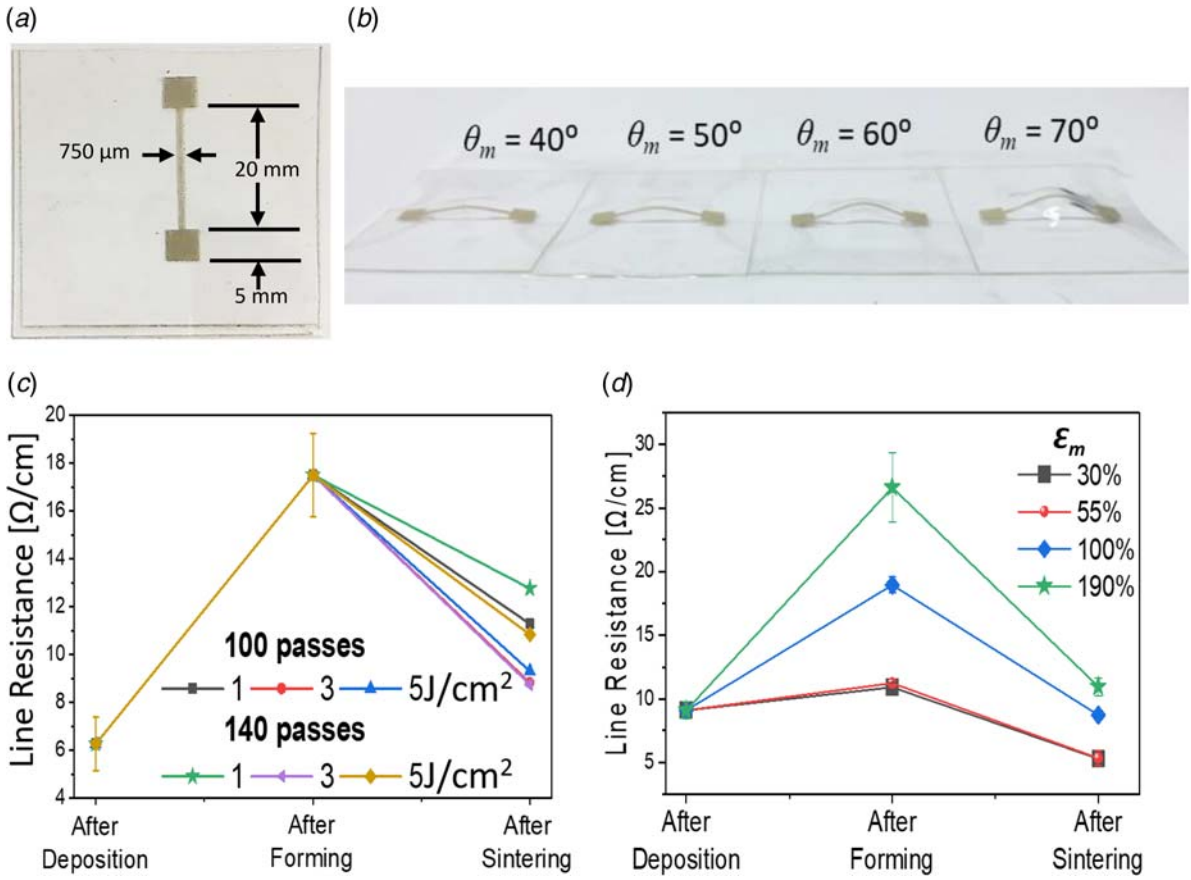

Fig. 5 (*a*) Aerosol-jet printed planar Ag NW interconnect, (*b*) postformed and post-FLS interconnect–polymer assemblies for different θ_m, (*c*) change in resistance for $\varepsilon_m = 100\%$ with number of printing passes and pulse fluence, and (*d*) change in resistance with maximum strain for 140 printing passes and 3 J/cm^2 pulsefluence (optimal parameters)

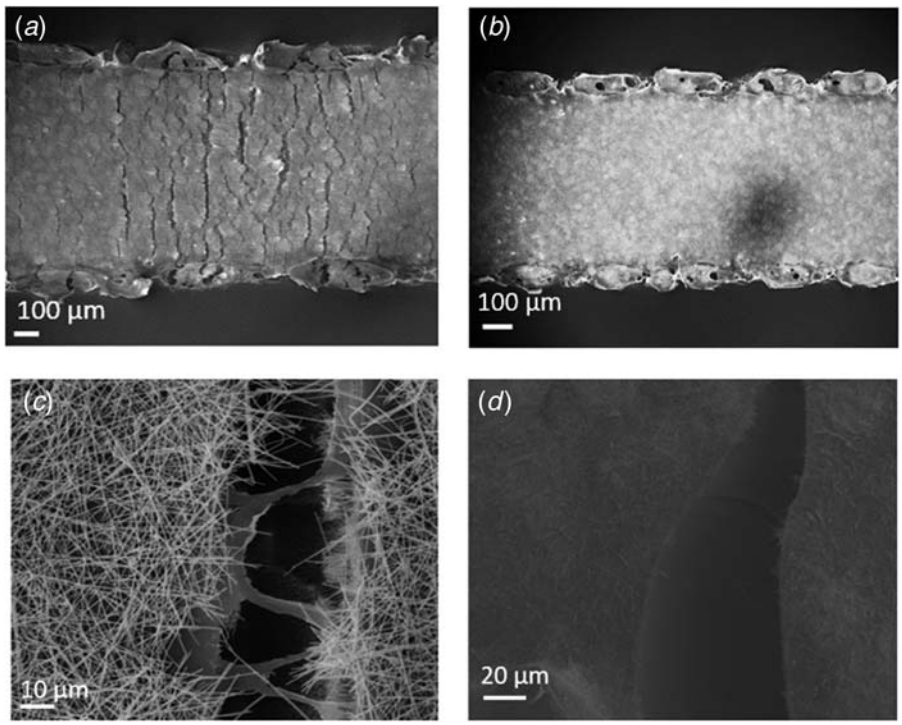

Fig. 6 SEM images of interconnects with 140 printing passes after thermoforming: For $\varepsilon_m = 100\%$ at (*a*) root section and (*b*) top section; (*c*) $\varepsilon_m = 30\%$ and (*d*) $\varepsilon_m = 100\%$ at the root section

across the crosssection of the interconnect, causing the observed thermoforming-induced increase in resistance. The magnitude of change in resistance with ε_m depends on the morphology across the crack width. At lower strain (e.g., $\varepsilon_m = 30\%$, Fig. 6(*c*)), some percolation is still retained across the cracks via crack width spanning ligaments. At a higher strain ($\varepsilon_m = 100\%$, Fig. 6(*d*)), these ligaments break. The resulting complete elimination of electron flow across the cracks significantly increases the resistance. This indicates a strain limit beyond which the postforming resistance of the interconnect increases more rapidly.

To understand why FLS reduces the resistance, the post-FLS SEM images are examined in Fig. 7. Comparing Figs. 7(*a*) and 7(*b*) with Figs. 6(*a*) and 6(*b*) shows that the thermoforming induced cracks in the interconnect grow after FLS. This is due to thermal stresses during FLS, mismatch in thermal expansion coefficient between the Ag and PC, and greater stress concentrations at the interconnect edges [49]. By itself, this phenomenon should increase post-FLS resistance beyond the postforming resistance. However, Fig. 7(*d*) shows FLS-induced neck growth at the NW contacts in the regions of the interconnect away from the cracks. This should reduce the contact resistance between the NWs [50], wherever NW contact is possible after thermoforming, and thus reduce the overall line resistance as well. Given the significant post-FLS reduction in resistance in Figs. 5(*c*) and 5(*d*), the above observations indicate that neck growth induced reduction in resistance due to FLS dominates over the concurrent increase in resistance due to thermoforming- and FLS-induced crack growth. At the same time, Fig. 7(*c*) shows that the FLS-induced neck growth is lesser at the root section than at the top section. The number of necks per unit area of the SEM images, measured over at least 3 images, increased from 0.6 necks/μm^2 at the root section to 3.1 necks/μm^2 at the top section. The reasons for this will be discussed shortly when describing the results from the thermal model.

Figure 5(*c*) shows process limits in terms of the interconnect thickness and pulse fluence. The postforming resistance for 180 printing passes was not measurable compared to finite values for 140 and 100 printing passes. This is because the thermoforming induced cracks at the root section propagated completely across the line width for 180 printing passes, as shown in Fig. 7(*e*). This caused a complete loss in electrical percolation in the interconnect compared to the partial crack propagation for 140 printing passes observable in Fig. 7(*f*). We hypothesize that this is due to greater deposition passes increasing both interconnect density and thickness, resulting in greater effective stiffness, greater stress, and thus greater crack growth during thermoforming. In Fig. 5(*c*), the post-FLS resistance is highest at fluence of 1 J/cm^2, decreases at 3 J/cm^2, and then increases again at 5 J/cm^2. Past works on planar FLS of silver nanowires has reported nanoscale degradation and evaporation of nanowires beyond a limiting fluence [51–53]. This is likely the operative mechanism behind the existence of a limiting fluence in our experiments as well. The optimum FLS fluence and interconnect thickness were found to be 3 J/cm^2 fluence and 140 printing passes (i.e., 600 nm thickness), respectively. These were the parameters used to understand the influence of ε_m in Fig. 5(*d*).

Figure 5(*d*) shows that increasing ε_m results in greater post-FLS reduction in resistance. Deeper understanding of this phenomenon is obtained by considering results from the thermal analysis. Figure 8(*a*) shows the temperature contours at the peak of the third FLS pulse for the optimal FLS fluence and interconnect thickness found above. As shown in Fig. 8(*b*), there is a significant temperature gradient across the length of the interconnect with greater temperatures at the top section. A common assumption made during FLS on planar substrates has been that the film temperature is uniform during the process [28,29]. This is based on the assumption of negligible effect of thermal conductivity, due to the low Biot number of the interconnects, and the fact of uniform fluence across the film. The temperature gradients observed here indicate that this assumption can no longer be used when analyzing FLS of 3D interconnects. Further, the higher temperatures at the top section also indicate that the neck growth should be lesser at the root section and greater at the top section. This gradient in sintering is supported by the difference in inter-NW neck growth between the top section in Fig. 7(*c*) and the root section in Fig. 7(*d*). These insights indicate that models of FLS of 3D interconnects need to consider local variations in thermal conductivity, which would develop due to gradients in thermal contact resistance at inter-NW contacts induced by local variations in inter-NW neck growth [54].

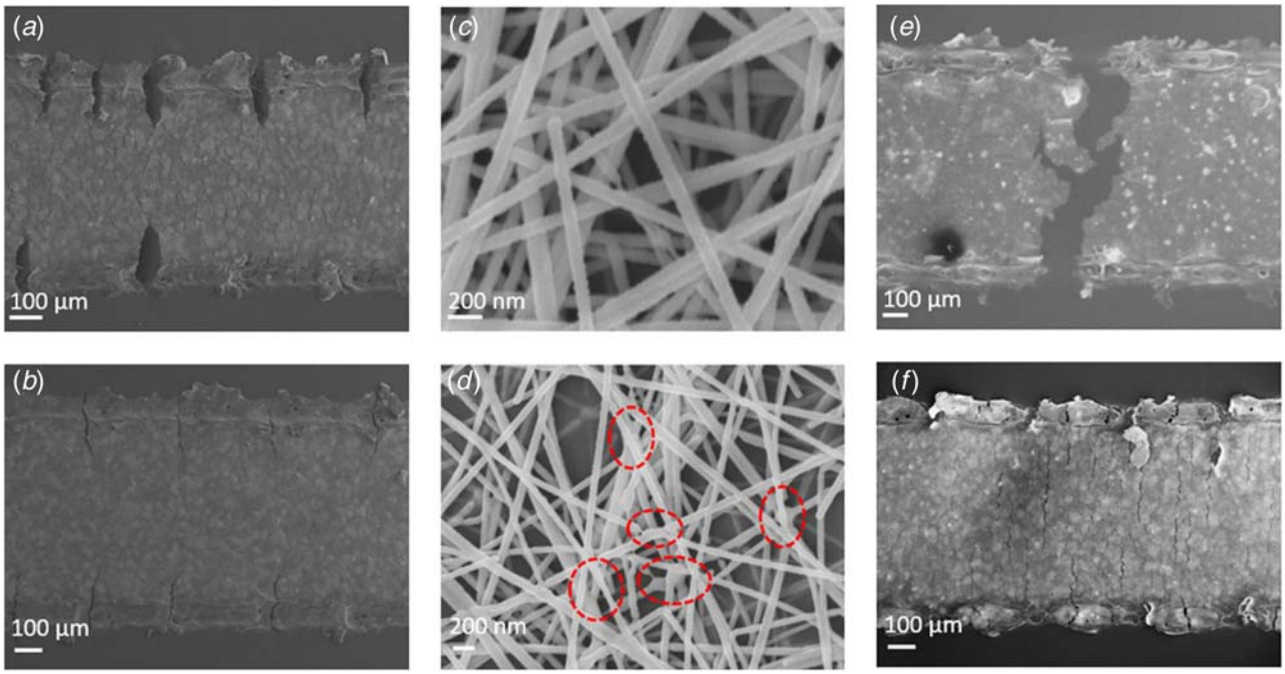

Fig. 7 Post-FLS SEM images for 3 J/cm^2 pulse fluence, 140 printing passes and $\varepsilon_m = 100\%$ at (*a*) the root section and (*b*) the top section; zoomed in views at (*c*) the root section and (*d*) the top section; The red dotted circles denote inter-NW necks; Postforming SEM images at the root section for $\varepsilon_m = 100\%$ for (e) 180 and (*f*) 140 printing passes

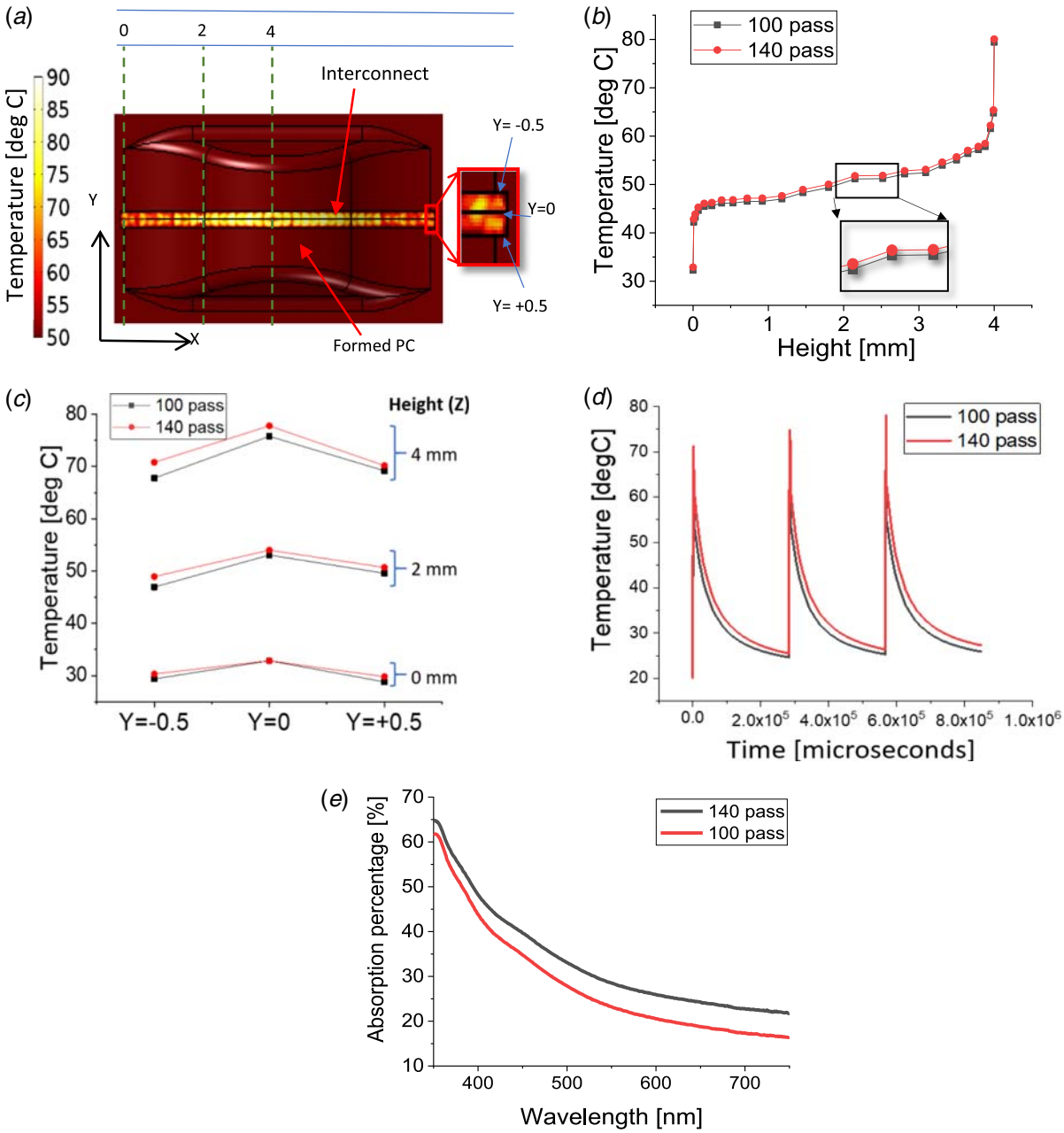

Fig. 8 Thermal model results for $\varepsilon_m = 100\%$ formed PC geometry at the peak of third pulse: (*a*) temperature contours, (*b*) interconnect temperature as a function of height (c) variation in temperature across the interconnect width, (*d*) Temperature evolution at the top section of the interconnect for multiple consecutive pulses, and (e) UV–Vis absorption spectrum for unsintered Ag NWs on PC with 100 and 140 printing passes

These temperature gradients also explain the relatively greater post-FLS resistance reduction for higher ε_m in Fig. 5(*d*). The temperature gradient is due to the spatial variation in incident fluence on the interconnect per Eq. (2). As θ_m and ε_m increase, the mold height $H(=r(1-\cos\theta_m))$ also increases. Thus, a greater portion of the formed interconnect gets closer to the lamp surface, as shown in Fig. 3(*c*). As is observable from Eq. (2), this increases the fluence and therefore the temperature and inter-NW neck growth over a greater length of the interconnect. This leads to greater reduction in resistance after FLS. The FEA results also show that the FLS temperature is slightly higher for 140 printing passes than for 100 printing passes (Figs. 8(*b*)–8(*d*)). This is because greater film thickness results in greater optical absorption, as shown in Fig. 8(*e*).

The developed thermoforming-FLS process was also used to integrate conductive interconnects on more complex surfaces. The stepped pyramid geometry in Fig. 9(*a*) was used to examine how the process deals with concave corners. The stepped dome shape in Fig. 9(*b*) was used to examine the inclusion of both concave and convex features in the same geometry. The optimal process parameters described earlier were used. The resistance after forming was 17.8 Ω/cm for the stepped pyramid, higher than that for the stepped dome (13.8 Ω/cm). However, the post-FLS line resistance for both cases was 7.8 Ω/cm, indicating lesser FLS-induced resistance reduction for the stepped dome. This was because the concave feature in the mid-section of the stepped pyramid was closer to the lamp surface than the concave feature at the base of the stepped dome, which, based on the thermal analysis presented earlier, resulted in greater FLS-induced temperature and neck growth at the midsection concave feature in the stepped pyramid. This is why FLS induced a greater reduction in resistance

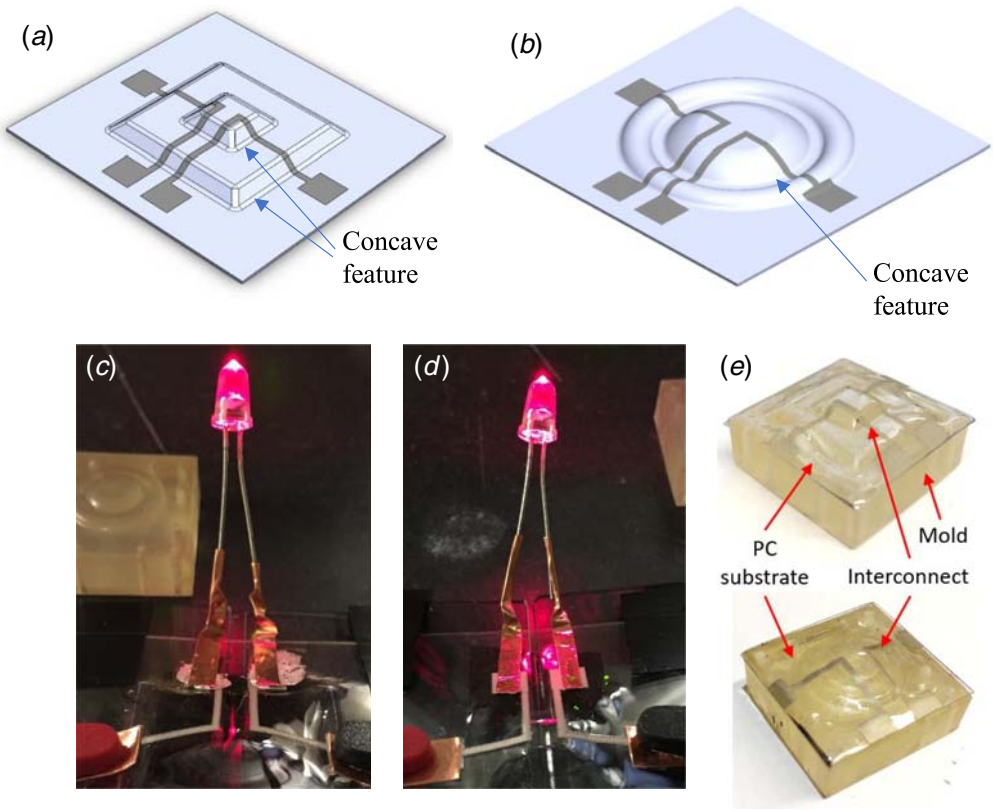

Fig. 9 Geometry of PC surface and interconnect for (*a*) stepped pyramid and (*b*) stepped dome shape; Demonstration of conformal interconnects using an LED (*c*) stepped pyramid and (*d*) Stepped dome shape; (*e*) Integrated PC–interconnect assemblies

for the stepped pyramid case. The interconnects could light up a red LED fully at 3 V and partially at 1.7 V, as shown in Figs. 9(*c*) and 9(*d*). As illustrated in Fig. 9(*e*), the interconnect–PC assemblies were easily adhesively integrated with the mold surface, which has the same form as the desired 3D surface.

The total processing time for each of these 1 square inch surfaces was 90.8 s. With an increase in surface size, to say 1 square foot, the thermoforming process will require larger machines, but will not need longer time. Such larger machines are easily available today. The optical footprint of FLS here is 1 ft × 0.75 in. or greater, implying that with in-plane overlap between consecutive optical footprints the FLS time would increase to around 10 s. Thus, the total time needed for this larger surface would be less than 2 min, which is much lesser than that needed for conformal printing over a similar area. It is worth noting that we also attempted to perform FLS first, followed by thermoforming. However, even with a higher FLS fluence and lower strain, the minimum resistance achievable was at least 10 times that obtained here. This is because the neck growth between the NWs during FLS increased the stiffness of the interconnect, leading to a greater crack growth and failure of the interconnect during thermoforming.

Conclusion

To summarize, this paper develops a new process that can transform planar printed circuits on thermoplastic sheets into freeform interconnect–polymer assemblies for facile integration with a desired 3D surface. This process concurrently leverages the inherently high scalability of the established planar printing and thermoforming processes and that of the emerging FLS process. Importantly, FLS-induced inter-NW neck growth significantly compensates for crack growth induced reduction in resistance during thermoforming and FLS. The observed nonlinear dependence of electrical conductivity on surface form, FLS fluence, and interconnect thickness is elucidated in terms of the underlying interconnect morphology and temperature evolution. Significant gradients in temperature and neck growth between the NWs are found, indicating the need to consider local variations in effective thermal properties during FLS analysis.

The demonstrated circuit integration paradigm is robust because the interconnect–polymer assembly is preshaped to the target surface geometry. It also enables easy circuit replacement and complete elimination of any heating of the 3D object. These advantages, when combined with the process scalability, create the potential for circuit integration that is agnostic to the object size and material. We note that conformal 3D printing on thermoformed polymer sheets (without interconnects), followed by FLS, could be an alternative to the process described here. However, this approach would lose the high scalability that is now available with planar printing approaches.

At the same time, we observe that gradation in sample positioning to compensate for gradients in degree of inter-NW neck growth may further lower post-FLS resistance in our process. This approach could be combined with xenon lamp reflectors that have a longer focal distance to accommodate surface form factors with a greater height. Further, the use of reflective surfaces below the polymer might allow absorption of light reflected from this surface by regions of the formed interconnect farther away from the lamp surface (e.g., the root section) to enable greater neck growth. Fundamentally, there is likely a change in the thickness of the interconnect after thermoforming. This will also contribute to the increase in resistance after forming, albeit likely not as strongly as the disruption in percolation due to crack growth. Fabricating the interconnect on flat inclined surfaces to measure the uniform change in thickness and bulk resistivity can help understand the contribution of this thickness change to the resistance change. Investigating these avenues to further reduce resistance is the focus of our future work.

Acknowledgment

The authors acknowledge the help provided by Mr. Michael Dexter in preparing the molds for thermoforming. This work was supported by the National Science Foundation USA (Grant Nos. CMMI #1809289 and CBET #1449383).

References

[1] Le Borgne, B., De Sagazan, O., Crand, S., Jacques, E., and Harnois, M., 2017, "Conformal Electronics Wrapped Around Daily Life Objects Using an Original Method: Water Transfer Printing," ACS Appl. Mater. Interfaces, **9**(35), pp. 29424–29429.
[2] Adams, J. J., Duoss, E. B., Malkowski, T. F., Motala, M. J., Ahn, B. Y., Nuzzo, R. G., Bernhard, J. T., and Lewis, J. A., 2011, "Conformal Printing of Electrically Small Antennas on Three-Dimensional Surfaces," Adv. Mater., **23**(11), pp. 1335–1340.
[3] Kim, D.-H., Xiao, J., Song, J., Huang, Y., and Rogers, J. A., 2010, "Stretchable, Curvilinear Electronics Based on Inorganic Materials," Adv. Mater., **22**(19), pp. 2108–2124.
[4] Jo, Y., Kim, J. Y., Jung, S., Ahn, B. Y., Lewis, J. A., Choi, Y., and Jeong, S., 2017, "3D Polymer Objects With Electronic Components Interconnected Via Conformally Printed Electrodes," Nanoscale, **9**(39), pp. 14798–14803.
[5] Meng, F., and Huang, J., 2018, "Fabrication of Conformal Array Patch Antenna Using Silver Nanoink Printing and Flash Light Sintering, " AIP Adv., **8**(8), p. 085118.
[6] Bausch, N., Dawkins, D. P., Frei, R., and Klein, S., 2016, "3D Printing onto Unknown Uneven Surfaces," IFAC-PapersOnLine, **49**(21), pp. 583–590.
[7] Wu, S.-Y., Yang, C., Hsu, W., and Lin, L., 2015, "3D-Printed Microelectronics for Integrated Circuitry and Passive Wireless Sensors," Microsyst. Nanoeng., **1**, 15013.
[8] Lucchini, R., Cattarinuzzi, E., Maraghechi, S., Gastaldi, D., Adami, A., Lorenzelli, L., and Vena, P., 2016, "Delamination Phenomena in Aluminum/Polyimide Deformable Interconnects: In-Situ Micro-Tensile Testing," Mater. Des., **89**, pp. 121–128.
[9] Gray, D. S., Tien, J., and Chen, C. S., 2004, "High-Conductivity Elastomeric Electronics," Adv. Mater., **16**(5), pp. 393–397.
[10] Kim, Y., Lee, D. H., Kim, D.-H., and Kim, J.-W., 2015, "Flexible and Transparent Electrode Based on Silver Nanowires and a Urethane Acrylate Incorporating Diels–Alder Adducts," Mater. Des., **88**, pp. 1158–1163.
[11] Hwang, B., An, C.-H., and Becker, S., 2017, "Highly Robust Ag Nanowire Flexible Transparent Electrode With UV-Curable Polyurethane-Based Overcoating Layer," Mater. Des., **129**, pp. 180–185.
[12] Kim, D.-H., Kim, Y., and Kim, J.-W., 2016, "Transparent and Flexible Film for Shielding Electromagnetic Interference," Mater. Des., **89**, pp. 703–707.
[13] Paulsen, J. A., Renn, M., Christenson, K., and Plourde, R., 2012, "Printing Conformal Electronics on 3D Structures With Aerosol Jet Technology," 2012 Future of Instrumentation International Workshop (FIIW) Proceedings, Gatlinburg, TN, Oct. 8–9, pp. 1–4.
[14] Kim, S. Y., Kim, K., Hwang, Y. H., Park, J., Jang, J., Nam, Y., Kang, Y., Kim, M., Park, H. J., Lee, Z., Choi, J., Kim, Y., Jeong, S., Bae, B. S., and Park, J. U., 2016, "High-Resolution Electrohydrodynamic Inkjet Printing of Stretchable Metal Oxide Semiconductor Transistors With High Performance," Nanoscale, **8**(39), pp. 17113–17121.
[15] Vaithilingam, J., Saleh, E., Körner, L., Wildman, R. D., Hague, R. J. M., Leach, R. K., and Tuck, C. J., 2018, "3-Dimensional Inkjet Printing of Macro Structures from Silver Nanoparticles," Mater. Des., **139**, pp. 81–88.
[16] Mueller, J., Shea, K., and Daraio, C., 2015, "Mechanical Properties of Parts Fabricated With Inkjet 3D Printing Through Efficient Experimental Design," Mater. Des., **86**, pp. 902–912.
[17] Qin, H., Cai, Y., Dong, J., and Lee, Y.-S., 2016, "Direct Printing of Capacitive Touch Sensors on Flexible Substrates by Additive E-Jet Printing With Silver Nanoinks," J. Manuf. Sci. Eng., **139**(3), pp. 031011–0310117.
[18] Salary, R., Lombardi, J. P., Rao, P. K., and Poliks, M. D., 2017, "Online Monitoring of Functional Electrical Properties in Aerosol Jet Printing Additive Manufacturing Process Using Shape-From-Shading Image Analysis," J. Manuf. Sci. Eng., **139**(10), pp. 101010–101013.
[19] Sun, H., Wang, K., Li, Y., Zhang, C., and Jin, R., 2017, "Quality Modeling of Printed Electronics in Aerosol Jet Printing Based on Microscopic Images," J. Manuf. Sci. Eng., **139**(7), pp. 07101201–07101210.
[20] Qin, H., Wei, C., Dong, J., and Lee, Y.-S., 2016, "Direct Printing and Electrical Characterization of Conductive Micro-Silver Tracks by Alternating Current-Pulse Modulated Electrohydrodynamic Jet Printing," J. Manuf. Sci. Eng., **139**(2), pp. 02100801–02100810.
[21] Finn, D. J., Lotya, M., and Coleman, J. N., 2015, "Inkjet Printing of Silver Nanowire Networks," ACS Appl. Mater. Interfaces, **7**(17), pp. 9254–9261.
[22] Lu, H., Na Wu, J. L., Nie, S., Luo, Q., Mab, C.-Q., and Cui, Z., 2015, "Inkjet Printed Silver Nanowire Network as Top Electrode for Semi-Transparent Organic Photovoltaic Devices," Appl. Phys. Lett., **106**(9), pp. 093302.
[23] Yang, C., and Hung, S.-W., 2004, "Modeling and Optimization of a Plastic Thermoforming Process," J. Reinf. Plast. Compos, **23**(1), pp. 109–121.
[24] Guzman-Maldonado, E., Hamila, N., Naouar, N., Moulin, G., and Boisse, P., 2016, "Simulation of Thermoplastic Prepreg Thermoforming Based on a Visco-Hyperelastic Model and a Thermal Homogenization," Mater. Des., **93**, pp. 431–442.
[25] Ropers, S., Kardos, M., and Osswald, T. A., 2016, "A Thermo-Viscoelastic Approach for the Characterization and Modeling of the Bending Behavior of Thermoplastic Composites," Compos. Part A Appl. Sci. Manuf., **90**, pp. 22–32.
[26] Kwak, J. H., Chun, S. J., Shon, C.-H., and Jung, S., 2018, "Back-Irradiation Photonic Sintering for Defect-Free High-Conductivity Metal Patterns on Transparent Plastic," Appl. Phys. Lett., **112**(15), pp. 153103.
[27] Niittynen, J., Sowade, E., Kang, H., Baumann, R. R., and Mäntysalo, M., 2015, "Comparison of Laser and Intense Pulsed Light Sintering (IPL) for Inkjet-Printed Copper Nanoparticle Layers," Sci. Rep., **5**, p. 8832.
[28] Dexter, M., Gao, Z., Bansal, S., Chang, C.-H., and Malhotra, R., 2018, "Temperature, Crystalline Phase and Influence of Substrate Properties in Intense Pulsed Light Sintering of Copper Sulfide Nanoparticle Thin Films," Sci. Rep., **8**(1), p. 2201
[29] Bansal, S., and Malhotra, R., 2016, "Nanoscale-Shape-Mediated Coupling Between Temperature and Densification in Intense Pulsed Light Sintering," Nanotechnology, **27**(49), pp. 495602.
[30] Kang, J., Ryu, J., Kim, H., and Hahn, H., 2011, "Sintering of Inkjet-Printed Silver Nanoparticles at Room Temperature Using Intense Pulsed Light," J. Electron. Mater., **40**(11), pp. 2268.
[31] Hwang, H.-J., Joo, S.-J., and Kim, H.-S., 2015, "Copper Nanoparticle/Multiwalled Carbon Nanotube Composite Films With High Electrical Conductivity and Fatigue Resistance Fabricated via Flash Light Sintering," ACS Appl. Mater. Interfaces, **7**(45), pp. 25413–25423.
[32] Garnett, E. C., Cai, W., Cha, J. J., Mahmood, F., Connor, S. T., Christoforo, M. G., Cui, Y., McGehee, M. D., and Brongersma, M. L., 2012, "Self-Limited Plasmonic Welding of Silver Nanowire Junctions," Nat. Mater., **11**(3), pp. 241.
[33] Jang, Y.-R., Chung, W.-H., Hwang, Y.-T., Hwang, H.-J., Kim, S.-H., and Kim, H.-S., 2018, "Selective Wavelength Plasmonic Flash Light Welding of Silver Nanowires for Transparent Electrodes With High Conductivity," ACS Appl. Mater. Interfaces, **10**(28), pp. 24099–24107.
[34] Chung, W.-H., Hwang, H.-J., Lee, S.-H., and Kim, H.-S., 2012, "In situ Monitoring of a Flash Light Sintering Process Using Silver Nano-Ink for Producing Flexible Electronics," Nanotechnology, **24**(3), pp. 035202.
[35] MacNeill, W., Choi, C.-H., Chang, C.-H., and Malhotra, R., 2015, "On the Self-Damping Nature of Densification in Photonic Sintering of Nanoparticles," Sci. Rep., **5**, pp. 14845.
[36] Park, S.-H., and Kim, H.-S., 2014, "Flash Light Sintering of Nickel Nanoparticles for Printed Electronics," Thin Solid Films, **550**, pp. 575–581.
[37] Kim, H.-S., Dhage, S. R., Shim, D.-E., and Hahn, H. T., 2009, "Intense Pulsed Light Sintering of Copper Nanoink for Printed Electronics," Appl. Phys. A, **97**(4), pp. 791.
[38] Hwang, H.-J., Oh, K.-H., and Kim, H.-S., 2016, "All-Photonic Drying and Sintering Process via Flash White Light Combined With Deep-UV and Near-Infrared Irradiation for Highly Conductive Copper Nano-Ink," Sci. Rep., **6**, pp. 19696.
[39] Dharmadasa, R., Dharmadasa, I., and Druffel, T., 2014, "Intense Pulsed Light Sintering of Electrodeposited CdS Thin Films," Adv. Eng. Mater., **16**(11), pp. 1351–1361.
[40] Colorado, H., Dhage, S., and Hahn, H., 2011, "Thermo Chemical Stability of Cadmium Sulfide Nanoparticles Under Intense Pulsed Light Irradiation and High Temperatures," Mater. Sci. Eng. B, **176**(15), pp. 1161–1168.
[41] Dharmadasa, R., Lavery, B., Dharmadasa, I., and Druffel, T., 2014, "Intense Pulsed Light Treatment of Cadmium Telluride Nanoparticle-Based Thin Films," ACS Appl. Mater. Interfaces, **6**(7), pp. 5034–5040.
[42] Hwang, H.-J., and Kim, H.-S., 2015, "Ultra-High Speed Fabrication of TiO_2 Photoanode by Flash Light for Dye-Sensitized Solar Cell," J. Nanosci. Nanotechnol., **15**(7), pp. 5028–5034.
[43] Danaei, R., Varghese, T., Ahmadzadeh, M., McCloy, J., Hollar, C., Sadeq Saleh, M., Park, J., Zhang, Y., and Panat, R., 2018, "Ultrafast Fabrication of Thermoelectric Films by Pulsed Light Sintering of Colloidal Nanoparticles on Flexible and Rigid Substrates," Adv. Eng. Mater. **21**, p. 6.
[44] Inoue, T., Okamoto, H., and Osaki, K., 1992, "Large Deformation of Polycarbonate Near the Glass Transition Temperature," Macromolecules, **25**(25), pp. 7069–7070.
[45] Michael, D., Andrew, P., Zhongwei, G., Gregory, S. H., Chih-hung, C., and Rajiv, M., 2018, "Modeling Nanoscale Temperature Gradients and Conductivity Evolution in Pulsed Light Sintering of Silver Nanowire Networks," Nanotechnology, **29**(50), pp. 505205.
[46] Mutiso, R. M., Sherrott, M. C., Rathmell, A. R., Wiley, B. J., and Winey, K. I., 2013, "Integrating Simulations and Experiments to Predict Sheet Resistance and Optical Transmittance in Nanowire Films for Transparent Conductors," ACS Nano., **7**(9), pp. 7654–7663.
[47] Lambricht, N., Pardoen, T., and Yunus, S., 2013, "Giant Stretchability of Thin Gold Films on Rough Elastomeric Substrates," Acta Mater., **61**(2), pp. 540–547.
[48] Erdem Alaca, B., Saif, M. T. A., and Sehitoglu, H., 2002, "On the Interface Debond at the Edge of a Thin Film on a Thick Substrate," Acta Mater., **50**(5), pp. 1197–1209.
[49] Pritesh, G., Dana, M., Enrico, S., Kalyan Yoti, M., Henrique Leonel, G., Eloi, R., Ammar, A.-H., Olfa, K., and Reinhard, R. B., 2017, "Controlling the Crack Formation in Inkjet-Printed Silver Nanoparticle Thin-Films for High Resolution Patterning Using Intense Pulsed Light Treatment," Nanotechnology, **28**(49), pp. 495301.
[50] Selzer, F., Floresca, C., Kneppe, D., Bormann, L., Sachse, C., Weiß, N., Eychmüller, A., Amassian, A., Müller-Meskamp, L., and Leo, K., 2016, "Electrical Limit of Silver Nanowire Electrodes: Direct Measurement of the Nanowire Junction Resistance," Appl. Phys. Lett., **108**(16), pp. 163302.
[51] Jiu, J., Nogi, M., Sugahara, T., Tokuno, T., Araki, T., Komoda, N., Suganuma, K., Uchida, H., and Shinozaki, K., 2012, "Strongly Adhesive and Flexible

Transparent Silver Nanowire Conductive Films Fabricated With a High-Intensity Pulsed Light Technique," J. Mater. Chem., **22**(44), pp. 23561–23567.
[52] Mallikarjuna, K., Hwang, H.-J., Chung, W.-H., and Kim, H.-S., 2016, "Photonic Welding of Ultra-Long Copper Nanowire Network for Flexible Transparent Electrodes Using White Flash Light Sintering," RSC Adv., **6**(6), pp. 4770–4779.
[53] Jiu, J., Sugahara, T., Nogi, M., Araki, T., Suganuma, K., Uchida, H., and Shinozaki, K., 2013, "High-Intensity Pulse Light Sintering of Silver Nanowire Transparent Films on Polymer Substrates: The Effect of the Thermal Properties of Substrates on the Performance of Silver Films," Nanoscale, **5**(23), pp. 11820–11828.
[54] Yang, L., Gan, Y., Zhang, Y., and Chen, J. K., 2012, "Molecular Dynamics Simulation of Neck Growth in Laser Sintering of Different-Sized Gold Nanoparticles Under Different Heating Rates," Appl. Phys. A, **106**(3), pp. 725–735.