Self-Limited and Forming-Free CBRAM Device With Double Al_2O_3 ALD Layers

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***Abstract*— Self-limited and forming-free Cu-based CBRAM devices with a double Al_2O_3 atomic layer deposition layer (D-ALD) structure were developed. The proposed structure offers desirable properties such as forming free ($V_{forming} = V_{SET}$), self-limited resistive switching with very low programming current (~10 nA), high ON/OFF ratio (>100), and nonlinear *I–V* (NL_{read} and NL_{SET} ~ 10) at low resistance state. The outstanding performance of D-ALD devices was due to the HT-ALD layer that operates as both a diffusion barrier preventing over injection of Cu ions and a tunneling barrier enabling self-limited programming.**

***Index Terms*— CBRAM, RRAM, low-current, nonlinearity, forming-free, self-limited, uniformity.**

I. Introduction

CONDUCTIVE-BRIDGE random access memory (CBRAM) has been considered as a promising candidate for next generation non-volatile memory, as well as in-memory computing applications due to its properties such as fast speed, low power consumption, high on/off ratio, and high density ($4F^2$) [1]–[3]. On the other hand, extensive device optimizations still need to be performed to support large-scale implementations [4]–[7]. First, forming-free cells are desired for crossbar operations since high forming voltages could damage cells already formed in the array [8], [9]. In addition, self-limited programming is necessary to ensure cell reliability, since external current compliance (CC) will not be effective in passive crossbar arrays [10], [11]. Low programming current helps mitigate the series resistance issue and reduces the operation power [12], while nonlinear I-V characteristics in low resistance state (LRS) helps mitigate sneak currents [13], [14].

In this study, a Cu-based CBRAM device with a double Al_2O_3 atomic layer deposition (D-ALD) layer structure, consisting of a low-temperature (LT) Al_2O_3 ALD switching layer and a high-temperature (HT) Al_2O_3 ALD barrier layer, was developed. The proposed D-ALD devices achieved ultra-low self-limited programming current (<100nA), forming-free switching ($V_{forming} = V_{SET}$), large on/off ratio (~100), reliable switching cycle (>1000 cycles), I-V nonlinearity (NL_{read} and NL_{SET} ~ 10), and good cycle-to-cycle (C-to-C) and device-to-device (D-to-D) uniformity, using CMOS compatible processes.

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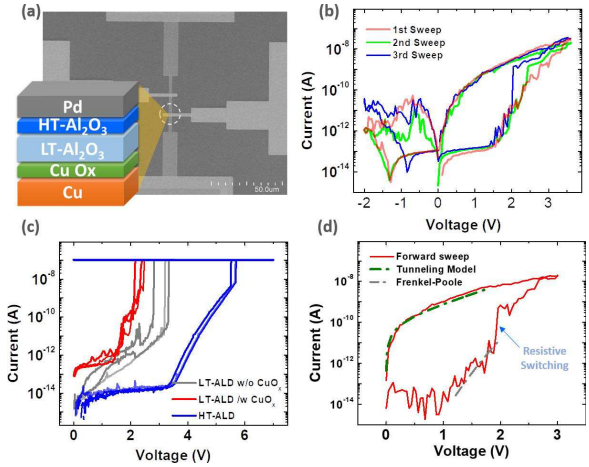

Fig. 1. (a) SEM image of Cu/CuOx/LT-ALD/HT-ALD/Pd crossbar devices. Inset: the schematic structure of D-ALD devices. (b) Successive I-V sweeps including the forming process of as-fabricated device (red) (c) I-V curves of LT-ALD devices without CuOx ($V_{forming}$ ~ 3V), LT-ALD devices with CuOx ($V_{forming}$ ~ 2V), and HT-ALD devices ($V_{forming}$ ~ 5.5V). Results from three devices are shown for each structure. (d) Fitting of the D-ALD device I-V. The fitting was limited to below 2.0V where resistive switching occurred.

II. Experiments

The Cu/CuO_x/LT-ALD/HT-ALD/Pd cells were fabricated in a $2\mu m \times 2\mu m$ two-terminal crossbar structure as shown in Fig. 1(a). The bottom electrode (BE) was defined on top of a SiO_2/Si substrate by photolithography, followed by e-beam evaporation of 5nm/50nm of NiCr/Cu. The Cu BE was then subjected to O_2 plasma treatment for 2 minutes at 150°C to form a copper oxide layer. 40 cycles (~45Å) of Al_2O_3 LT-ALD switching layer was then deposited in an Oxford ALD tool at 110°C using H_2O recipe, using $Al(CH_3)_3$ and H_2O as metal precursor and oxidizing agent, respectively. The ALD tool was then heated up to 250°C, and 6 cycles (~7Å) of Al_2O_3 HT-ALD layer was deposited with plasma recipe using O_2 plasma as oxidizing agent. The Pd top electrode (TE) was formed by e-beam evaporation. The devices were measured by a Keithley 4200 semiconductor parameter analyzer. All switching characteristics were obtained without external CC.

III. Results and Discussions

In Fig. 1(a), D-ALD device with Cu/CuO_x/LT-ALD/HT-ALD/Pd structure is illustrated. The CuO_x layer was found to improve nucleation during growth of the LT-ALD switching layer. Additionally, the Cu ions in the CuO_x layer facilitates the redox processes involved in conducting filament (CF) formation and thus reduces $V_{forming}$ [15], [16]. The thin HT-ALD layer is used as a barrier layer to limit CF growth and reduce the programming current. X-ray reflectance measurements (XRR) show the HT-ALD film has higher

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density (3.7g/cm^3) than the LT-ALD film (3.3g/cm^3). Resistive switching in HT-ALD was found to be more difficult than in LT-ALD, possibly because of the denser film makes it harder for the inclusion of water molecules to mediate Cu redox processes [17]. As a result, the HT-ALD film can act as a good Cu diffusion barrier layer.

Fig. 1(b) shows three consecutive resistive switching curves without CC, starting from the as-fabricated state, with voltage applied on the Cu BE and the TE grounded. Note the non-zero crossing during the negative sweep was caused by a small (∼0.15pA) offset current, likely due to discharging from parasitic capacitances as the voltage is decreased. Smooth I-V curves and zero-crossing can be obtained by removing this small current offset. The first I-V sweep from the as-fabricated device leads to a switching to LRS at ∼2V. This $V_{forming}$ is the same as the switching voltage in subsequent sweeps, showing forming-free characteristics. The self-limited programming process can be observed from the reliable switching curves - the switching does not lead to uncontrollable ramp up of the current, even without any external CC or added series-resistance to limit the applied voltage. Compared with previous studies on Al_2O_3-based CBRAM that require high $V_{forming} \sim 2.3 \times V_{SET}$ and external CC [6], the forming-free and self-limited programming of D-ALD devices allow more reliable device operation and transistor-free 1S1R crossbar implementations, where low-forming voltage is necessary and external current compliance will be difficult to apply. The I-V curves obtained from the resistive switching cycles are similar to each other, with consistent LRS and high-resistance state (HRS) values, showing good C-to-C uniformity without elaborate control circuitry. I-V nonlinearity NL_{read} and NL_{SET} of ∼10 (defined as $NL_{read} = I(V_{read})/I(1/2V_{read})$ at $V_{read} = 1.0V$ and $NL_{SET} = I(V_{SET})/ I(1/2V_{SET})$ at $V_{SET} = 3.0V$) are also observed in the I-V curve in LRS. Due to the very low read current (0.1 nA) and the high on-state device resistance (> 1GΩ), the ground scheme can be successfully applied to arrays during read, while the nonlinearity NL_{SET} becomes attractive during write to help reduce the power consumption using the V/2 write scheme during array operation [13], [14].

The desirable performance can be attributed to the role of the layers, CuO_x, LT-ALD, and HT-ALD in the device. Fig. 1(c) shows forward I-V sweeps obtained from three as-fabricated control devices with different structures until their breakdown. Cu(TE)/LT-ALD(50 cycles)/Pd (BE) devices without CuO_x was used to investigate the role of the CuO_x layer. It showed not only higher $V_{forming} \sim 3V$, but also large D-to-D variations (gray curves) and low yield (5 out of 10 devices were initially shorted). This result can be attributed to poor nucleation of the LT-ALD layer on top of the copper BE that leads to high density of defects such as pin-holes and rough surface [18]. To address this issue, we note copper oxide has been used to improve nucleation of the Al_2O_3 layer during ALD growth since hydroxyl (OH) groups can be chemisorbed onto the CuO sites and react with the organometallic precursors during ALD [19]–[21]. Hence, Cu(BE)/CuO_x/LT-ALD(50 cycles)/Pd (TE) devices with the LT-ALD layer grown on top of CuO_x were fabricated. The formation of CuO_x was conducted by 2 minutes of exposure to O_2 plasma. The LT-ALD devices grown on CuO_x layer show a low $V_{forming}$ close to 2.0V (red curves) with enhanced uniformity and high yield (all the pristine devices are initially insulating). Moreover, copper ions (Cu^{2+}) can be more easily supplied from CuO_x and diffuse into the Al_2O_3 layer compared to the Cu metal case, due to the lower Cu-O bond energy in CuO (∼1.5eV) compared with that of Cu-Cu metallic bond (∼2.0eV) [16], [21]–[23]. Therefore, devices with CuO_x as the ion source layer exhibit reduced $V_{forming}$. The low forming voltage of LT-ALD can also be attributed by the effects of H_2O molecules in the LT-Al_2O_3 film, which has been shown to be more hydrophilic than SiO_2 [24]. The H_2O molecules absorbed in the LT-ALD layer can facilitate the Cu redox processes, as has been observed in SiO_2-based devices [15].

The HT-ALD control devices were fabricated in the same structure as the LT-ALD device, i.e. Cu(BE)/CuO_x/HT-ALD(50cycles)/Pd(TE), by simply replacing the ALD growth condition from 110°C with H_2O in the LT-ALD device to 250°C with O_2 plasma in the HT-ALD device. Since the same number of ALD cycles (50 cycles) for both the HT-ALD device and the LT-ALD device were used, resulting in similar thickness of ∼55 Å, the difference of I-V the characteristics between LT-ALD devices and HT-ALD devices are mainly due to the ALD film quality. The I-V curves of HT-ALD devices (blue lines) in Fig.1(c) showed very low leakage current (∼10^{-14}A) and eventually broke down at a high voltage, ∼5.5V. These results verify that the HT-ALD layer can offer very low leakage current and support high electric field. The closely packed Al_2O_3 in HT-ALD films makes it harder to hold water molecules, which have been shown to reduce the activation energy of copper ion migration [17]. These results suggest that HT-ALD can be used as an effective ion diffusion barrier to control the growth of the CF. The excellent insulating quality of the HT-ALD layer is also useful to limit the current and achieve self-compliance during the switching process, as have been verified in the D-ALD devices shown in Fig. 1(b).

The conduction mechanism can be further explained by fitting the I-V curves, as shown in Fig. 1(d). The I-V curve in HRS was fitted to Frenkel-Poole model in the 1.2∼2.0V range (where the current is clearly above the measurement resolution limit), which implies trap-related leakage mechanism in HRS, as shown in Fig.1(d) [25]. The LRS regime can be fitted with direct tunneling, implying the existence of a barrier between the CF and the inert electrode [26]. From the fitting, the tunneling gap and diameter of the CF is estimated to be 10Å and 16 Å, respectively. The tunneling gap of 10Å is close to the thickness of the HT-ALD barrier, ∼7 Å.

This analysis supports the hypothesis that the vertical growth of the Cu CF is stopped by the HT-ALD layer, and conduction in the LRS is dominated by tunneling through the barrier layer.

Additional evidence of reliability of the HT-ALD barrier can be observed in Fig. 2(a). Here the applied voltage was continuously applied beyond the typical programming voltage range of 3V. At ∼4V, Cu ion injection into the HT-ALD barrier layer occurs, leading to abruptly increased current. However, the device recovers the lower LRS current level at ∼1.6V during reverse sweep without suffering from permanent damage, suggesting the partial filament in the HT-ALD layer is not stable and the HT-ALD film can restore its barrier property even if the device is accidentally exposed to high voltage. The instability of the Cu filament in the HT-ALD layer can be understood from the enhanced mechanical stress due to

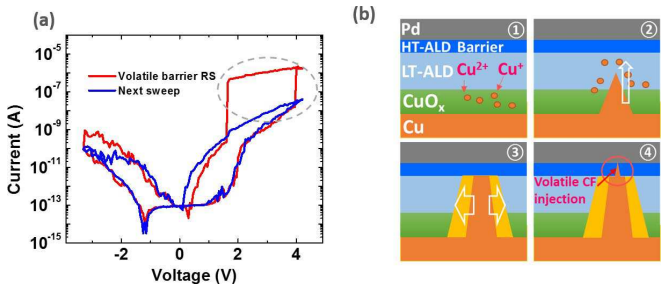

Fig. 2. (a) An I-V sweep with larger voltage range showing over-programming (red) and the subsequent restoration to the original resistive switching curve (blue) (b) Schematic illustration of the switching mechanism of D-ALD device.

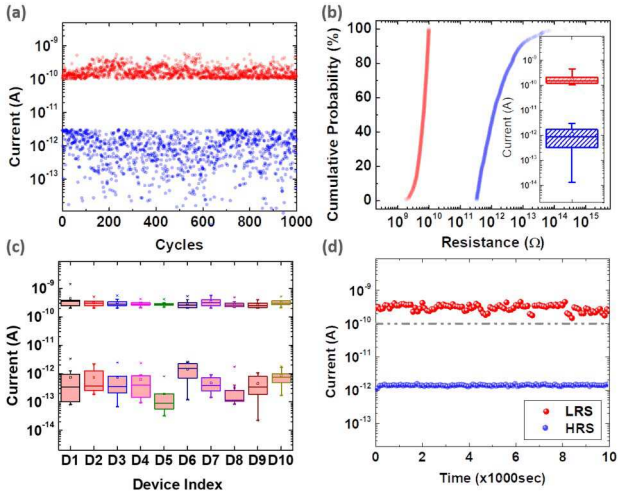

Fig. 3. (a) Pulse cycling test (3.0V/5ms for SET pulse, −2.5V/5ms for RST pulse, and 1.0V for read pulse) (b) Cumulative probability of resistance in LRS and HRS. Inset: box plot showing C-to-C variation. (c) Box plots of on/off current from 10 devices (d) retention test of LRS and HRS at T = 100°C.

the high Young's modulus in the HT-ALD layer [27]–[29]. Enhanced mechanical stress reduces the activation energy for Cu cluster dissolution and makes the CF volatile in the HT-ALD layer.

The resistive switching mechanism of the D-ALD device is illustrated in Fig. 2(b). (1) In the as-fabricated device, Cu ions can be supplied from the CuO_x layer and migrate into the LT-ALD layer leading to resistive switching with forming-free behavior (2). The growth of the Cu CF in the LT-ALD layer increases the current level from $\sim 10^{-12}$A to $\sim 10^{-9}$A. The vertical growth is stopped by the HT-ALD layer. (3) Afterwards, lateral CF growth results in gradual increase in device current when the voltage is continuously applied. (4) If the device is accidentally subjected to high voltage, Cu ions may be injected into the HT-ALD layer. However, the injected Cu will not be stable and the HT-ALD layer can recover its barrier property.

Fig. 3(a) shows the cycling test results. The D-ALD device achieved 1000 cycles of resistive switching without any observable degradation of on/off ratio (∼100). The C-to-C cumulative distribution in Fig. 3(b) shows uniform on-current in the 100∼300pA range (at 1V), without any help of CC. D-to-D uniformity was examined in Fig. 3(c). Box plots measured from 10 different devices show similar distribution in current levels in both LRS and HRS for all devices. The improved uniformity of the devices can be attributed

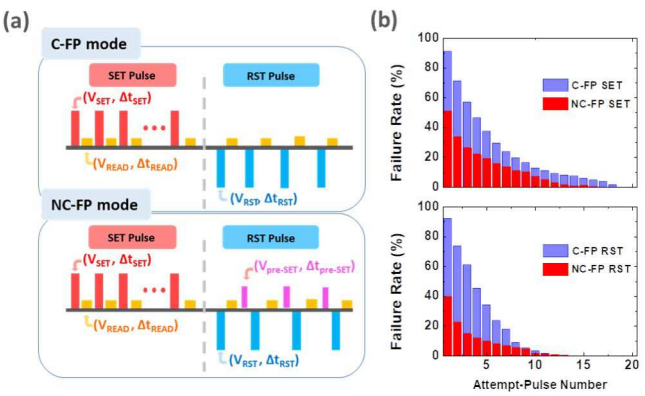

Fig. 4. (a) Schematic pulse sequence consisting of SET pulse train and RST pulse train with verification scheme, for the cumulative fixed pulse mode (C-FP) and the non-cumulative fixed pulse mode (NC-FP). (b) Switching probability of SET (upper) and RESET (lower) for attempts using C-FP (purple) and NC-FP (red). The conditions of SET, RST, pre-SET pulses are fixed at 3.0V/5ms, −2.5V/5ms, and 2.0V/5ms, respectively.

to the uniformity of the deposited ALD layers, including both the LT-ALD switching layer and the HT-ALD barrier layer. In addition, retention over 10^4 seconds was obtained at 100°C (Fig.3(d)).

Finally, we examined the effects of the pulse programing algorithms on device operation. The standard pulse programming method is the cumulative fixed pulse (C-FP) mode, a commonly-used write-verification method, consisting of 3.0V/5ms SET pulses followed by 1.0V read pulses for verification during SET, and −2.5V/5ms RESET (RST) pulses and subsequent read pulses during RESET (top panel of Fig.4(a)). To optimize device operation, the RESET sequence was changed following [30]. When the device was not erased after an RST pulse, a positive voltage pulse (pre-SET pulse) (2.0V/5ms) was applied prior to the subsequent RST pulse (bottom panel of Fig.4(a)). This programming method is called non-cumulative fixed pulse (NC-FP) mode [30]. Compared with C-FP mode, the application of the NC-FP mode lowered the switching failure rate, defined as the probability of resistive switching not being successful after a sequence of attempt SET or RST pulses, as shown in Fig.4(b) and improved the endurance from ∼200 to >1000. It is believed that the pre-SET pulses help the Cu atoms escape from the metastable locations that may favor forward migration vs. backward migration. The reduction of the gap size due to the pre-SET pulse also increases the field during the subsequent RESET pulse and facilitates the subsequent removal of the Cu atoms. This approach additionally improves SET reliability, likely due to reduction of residual Cu ions in the LT-ALD layer and the reduced stress from the reduced number of RST attempts.

IV. Conclusions

Cu-based CBRAM devices with double Al_2O_3 ALD layers have been developed. The D-ALD devices achieved self-limited current, forming free, high on/off ratio, good uniformity, nonlinear I-V at LRS, and robust pulse switching. The roles of CuO_x and HT-ALD layers were investigated. The promising results from the D-ALD devices help advance of the CBRAM crossbar arrays for storage and novel computing applications.

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