

An Efficient Complementary Topology Switched-Capacitor Based DC-DC Converter

Ruikuan Lu, Mohammad R Haider
Dept. Electrical and Computer Engg.
University of Alabama at Birmingham
Birmingham, AL, USA
{lukuan, mrhaider}@uab.edu

Yehia Massoud
School of Systems and Enterprises
Stevens Institute of Technology
Hoboken, NJ, USA
ymassoud@stevens.edu

Nasim Uddin
Dept. of Civil Engineering
University of Alabama at Birmingham
Birmingham, AL, USA
nuddin@uab.edu

Abstract—This paper proposes a complementary topology for Switched-Capacitor (SC) DC-DC converter to enhance the dynamic response. For battery charging unit with faster charging time requirement, one of the major restrictions comes from the equivalent output resistance of the SC DC-DC converter. By connecting one completely symmetric SC converter as complementary topology with the original single converter, the proposed SC DC-DC converter topology decreases the equivalent output resistance down to half. Simulated in 0.13- μm standard CMOS process, the simulation results show that this complementary SC converter gains faster dynamic response, shorter charging time, and higher energy-conversion efficiency.

Index Terms—switched-capacitor, DC-DC converter, complementary topology, dynamic response, complementary topology

I. INTRODUCTION

Proliferation of wireless sensors and sensor network has enabled widespread deployment of multi-sensors and power management units for industrial, civil, military, medical and Internet-of-Things (IoT) applications [1] - [6]. In the field of portable battery charging unit and high-quality MOS monolithic integrated power converter circuit design, the switched-capacitor (SC) circuit technology is being widely used because of its low-cost, high conversion efficiency, and low-power consumption shown in Fig. 1. The widespread applications of SC DC-DC converters are ranging from high power applications such as electric and hybrid vehicles to low power applications in dynamic random access memory (DRAM) circuits, electrically-erasable programmable read-only memory (EEPROM) circuits, and phase-locked loop (PLL) circuits. Conventional switching mode power supply circuits (SMPS) use inductor composed of an electromagnetic coil in order to process the energy and stabilize the output voltage [7].

The conventional LRC DC-DC boost converter circuit contains a DC power supply, an inductor, a diode, a capacitor, a load resistor, a MOSFET as a switch and the square wave control signal. However, most of the low-power, small-volume mobile devices need to integrate the power supply onto a CMOS integrated circuit. Furthermore, the off-chip inductor is not suitable for integration on a single chip because of its large size and its strong nonlinear characteristics. The SC DC-DC converter is one subset of the power DC-DC converter, which is only consisted of switches and capacitors. Because of there

is no inductive component in an SC DC-DC converter, it is extremely suitable for integration on a single chip.

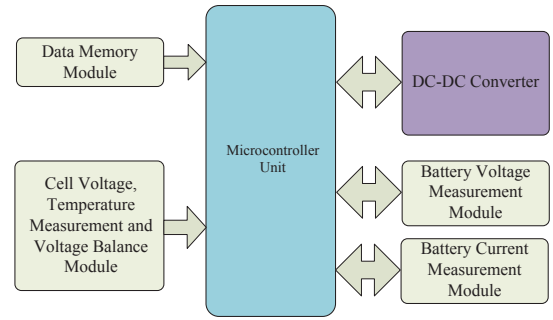


Fig. 1. Schematic diagram of a battery management system where DC-DC converter plays an integral role.

In this paper, a complementary topology for SC DC-DC converter is proposed. This complementary topology uses an extra completely symmetric converter to connect with the original single converter together. By this way, the complementary SC DC-DC converter could decrease the equivalent output resistance and increase its dynamic response. Furthermore, the proposed complementary SC DC-DC converter is adapted to other converter topologies with different types and conversion ratios.

The organization of the paper is as follows. The overview of the SC DC-DC converter is discussed in section II, while the optimized complementary SC converter topology is demonstrated in section III. The simulation results of converter output voltage as well as power conversion efficiency, and conclusion are discussed in section IV and section V separately.

II. OVERVIEW OF THE SC DC-DC CONVERTER

An SC DC-DC converter can implement one or several different topologies, where the converter can achieve multi-ratio purpose. Each topology corresponds to a particular configuration of switches and capacitors. By changing the control signal's timing sequence of the different groups of switches, the capacitors will be into charging state and discharging state alternately. As a result, the converter could be configured in different topologies [7].

A single 3:1 ladder converter topology example is shown in Fig. 2. As we known, the capacitors C4 and C5 are defined as flying capacitors and C1, C2 and C3 are defined as output or bypass capacitors. The conversion ratio is 3:1 which means the output voltage is one-third of the V_{dd} voltage, where the V_{dd} is the DC input voltage and the V_{out} is the DC output voltage.

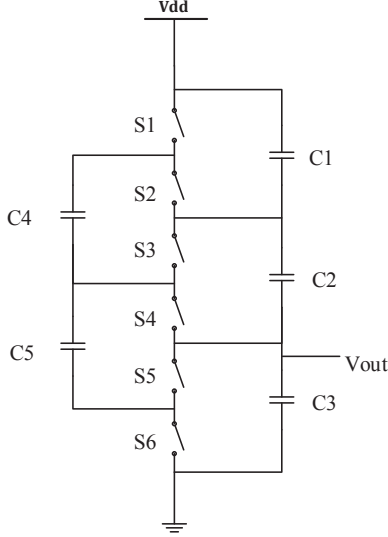


Fig. 2. Diagram of single 3:1 ladder converter.

In this example, the converter is working under two non-overlapped square wave clock signals. The odd number switches are turned off during phase 1 and the even number switches are turned on at this phase. And during phase 2, the odd number switches are turned on and the even number switches are turned off simultaneously. Under different switching phases, the capacitors are in charging and discharging state alternately. And for the load capacitor C3, it will into steady state until it is fully charged. At the steady state, the output voltage of C3 is one-third of V_{dd} voltage. The converter working in different phases are shown in Fig. 3 (a) and (b).

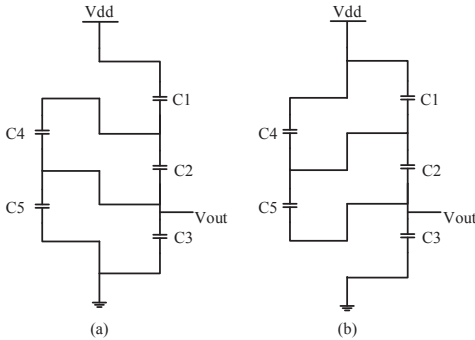


Fig. 3. Single 3:1 ladder converter works under phase 1 (a) and phase 2 (b).

The critical restriction for the SC DC-DC converter is the equivalent output resistance. To transfer charges between

input and output of converter, the capacitors will be charged and discharged alternately. The voltage drop is proportional to output current, which could be represented as equivalent output resistant. The idealized transformer equivalent circuit is shown in Fig. 4.

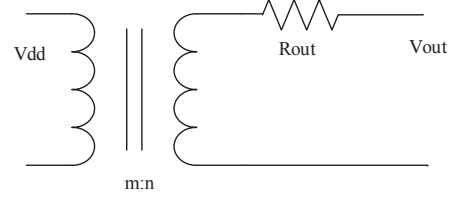


Fig. 4. Idealized transformer equivalent circuit of SC DC-DC converter.

The converter ratio M is,

$$M = \frac{m}{n} = \frac{V_{dd}}{V_{out}} \quad (1)$$

where M is the DC-DC power converter ratio, m and n represent from primary side to secondary side. Furthermore, V_{dd} is the input side DC voltage and V_{out} is the output side DC voltage separately. The equivalent output resistant R_{out} can be represented as,

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \quad (2)$$

where R_{SSL} is the slow switching limit (SSL) impedance and R_{FSL} is the fast switching limit (FSL) impedance [8]. The R_{SSL} value is only depending on converter topology, capacitor value and switching frequency. Additionally, for the SSL impedance, the finite resistance of switches, capacitors and interconnect are neglected. And the FSL impedance is characterized by constant current flow between capacitors. The switches' turn-on impedance and other resistances are sufficiently large that cannot be neglected. So this R_{FSL} value is not only depending on converter topology, capacitor value and switching frequency, but also on switches' turn-on resistance, capacitors' equivalent series resistance.

III. PROPOSED COMPLEMENTARY SC DC-DC CONVERTER

As the equivalent transformer circuit shown in Fig. 4, the SC DC-DC converter is suitable for no load and capacitive load connection. In order to decrease the equivalent output resistance and to increase its dynamic response, we propose a new complementary SC DC-DC converter topology which contains a pair of completely symmetrical SC DC-DC converters forming the complementary structure. The circuit diagram is shown in Fig. 5(a).

This complementary SC DC-DC converter is also working under two non-overlapped square wave clock signals. During phase 1, the odd number switches of original single ladder converter (S1, S3, S5) and the even number switches of the symmetric ladder converter (S2', S4', S6') are turned on while the other switches are turned off as shown in Fig. 5(b).

In the same way, during phase 2, the even number switches of original ladder converter (S2, S4, S6) and the odd number

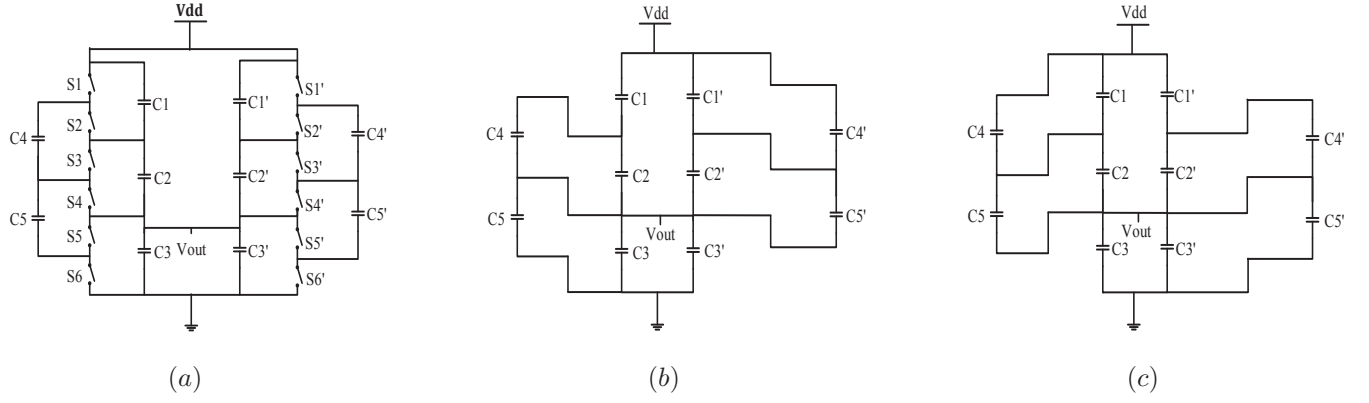


Fig. 5. Proposed Complimentary SC DC-DC Converter. (a) Complementary 3:1 SC DC-DC ladder converter topology. (b) Diagram of complementary converter under phase 1. (c) Diagram of complementary converter under phase 2.

switches of the symmetric ladder converter ($S1'$, $S3'$, $S5'$) are turned on. The other switches are turned off as shown in Fig. 5(c). Unlike the single converter, the load capacitors or bypass capacitors are consisted of two parallel capacitors $C3$ and $C3'$. During different phases, one load capacitor is discharging but the other symmetric one is charging. In generally, no matter in which phase, there is always one load capacitor in charging state. The original converter and the symmetric converter are as complement for each other converter to charging the load capacitor while one converter is in discharging phase. In this two phases topology, as constriction, there can be only one symmetrical structure to form this complementary topology with the original converter.

Under this complementary topology, the equivalent output impedance is decreased, which means this complementary converter enhance the load capacity and dynamic performance. When this complementary converter connects with a capacitive load, the time constant will down to half of the original converter. By adding one symmetric converter, the complementary SC DC-DC converter could decrease the equivalent output resistance down to half of the single converter and increase the dynamic response performance.

IV. SIMULATION RESULTS

Cadence simulations are performed to access the SC DC-DC converter integrated on single chip. The proposed scheme is designed using 0.13- μm standard CMOS process. The Vdd is using 1 V DC power supply and the two non-overlapped square wave clock signals' frequency are 200 MHz and the load capacitor is 1 nF. The simulation results of the output voltage between the single ladder converter and the complementary ladder converter are shown in Fig. 6.

From the simulation results, the steady state output voltage of the single converter is 327 mV and the rise time is 138 ns. Furthermore, the steady state output voltage of the complementary converter is 328 mV and the rise time is 60.1 ns. The complementary converter decreases the time constant down to half of the single converter. The rise time of the complementary converter is 43.6% of the single converter.

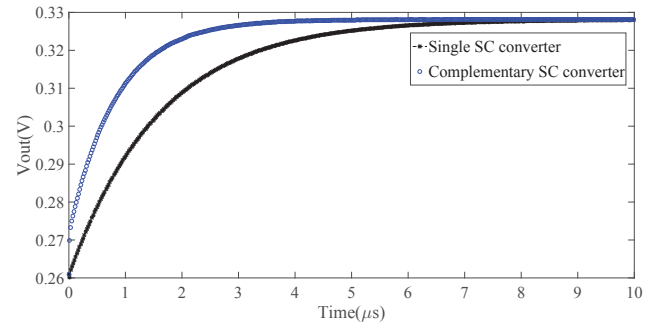


Fig. 6. Output voltage comparison of single SC converter and complementary SC converter under 1 nF capacitor load

Under a resistive load R_{load} of 10 K Ω , input voltage of 1 Volt, and switching frequency of 200 MHz, the simulated output voltages of the single converter and the complementary converter are shown in Fig. 7. From the simulation results, the DC output voltage of the single converter is 248.0 mV and the ripple voltage is 21.7 mV. Comparatively, the DC output voltage of the complementary converter is 281.5 mV and the ripple voltage is 14.4 mV. The SC converter with complementary topology improve the steady-state output voltage and decrease the DC voltage ripple. Moreover, under different resistor ratio R_{out}/R_{load} , the steady-state DC output voltage comparison

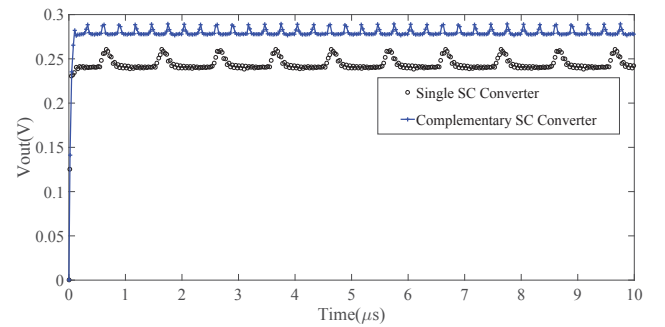


Fig. 7. Output voltage comparison of single SC converter and complementary SC converter under 10 K Ω resistor load

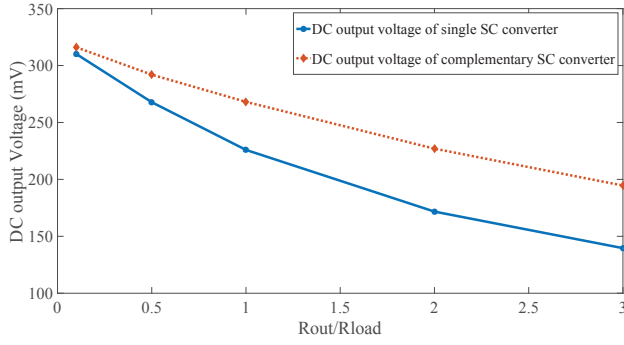


Fig. 8. DC output voltage comparison between single SC converter and complementary SC converter

between the single SC converter and the complementary SC converter is shown in Fig. 8. The ripple output voltage comparison between the single SC converter and the complementary SC converter is shown in Fig. 9.

The simulation results show that the SC converter with complementary topology improve the steady-state output voltage and decrease the DC voltage ripple. Furthermore, as the SC DC-DC converter power efficiency η can be represented from the transformer model shown in Fig. 4,

$$\eta = \frac{V_{out}I_{out}}{V_{dd}I_{dd}} = \frac{1}{1 + \frac{R_{out}}{R_{load}}} \quad (3)$$

The power efficiency comparison result between single converter and complementary converter under some value of load resistor is shown in Fig. 10.

Under capacitive load, the proposed complementary converter topology can improve the dynamic response in rise time and time constant. Furthermore, under same resistive load, since equivalent output resistance of complementary converter topology is only half of single converter's, the complementary SC DC-DC converter has higher steady-state output voltage, lower DC ripple and high-power conversion efficiency.

V. CONCLUSION

This paper has introduced a complementary converter topology for on-chip SC DC-DC converter circuit design. The complementary SC DC-DC converter technique distinctly decreases converters equivalent output resistance. Therefore, the

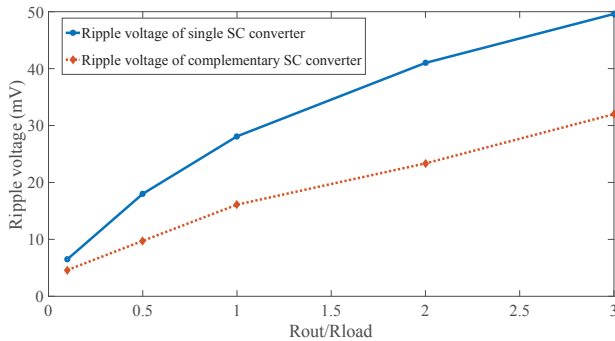


Fig. 9. Ripple output voltage comparison between single SC converter and complementary SC converter

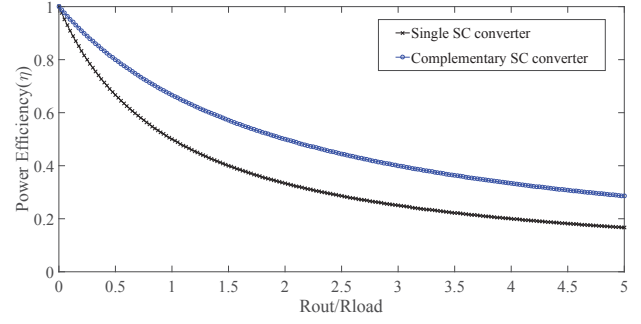


Fig. 10. Power efficiency comparison between single SC converter and complementary SC converter.

complementary converter topology can effectively decrease the charging time under capacitive load and enhance the power conversion efficiency from one DC voltage level to another DC voltage level under resistive load. With the increasing demand for miniaturization, high power conversion efficiency, and low-cost power management systems, the switched-capacitor DC-DC converter has gained developing momentum. This proposed complementary SC DC-DC converter topology can be applied in wireless power transfer, fast charging in electric vehicle, high efficiency battery management system, PLL circuit and oscillator neural network circuits.

ACKNOWLEDGMENT

This work was supported by the NSF-CPS (Cyber-Physical Systems) program with award number CNS-1645863.

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