A High-gain Large-scanning 60 GHz Via-fed Patch Phased Array Antenna

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***Abstract*—This paper presents a 7×7 via-fed patch phased array antenna for next-generation communication systems. The low-profile antenna array is fabricated on a printed circuited board (PCB) resulting in a low-cost approach. While the via-fed design enables testing of the antenna component in a laboratory environment, it also provides a path for direct integration on a transceiver chip. The designed finite array is well matched at 60 GHz with the bandwidth covering 57 GHz to 64 GHz. The maximum realized gain for the 7×7 array is 22.15 dBi with the gain reduction of $\leq$4 dB under the condition of the maximum scanning angle. Moreover, the scanning volume of the designed antenna is $\pm 55°$ in *H* plane and $\pm 53°$ in *E* plane without using any superstrate. As a single-layer patch array, the designed array satisfies high gain and large scanning volume in both *E* and *H* planes.**

Keywords—60 GHz band, Phased array antenna, Millimeter-wave, Large scanning

I. INTRODUCTION

Millimeter-wave antenna arrays have recently attracted increased attention due to continuous demand growth for high data rate transmission [1]. As the cellular data traffic increases, the future wireless communication systems are expected to operate with higher bandwidth. The 60 GHz band has emerged as one of the candidates for next-generation communication systems because of available 7 GHz of unlicensed band (57-64 GHz). However, due to large path loss at 60 GHz, high-gain and steerable antenna arrays are required to guarantee short-range communication. Moreover, the antenna arrays need to be low-cost and easily integrated with silicon transceivers [2-3].

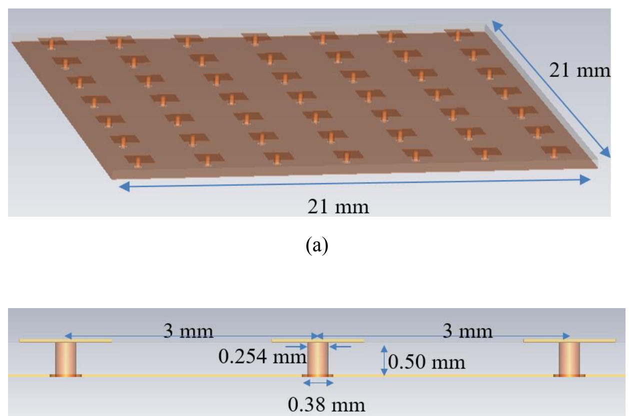
Compared to other antennas, patch antennas have the advantages of being low-cost, low-profile and light-weight, and are commonly used for satellite and defense applications. For instance, a 60 GHz phased array was designed to achieve the high gain and wide bandwidth [4]. In another work [5], the artificial magnetic conductor was employed, but it needed large volume to improve the gain. In addition, an air cavity substrate was adopted to increase the bandwidth [6], however, the structure was complex and costly.

To achieve high gain, easy fabrication, and low cost, a 7×7 patch antenna array is proposed in this paper. The simulation is performed using time-domain CST Design Studio. Via feeding is used for ease of testing and integration with current PCB fabrication techniques. In Section II, the antenna geometry and substrate properties are discussed. The scanning range in both *E* and *H* planes are analyzed in Section III. Finally, the impedance bandwidth is presented.

II. ANTENNA DESIGN

A. Antenna Geometry

The 7×7 finite array model is shown in Fig. 1. Given the wavelength size ($\lambda = 5$ mm at 60 GHz) and fabrication limitations, the element spacing is increased from 0.5 λ to 0.6 λ, consequently, the array size is $21\ mm \times 21\ mm$.



(b)

Fig. 1. (a) 3D Schematic model of the 7×7 array and (b) cross-section with detailed geometry showing the via-fed design.

Due to its acceptable performance at millimeter-wave band, RO3003 is chosen ($\epsilon_r = 3$, $tan\delta = 0.0013$ at 10 GHz) as substrate material. To increase the scanning range, the substrate height is chosen to be 0.5 mm ($\lambda/10$). In addition, standard 254 μm (10 mil) via holes are fabricated on the RO3003 board (shown in Fig.1 (a)).

For unit cell elements, the size is 3 mm $\times$ 3 mm (shown in Fig.1 (b)). By taking the mutual coupling and impedance matching into account, the length and width of the patch is optimized as 1.11 mm and 1.22 mm, respectively. Furthermore, the inset position of feeding via is designed as 0.30 mm.

B. Phased Array design

Obviously, broadside scanning requires all radiating elements in the same phase (shown in Fig.2). For active scanning, once the scanning plane is identified, the radiating rows are excited with progressive phase difference. For instance,

Fig.3 presents the electric field pattern under condition of active scanning (*E* plane and 30° from broadside).

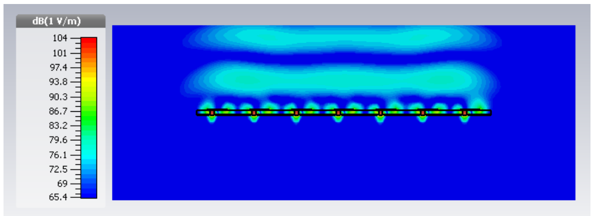


Fig.2. The electric field of active scanning (broadside).

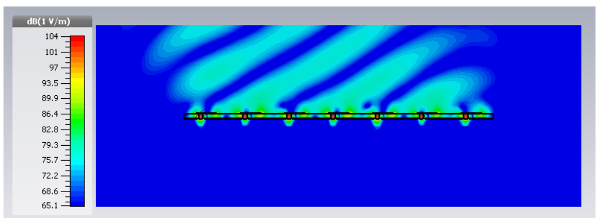


Fig.3. The electric field of active scanning (*E* plane and 30° from broadside).

III. Results

Fig.4 and 5 present the realized gain at *E* plane and *H* plane, respectively. It is observed that this antenna array is capable of ±55° scanning in *H* plane and ±53° scanning in *E* plane. For the maximum angle, the realized gain is 19 dBi, i.e., the gain reduction is less than 4 dB considering all scanning angles.

The magnitude of S_{11} is plotted in Fig.6, showing that the designed antenna array is well matched at 60 GHz. It is important to note that the bandwidth is sufficient for 60 GHz applications.

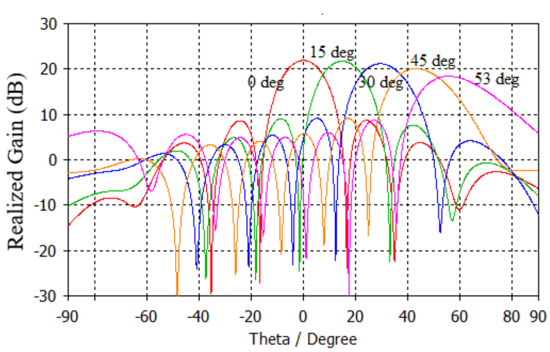


Fig.4. Realized gain at *E* plane showing that the maximum angle is 53°.

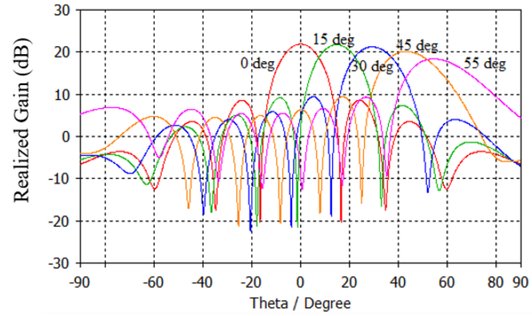


Fig.5. Realized gain at *H* plane showing that the maximum angle is 55°.

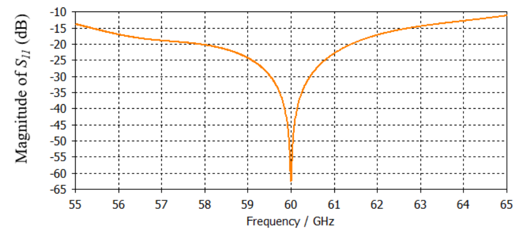


Fig.6. Magnitude of S_{11} showing that the designed array is matched at 60 GHz.

IV. Conclusion

In this paper we presented a novel design of a 7×7 patch array at 60 GHz using PCB process. The designed 7×7 antenna array is capable of scanning ±53° in *E* plane and ±55° in *H* plane without using any superstrate. The broadside gain is 22.15 dBi with the gain reduction ≤4 dB in the case of all scanning angles. Moreover, the -10 dB impedance bandwidth covers the 57 GHz to 64 GHz unlicensed band. Therefore, as a single-layer patch array, the designed antenna array achieves high gain and large scanning volume in both *E* and *H* plane with low profile. Design, fabrication, and testing results of the array will be presented at the meeting.

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