# 15.7 An 8.3MHz GaN Power Converter Using Markov Continuous RSSM for 35dBμV Conducted EMI Attenuation and One-Cycle $T_{ON}$ Rebalancing for 27.6dB $V_0$ Jittering Suppression

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GaN power switches have gained fast-growing popularity in power electronics. With a similar $R_{DS\_ON}$ resistance, they boast 2-to-3-order lower gate capacitance than silicon counterparts, making them highly desirable in high-frequency ($f_{SW}$), high-performance power converters. However, at high $f_{SW}$, switching transitions have to be completed in much shorter times, creating much larger *di/dt* and *dv/dt* changes in power stage, which directly link to electromagnetic-interference (EMI) emissions [1]. To suppress EMI, spread-spectrum-modulation (SSM) techniques [2-5] have been proposed. As depicted in Fig. 15.7.1, a periodic SSM (PSSM) is straightforward and easy to implement. However, its EMI suppression is not effective [2]. A randomized SSM (RSSM) can outperform the PSSM, with lower peak EMI and near-uniform noise spreading, but its performance highly relies on the random clock design. In [3], an N-bit digital random clock was reported to achieve a discrete RSSM (D-RSSM). However, the bit number N has to be large in order to achieve satisfying EMI attenuation, significantly increasing circuit complexity, chip area, and power consumption. To overcome this, a thermal-noise-based random clock was proposed [4]. Unfortunately, thermal noise is very sensitive to temperature and is hard to predict. To apply this approach to a practical implementation requires additional signal processing with periodic signals to confine its range of randomization, which, in turn, reduces the benefits of the RSSM. To achieve a near ideal RSSM, a continuous RSSM (C-RSSM) with a cost-effective implementation is highly preferable. Meanwhile, another challenge of applying SSM schemes lies in the fact that the schemes deteriorate $V_0$ voltage regulation. As shown in Fig. 15.7.1, as an SSM scheme continuously or periodically modulates $f_{SW}$, a converter switching period fluctuates cycle by cycle, causing random errors on the duty ratio and thus jittering effect on $V_0$. This is difficult to correct by a feedback control loop, as the duty-ratio error changes randomly between switching cycles. Due to a limited loop-gain bandwidth, the loop response usually lags far behind. Although a ramp compensation scheme was reported to resolve this [5], the improvement is very limited, and the scheme only works for voltage-mode converters.

To mitigate the above challenges, this paper presents a continuous RSSM (C-RSSM) scheme for EMI attenuation and a one-cycle $T_{ON}$-rebalancing (1TR) technique for $V_0$ jittering suppression, which are implemented in the converter of Fig. 15.7.2. The Markov-chain-based random clock implements analog $f_{SW}$ modulation within a sideband of $\Delta f_C$ centered at $f_{SW0}$. Hence, it conducts SSM continuously and spreads spurious noise at $f_{SW0}$ and its harmonics uniformly, achieving desirable C-RSSM. As illustrated in the spectrum plot, although conventional D-RSSM could achieve similar peak EMI reduction ($\Delta$EMI) with a wider modulation range ($\Delta f_D > \Delta f_C$), it elevates noise floor significantly due to spectral overlap. In the proposed Markov C-RSSM, the peak EMI and noise floor are both effectively attenuated with minimal die-area overhead. On the other hand, the proposed 1TR technique performs a two-step operation in each charge phase. As shown in Fig. 15.7.2, during $t_1$, the 1TR module detects the instant duty ratio D, determined by the converter PWM controller. By analyzing the sensed information of D and the instant $f_{SW}$ from the output of Markov-chain-based random clock, the 1TR adaptively adjusts the length of $t_2$. Hence, D and the ON-duty $T_{ON}$ of the converter are thus dynamically rebalanced to instantly modulated $f_{SW}$ within one cycle, preventing $V_0$ from jittering.

Figure 15.7.3 depicts the implementation of the Markov C-RSSM. From simulated $f_{SW}$ modulation, $f_{SW}$ traverses arbitrarily within the sideband $\Delta f_C$, creating a continuously and randomly distributed modulation pattern. Thus, noise spectrum at center frequency ($f_{SW0}$) and its harmonics can be uniformly spread. The random clock is designed using a Markov chain described by the chaotic criteria below [6]:

$$V_{ran}[n+1]=\begin{cases} kV_{ran}[n]+[(1-k)V_M+\Delta V], & V_{ran}[n]<V_M \\ kV_{ran}[n]+[(1-k)V_M-\Delta V], & V_{ran}[n]\geq V_M. \end{cases}$$

Here, $V_{ran}$ is the random output, $V_M$ and $\Delta V$ represent the center reference and the variation range, respectively, and k is the slope that should be well designed to avoid divergence issues. In the circuit of Fig. 15.7.3, to compute the next random state $V_{ran}[n+1]$, the present state $V_{ran}[n]$ is fed into a $G_m$ cell, which also drives the converted current $I_{gm}$ into a summation node $\Sigma$. Meanwhile, $V_{ran}[n]$ is compared to $V_M$. The comparison result multiplies the current $I_1$ in binary to implement the Markov partition. Finally, a fixed current $I_2$ is subtracted from the node $\Sigma$ to generate the random current $I_{ran}$, leading to $V_{ran}[n+1]=I_{ran}\times R_1$. Hence, the ratio of $R_1/R_2$ determines the slope k. By layout matching these two resistors, k could be well defined, ensuring the convergence of the Markov transitions. Triggered by the trailing edge of $V_{CMP}$ from the feedback loop, $V_{ran}[n+1]$ is sampled and added to $V_{DC}$, adjusting the VCO input $V_{ctrl}$ and hence the clock frequency. Thanks to Markov state transitions, $V_{ctrl}$ varies randomly within $\pm\Delta V$ centered at ($V_{DC}+V_M$) and $f_{SW}$ is modulated accordingly.

The proposed 1TR scheme and circuit are detailed in Fig. 15.7.4. $T_{ON}$ in a conventional PWM generator is initiated by the clock and reset by trailing edge of $V_{CMP}$. As $f_{SW}$ is varied by the RSSM, $T_{ON}$ cannot be corrected immediately due to a slow feedback path, resulting in $V_0$ jittering. To avoid this, the proposed 1TR module creates a fast $f_{SW}$ tracking path to modulate $T_{ON}$ synchronously with $f_{SW}$ dithering. As the trailing edge of $V_{CMP}$ triggers $f_{SW}$ transition, instant switching cycle of the converter is defined between two adjacent trailing edges of $V_{CMP}$. Two cycles, T[n] and T[n+1] ($=\alpha\times T[n]$), are shown in the waveforms. $T_{ON}$ in each cycle is split equally into $t_{on1}$ and $t_{on2}$ ($t_{on1}=t_{on2}$) in steady state. The operation could be explained by focusing on $t_{on2}[n]$ and $t_{on1}[n+1]$. The leading edge of the clock initiates $V_{PWM}$ and $t_{on2}[n]$. $I_L$ then ramps up. Meanwhile, the phase detector sets $V_{UP}$ to high, starting to charge $C_{cp}$ with $I_{UP}$. Controlled by the VCO input $V_{ctrl}[n]$, $I_{UP}$ is inversely proportional to T[n]. The $t_{on2}[n]$ is terminated until $V_{CMP}$ triggers low by the feedback loop and then $V_{UP}$ is reset to stop charging $C_{cp}$. Thus, $t_{on2}[n]/T[n]$ ($=0.5\times D[n]$) is converted into $V_{cp}$, completing D sensing. T[n+1] begins after $V_{CMP}$ flips to low. $I_L$ continues to rise as $V_{PWM}$ remains high. $I_{DN}$ is enabled by the trailing edge $V_{CMP}$ to discharge $C_{cp}$. As the trailing edge $V_{CMP}$ updates $V_{ctrl}[n]$ to $V_{ctrl}[n+1]$, $I_{DN}$ is inversely proportional to T[n+1]. When $V_{cp}$ hits $V_{RST}$, the comparator CMP1 triggers to terminate $t_{on1}[n+1]$ by resetting $V_{PWM}$. The charge conservation of $C_{cp}$ makes $t_{on1}[n+1]=\alpha\times t_{on2}[n]$. Hence, D is stabilized (D[n+1]=D[n]) cycle by cycle, eliminating $V_0$ jittering.

The prototype chip was fabricated in a 0.18μm HV CMOS process. Two enhancement mode GaN FETs are used as power switches. The converter delivers a maximum $I_0$ of 1.5A over wide input and output ranges of 3 to 40V and 1.2 to 5V, respectively. The C-RSSM modulates $f_{SW}$ at the center frequency of 8.3MHz with ±10% modulation range. The measured switching node $V_{SW}$ and EMI noise spectra are shown in Fig. 15.7.5. The Markov C-RSSM reduces the peak EMI noise by 31dBμV at the fundamental frequency and 35dBμV at the 3rd-order harmonic with the 27dBμV noise floor at the mid-frequency range. To validate the effectiveness of the 1TR scheme, Fig. 15.7.6 shows the measured $V_0$ waveforms. With conventional PWM design, the peak-to-peak magnitude of $V_0$ jittering is up to 240mV. With the proposed 1TR scheme, it drops below 10mV. In comparison to prior arts, this work achieves the lowest noise floor of 27dBμV. Implemented on a much higher technology node, the Markov-chain-based random source consumes 53% less silicon area than its digital counterpart [3]. With both using the C-RSSM, this work achieves 119% higher peak-EMI attenuation, and 3 times higher $V_0$-jittering suppression than [5]. The die micrograph is shown in Fig. 15.7.7, with the active area of 1.54mm$^2$.

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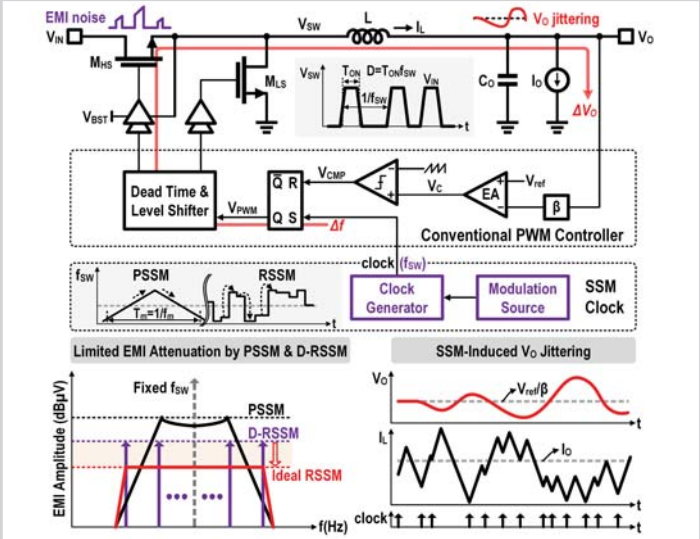



Figure 15.7.1: Challenges of implementing a spread-spectrum-modulation (SSM) scheme in power converters.

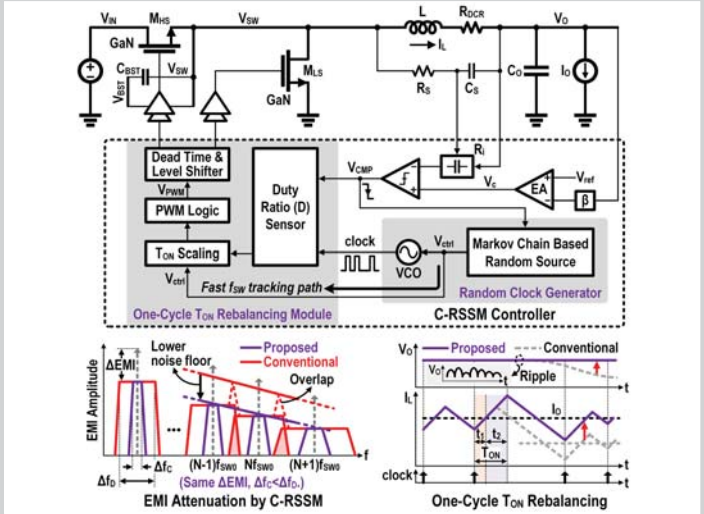



Figure 15.7.2: Proposed GaN power system with Markov continuous RSSM (C-RSSM) for EMI attenuation and one-cycle $T_{ON}$ rebalancing to eliminate $V_O$ jittering.

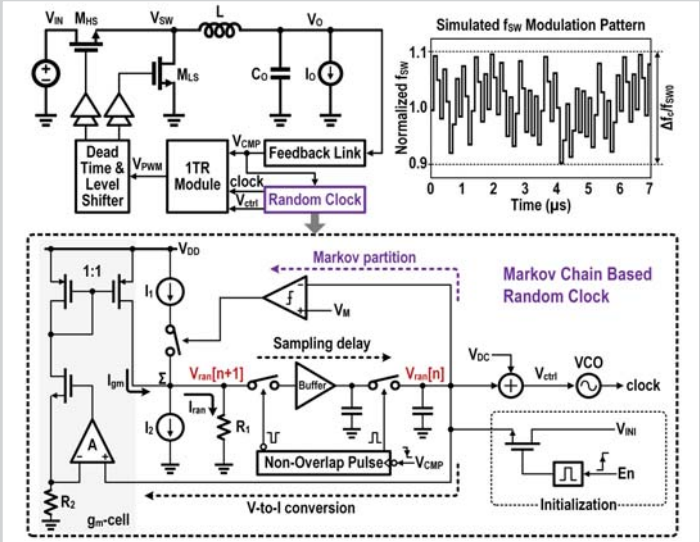



Figure 15.7.3: Implementation of the Markov continuous RSSM (C-RSSM) scheme.

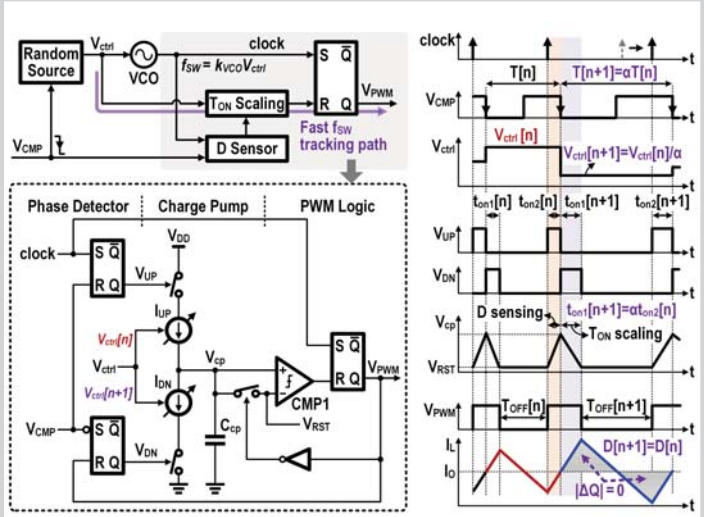



Figure 15.7.4: Scheme and circuit implementation of the proposed one-cycle $T_{ON}$ rebalancing.

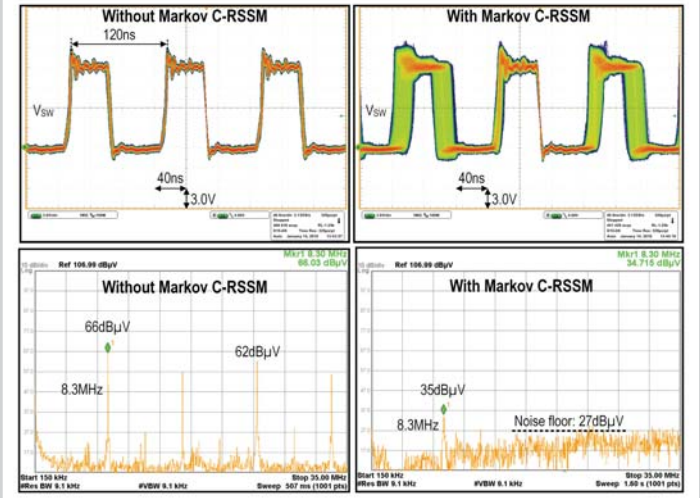
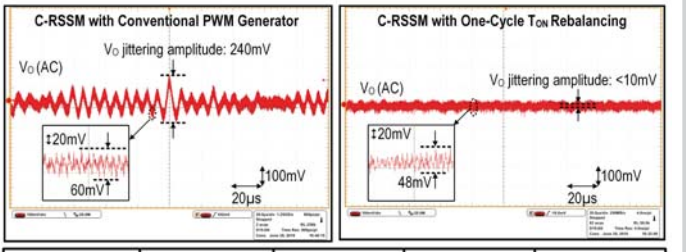



Figure 15.7.5: Measured switching-node transient waveforms and conducted-EMI noise attenuation with the C-RSSM.




| Design | | ISSCC2018 [3] | ISSCC 2017 [4] | CICC 2010 [5] | This Work |
|---|---|---|---|---|---|
| Process | | 55nm CMOS | 0.35μm HV BCD | 0.35μm CMOS | 0.18μm HV CMOS |
| Power Switch | | MOSFET | GaN FET | MOSFET | GaN FET |
| Control Mode | | Hysteresis current mode | PWM voltage mode | PWM voltage mode | PWM current mode |
| Central $f_{SW}$ | | 1MHz | 10MHz | 1MHz | 8.3MHz |
| $f_{SW}$ Modulation Way | | Discrete RSSM | Triangular modulation | Continuous RSSM | Continuous RSSM |
| Random Source Area | | 0.17mm² | Not reported | Not reported | 0.08mm² |
| $f_{SW}$ Modulation Range | | -21%/+22% | ±9% | ±20% | ±10% |
| Peak EMI Attenuation | | 35dBμV | 33dBμV | 16dBμV | 35dBμV |
| Peak Noise Floor | | 45dBμV | 52dBμV | Not applied | 27dBμV |
| $V_O$ Jittering Suppression | Amplitude | Not reported | Not reported | 18.1dB | >27.6dB |
| | Method | Pseudo hysteretic window | Not reported | Ramp compensation | 1TR scheme |

Figure 15.7.6: Measured $V_O$-jittering suppression by the one-cycle $T_{ON}$ rebalancing and a comparison table.

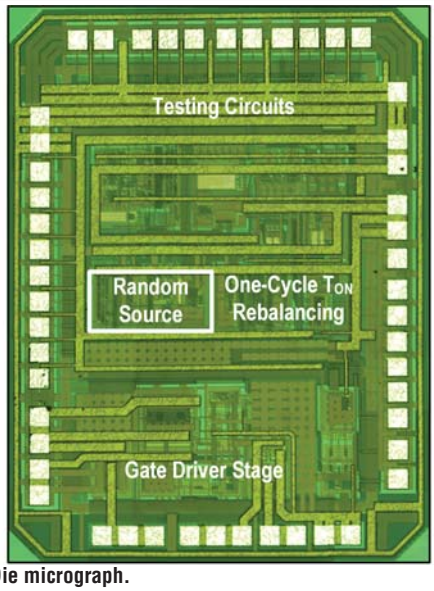



Figure 15.7.7: Die micrograph.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