A 120V-to-1.8V 91.5%-Efficient 36-W Dual-Inductor Hybrid Converter with Natural Soft-charging Operations for Direct Extreme Conversion Ratios

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***Abstract*—This paper presents a new dual inductor hybrid converter (DIHC) that is capable of efficient direct non-isolated DC-DC conversions with extremely large voltage conversion ratios. The converter employs two interleaved inductors and a switched-capacitor (SC) network to bring several significant topological benefits. Capacitance of the flying capacitors of this new topology can be optimally sized to achieve natural, complete soft-charging for all capacitors. This novel capacitor soft-charging feature is a key contribution of this work and can be exploited to overcome the limitations of conventional SC converters suffering from capacitor hard charging losses. The converter topology and its operation are verified in an 36-W converter prototype for 40-120V input to 0.9V-1.8V output up to 20A of current load that achieves peak efficiencies of 91.5% for 120V-to-1.8V and 87.3% for 120V-to-0.9V conversion. Its advantages and performance at extreme conversion ratios push the limit of point-of-load converters, reducing complexity and cost for bus voltage distributions, as well as enabling fewer conversion stages and thus higher efficiency for data centers and high-performance digital systems.**

***Keywords*—Hybrid converter, complete soft-charging, switched capacitor network, capacitance optimization.**

I. Introduction

There is urgent need for an efficient regulator that can support large conversion ratios to bridge the voltage differences between system distribution bus and core voltages in both data center and telecommunication system power delivery architectures [1]. In these high-performance digital systems, the processor and core voltages, ranging from ∼0.6V to 1.8V, demand increasingly high currents to meet required computing needs. To provide these voltage rails, point-of-load (PoL) converters that can support large conversion ratios are desirable to reduce board level distributions by lowering currents at a higher bus voltage. In this trend, 48-V PoL converters are replacing conventional 12-V solutions [2]. However, large conversion ratios, i.e. 48V-to-1.8V, come with escalated challenges in the converter design to achieve both high efficiency and high power density. In addition to difficulties in choosing optimal switches with satisfying breakdown voltages, at large conversion ratios, the required duty cycle of power switches that gets problematically small and comparable to rise-time and fall-time of gate driver signals poses a key challenge in switch control, stressing the controller's resolution limit for output regulation. To deal with the challenges, different converter architectures have been studied that can be categorized into multi-stage, single-stage, isolated, and non-isolated solution. Multi-stage solutions benefit from simple implementations realized by commercial converter building blocks e.g. 48V-to-12V and 12V-to-1V blocks, but suffer from efficiency limit at ∼90% because of cascaded conversion stages. An isolated converter reported in [3] uses a resonant ICN architecture to achieve ∼90% efficiency for a 48V-to-1.8V conversion. In the non-isolated category, 93.4% peak efficiency was achieved by a single-stage sigma converter using one transformer for a 48V-to-1V conversion [4]. This converter, however, requires a complex startup control and its efficiency severely degrades with input voltage variations [5].

To avoid bulky transformers and related complexities in isolated converters, this work focuses on non-isolated direct conversion. In this category, hybrid converter topologies, e.g. flying capacitor multilevel (FCML)[6] and Hybrid Dickson [7], [8], have been explored recently. Non-isolated hybrid topologies exploit a flying capacitor network to block most of the input voltages, and an inductor at the output to provide a required fine regulation. More importantly, to achieve high efficiency the inductor can be operated to softly charge or discharge the capacitors as a current source. As the result, this architecture overcomes the fundamental hard-charging loss, i.e. slow switching limit loss, in traditional switched-capacitor converter that limits efficiency to fine conversion ratios [9], [10]. As the SC part blocks a large portion of the input voltage, the voltage swing that the inductor and power switches process

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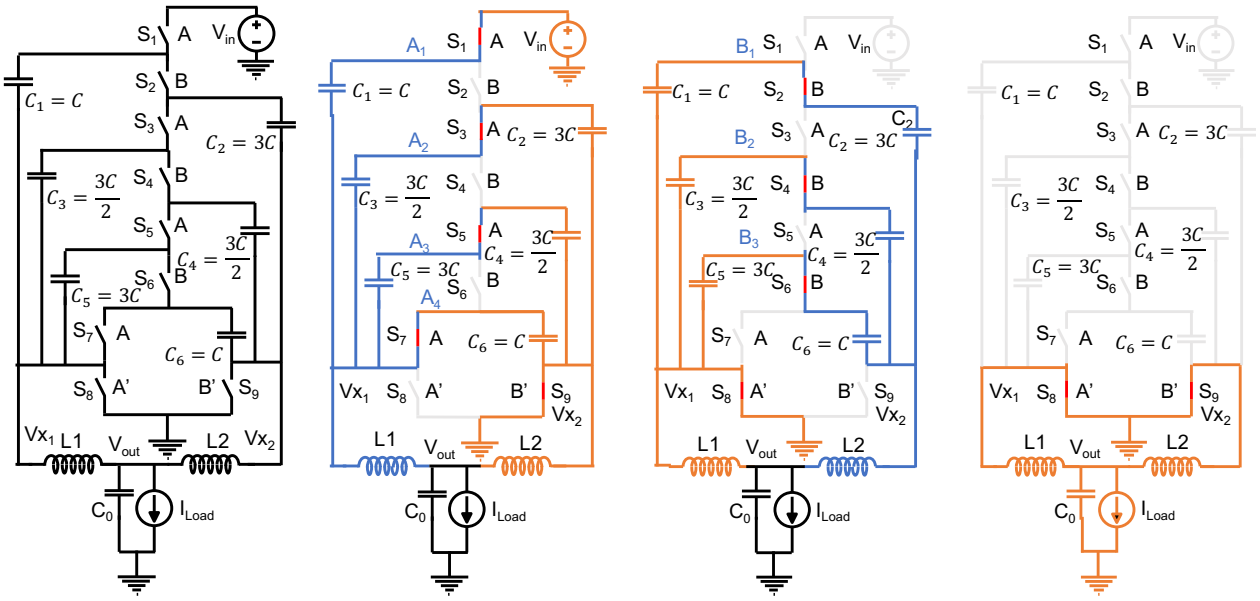

(a) State 1(Active Phase: A) (b) State 3 (Active Phase: B) (c) States 2 and 4

Fig. 1. 7-to-1 DIHC Schematic

Fig. 2. Schematic and operating states of the proposed DIHC

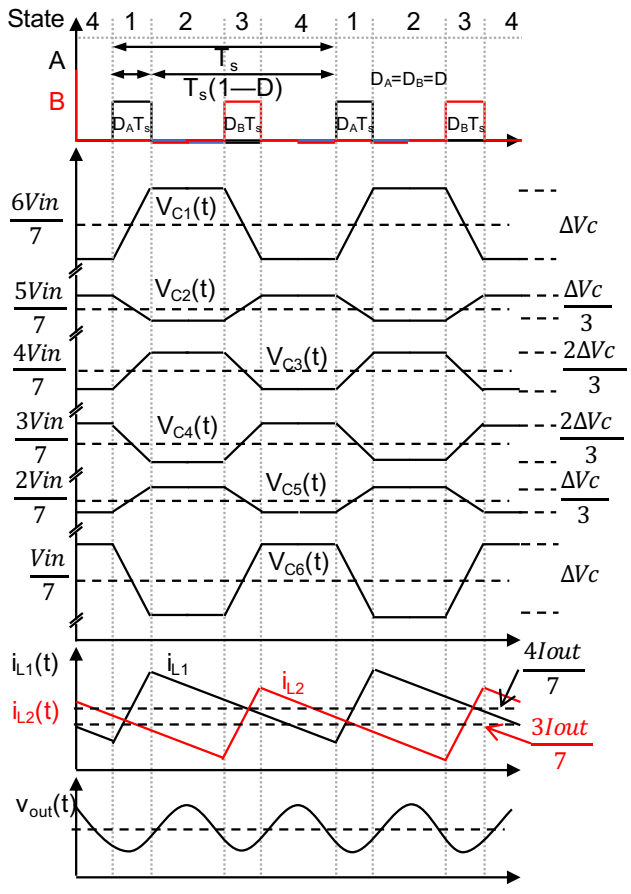

Fig. 3. Operational waveforms of the proposed DIHC

is reduced significant.

The small voltage swing applied at the inductors enables these hybrid converters to operate at reasonable duty cycles avoiding disadvantages of extremely small duty cycles, e.g. high resolution PWM requirement, poor switch utilization, or increase in conduction loss. The (FCML) converter in [6] was demonstrated to obtain ∼85% efficiency for a 48V-to-2V conversion, while the Hybrid Dickson converter in [8] achieved ∼95.2% maximum efficiency[8] for a voltage conversion from 130V to 12V at 2A load. Note that for the same output power and conversion ratio, achieving a high power density at n times lower output voltage is n^2 times, i.e. quadratically, harder because of both n times higher output current and n times lower output voltage.

The dual-inductor hybrid converter (DIHC) proposed in this paper, shown in Fig. 1, shares the key benefits of the published hybrid converter topologies, i.e. complete soft charging for flying capacitors and low voltage stresses on power devices. Moreover, it overcomes their complexities and drawback, including the complicated capacitor voltage balancing circuit in the FCML converter and the split-phase control[7], required in the Hybrid Dickson, to guarantee desired capacitor voltages for soft-charging. The Hybrid Dickson converter also suffers from duty cycle reduced by a factor of 2, i.e. $D = \frac{NV_{out}}{2V_{in}}$, from the original ratio $\frac{NV_{out}}{V_{in}}$. The proposed DIHC has two naturally interleaved inductors capable of supporting high output currents and providing advantages, similar to multi-phase interleaved Buck converters[11]. Its simple Buck-like interleaved PWM operation yields the original, wider duty cycle of $D = \frac{NV_{out}}{V_{in}}$, allowing extremely large conversion ratios. More details of the converter operations and advantages will be provided in Sections II and III. Experimental results of a DIHC prototype supporting an extreme conversion ratios of

TABLE I
IMPORTANT EXPRESSIONS OF THE PROPOSED DIHC

	Values of the Flying Capacitors	Flying Capacitor Voltage						Output Voltage	Expr. No.
		V_{C_1}	V_{C_2}	V_{C_3}	V_{C_4}	V_{C_5}	V_{C_6}	V_{out}	
Steady State Values		$\frac{6V_{in}}{7}$	$\frac{5V_{in}}{7}$	$\frac{4V_{in}}{7}$	$\frac{3V_{in}}{7}$	$\frac{2V_{in}}{7}$	$\frac{V_{in}}{7}$	$\frac{DV_{in}}{7}$	(1)
At the end of state 3	When$C_{1-6}=C$	$\frac{6V_{in}}{7}-\frac{\Delta V_c}{2}$	$\frac{5V_{in}}{7}+\frac{\Delta V_c}{2}$	$\frac{4V_{in}}{7}-\frac{\Delta V_c}{2}$	$\frac{3V_{in}}{7}+\frac{\Delta V_c}{2}$	$\frac{2V_{in}}{7}-\frac{\Delta V_c}{2}$	$\frac{V_{in}}{7}+\frac{\Delta V_c}{2}$		(2)
	When $C_1=C_6=C$, $C_2=C_5=3C$, $C_3=C_4=\frac{3C}{2}$	$\frac{6V_{in}}{7}-\frac{\Delta V_c}{2}$	$\frac{5V_{in}}{7}+\frac{\Delta V_c}{6}$	$\frac{4V_{in}}{7}-\frac{\Delta V_c}{3}$	$\frac{3V_{in}}{7}+\frac{\Delta V_c}{3}$	$\frac{2V_{in}}{7}-\frac{\Delta V_c}{6}$	$\frac{V_{in}}{7}+\frac{\Delta V_c}{2}$		(3)
		Voltage at node V_{x_1} by active branches							
Branch		A_1		A_2		A_3		A_4	
		$V_{in}-V_{C_1}$		$V_{C_2}-V_{C_3}$		$V_{C_4}-V_{C_5}$		V_{C_6}	
At the beginning of State 1	When$C_{1-6}=C$	$\frac{V_{in}}{7}+\frac{\Delta V_c}{2}$		$\frac{V_{in}}{7}+\Delta V_c$		$\frac{V_{in}}{7}+\Delta V_c$		$\frac{V_{in}}{7}+\frac{\Delta V_c}{2}$	(4)
	When $C_1=C_6=C$, $C_2=C_5=3C$, $C_3=C_4=\frac{3C}{2}$	$\frac{V_{in}}{7}+\frac{\Delta V_c}{2}$		$\frac{V_{in}}{7}+\frac{\Delta V_c}{2}$		$\frac{V_{in}}{7}+\frac{\Delta V_c}{2}$		$\frac{V_{in}}{7}+\frac{\Delta V_c}{2}$	(5)
$V_{out}=\frac{DV_{in}}{N}$ and $V_{C_k}=\frac{(N-k)V_{in}}{N}$, where, $k=1,2,....,N-1$									(6)
$C_{A_1}=C_1,\ C_{A_2}=C_2\|\|C_3,\ C_{A_3}=C_4\|\|C_5,\ C_{A_4}$=$C_6,\ C_{B_1}=C_1\|\|C_2,\ C_{B_2}=C_3\|\|C_4,$ and $C_{B_3}=C_5\|\|C_6$									(7)
$C_{B_1}=C_{B_2}=C_{B3}$ and $C_{A_1}=C_{A_2}=C_{A_3}=C_{A_4}$									(8)
$C_1=C,\ C_2=3C, C_3=\frac{3C}{2}, C_4=\frac{3C}{2},\ C_5=3C,\ C_6=C,\ C_A=C$ and $C_B=\frac{3C}{4}$									(9)
$C_k=\frac{N-1}{N-k}C,$ when k is an odd number or $C_k=\frac{N-1}{k}C$ when k is an even number $C_n=C_{N-n},\ C_A=C,\ C_B=\frac{N-1}{N+1}C$ where, $n=1,\ 2,\ ....,\ \frac{N-1}{2}$ and $k=1,\ 2,\ 3....,\ \frac{N-1}{2}$									(10)

120V-to-0.9V is presented in Section IV. The paper will then be concluded in Section V.

II. DUAL INDUCTOR HYBRID CONVERTER TOPOLOGY AND OPERATION

To provide extreme conversion ratios and high output currents, an exemplary 7-to-1 (M = 8 levels) DIHC topology is shown in Fig. 1. The converter operational states are shown in Fig. 2 and its key operational waveforms in Fig. 3. The converter employs six flying capacitors, nine switches and two output inductors. This configuration allows the proposed topology to obtain the same voltage division at the switching node, N-to-1 using only $N+2$ switches compared to a Hybrid Dickson counterpart comprising $N+4$ switches, which leads to better switch utilization and loss reduction as will be discussed in Section III. The converter topology has two interleaving halves. The right half includes three capacitors $C_{1,3,5}$, inductor L_1, and two switches $S_{7,8}$. The left half includes three capacitors $C_{2,4,6}$, inductor L_2, and switch S_9. Illustrated in Fig. 2, these two halves operate in two interleaved phases, Phase A and B, that have the same duty cycle and are offset by 180 degrees, or $\frac{1}{2}T_s$. As color-coded in Fig. 2 where components in blue are charging and ones in orange discharging, the odd-numbered switches $S_{1,3,5,7,9}$ in phase A during State 1 (Fig. 2a) charge inductor L_1 while soft-charging $C_{1,3,5}$ and soft-discharging $C_{2,4,6}$. Similarly, during State 3 (Fig. 2b), the even-numbered switches $S_{2,4,6,8}$ in phase B charge L_2 also soft-charging $C_{2,4,6}$ and soft-discharging $C_{1,3,5}$. During States 2 and 4 (Fig. 2c), the upper switches $S_{1\text{-}7}$ stay off leading the flying capacitors idle and the inductors L_1 and L_2 freewheeling via switch S_8 and S_9, respectively.

Considering small voltage ripples in the capacitors and small current ripple in the inductors, a steady state analysis shows the capacitor voltages gradually decrease from V_{C1} to V_{C6}, similar to a regular 7-to-1 Dickson switched-capacitor converter, and output voltage V_{out} is $\frac{DV_{in}}{7}$, as listed in expression 1 in Table I. A general steady states of an N-to-1 DIHC are also given in expression 6.

Since the SC network works as DC transformer, the output voltage can be simply regulated by controlling the duty-cycle D. The capacitor voltages are also balanced to particular voltages based only on a given input voltage. Compared with the Hybrid Dickson converter counterpart in [7] having $V_{out} = \frac{2DV_{in}}{N}$, the proposed DIHC is capable of reaching half the output voltage for the same input voltage, duty-cycle, and switching frequency implying benefit in extreme step-down conversion with reasonable on-time.

III. SOFT-CHARGING OPERATION AND STRATEGY FOR CAPACITOR SIZING

As the proposed circuit features different circuit configuration and accompanies unique capacitor design consideration to achieve soft-charging, this section reveals fundamental background of circuit operation and provides its basic idea.

A. Switched Capacitor Network Operation and Two Inductor Current

In the DIHC topology, the same charge flows sequentially from higher to lower level through the capacitors in phase A and B either charging or discharging a capacitor around its steady state value while maintaining capacitor charge balance. When the same duty cycle D is applied to both phases A and B ($D_A = D_B = D$ as in Fig. 1), this results in the same current through the capacitor branches, regardless of phase or capacitances in the branches. Inductor L_1 in state 1 sees four branches of capacitors, including C_1, C_2-C_3, C_5-C_4, and C_6, while L_2 in state 3 sees only three branches of capacitors, including C_1-C_2, C_3-C_4, and C_5-C_6 . This results in different current averages of the two inductors proportional to the number of interacting branches. In case of 7-to-1 DIHC in Fig. 1, the average current of inductor L_1 is $\frac{4}{3}$ times of that of inductor L_2, or, $I_{L1} = \frac{4}{3} I_{L2}$. To generalize in case of an N-to-1 DIHC where N is an odd number, $\frac{N+1}{2}$ branches will be tied to L_1 at node V_{x_1} and $\frac{N-1}{2}$ branches to L_2at V_{X_2}; $I_{L_1} = \frac{N+1}{N-1} I_{L_2}$. Although the inductor current are unequal, their proportional behavior is a natural characteristic of odd level DIHCs. The two currents can be made equal by adjusting the duty cycle of phase B $\frac{N+1}{N-1}$ times that of phase A. However, that will result in higher conduction loss in the active components during phase B.

B. Capacitance Optimization to Achieve Complete Capacitor Soft-Charing

Note that capacitors $C_{2\text{-}5}$ always (both in Phase A and B) transfer their charge in series combination with other capacitors; C_2 operates with either C_1 or C_3. On the contrary, C_1 and C_6 operates alone in phase A and B, respectively. Also, the charging and discharging charges through individual capacitors are equal and they do not depend on the capacitances. These conditions imply that the voltage swings on capacitors C_1 and C_6 be higher than the other capacitors. That translates that if all flying capacitors are sized identical (same capacitance), hard charging will happen in switched capacitor network operations, specifically in the beginning of State 1 and 3.

As example, if capacitors $C_{1\text{-}6}$ are chosen so that they have a same base value of C. And, assumably, at the end of state 2, all the capacitor voltages occupy charges to have same voltages like their steady states as in expression 1.

In state 3, charges re-distribute in the capacitor network and C_1, C_3 and C_5 give away charges to C_2, C_4 and C_6. Because of charge re-distribution, there will be a change in the voltage of every capacitor. As the amount of charges shared among the capacitors are same, this absolute change of voltages will also be same. If this absolute value is termed as $\frac{\triangle V_c}{2}$, at the end of state 3, the capacitor voltages are shown in expression 2.

Capacitor network remains inactive during state 4. During state 1, capacitors re-organize among themselves building four capacitor branches having different effective voltage at node V_{x1} shown in expression 4. These voltage mismatches creates current flow initially from one branch to another until the mismatches are resolved instead of the natural flow of currents from these branches to the inductor. This is the hard-charging problem due to voltage ripple mismatch also present in Hybrid Dickson converter[7], [8].

In order to eliminate the hard-charging and achieve complete soft-charging, a capacitor size optimization strategy is proposed. The purpose of this optimization is to make all branches' effective capacitances connected by the same switching node equal both active states. In the proposed 7-to-1 DIHC topology, equivalent capacitances of different branches in State 1 and 3 are shown in expression 7, where the operator $\|$ is used to express $C1{*}C2/(C1{+}C2)$, equivalent capacitance of series capacitors. For hard-charging elimination, according to the proposed strategy, the equivalent capacitances of all the branches need to equal as shown in expression 8. Solving expression 7 and 8 yields the optimal capacitance values as in expression 9.

By the optimal capacitance ratios, the absolute changes in capacitor voltages become different at the end of state

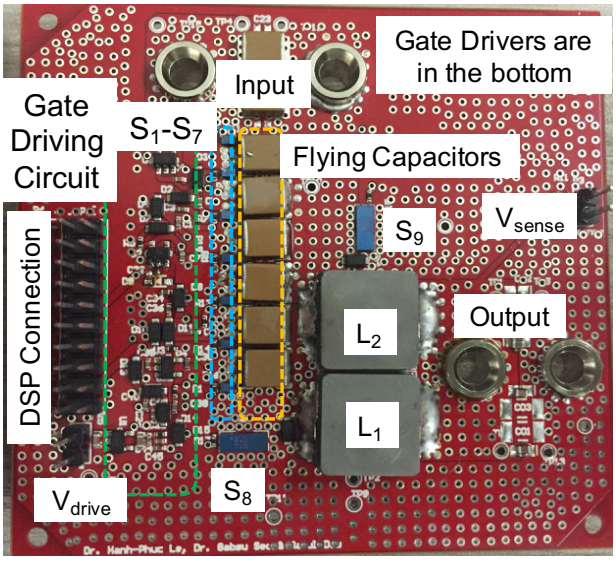

Fig. 4. 7-to-1 DIHC prototype PCB

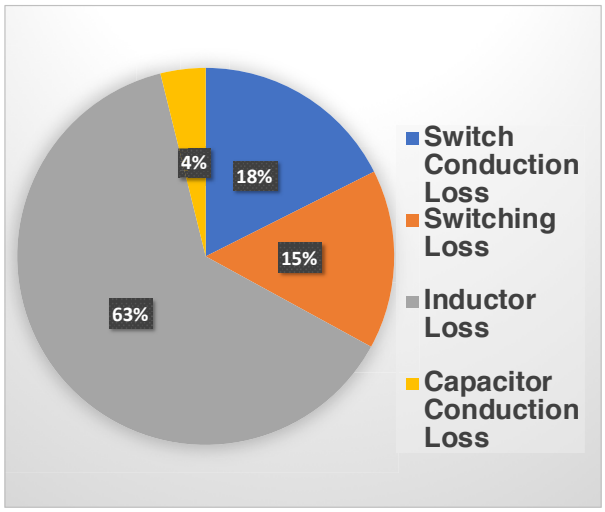

Fig. 5. Analytical loss breakdown at 120V-to-1.8V/15A conversion at 250kHz switching frequency

TABLE II
KEY COMPONENTS

Component	Part
S_{1-7}	EPC2014c
S_{8-9}	EPC2023
C_1	2x0.68uF 450V TDK
C_2	2.2uF+2x1.0uF 450V TDK
C_3	2.2uF 450V TDK
C_4	1.0uF+0.68uF 450V TDK
C_5	2.2uF+1.0uF 450V TDK
C_6	1uF 450V TDK
L_{1-2}	2.2 uH IHLP5050EZER1R8M01
Isolated Gate Drivers	Si8275-GBD IS1

3(expression 3) and the voltages generated on all the branches at the beginning of State 1 become equal to $\frac{V_{in}}{7} + \frac{\Delta V_C}{2}$ as expressed in 5 on Table I, which verifies complete soft charging operations of all flying capacitors. This converter characteristic is also illustrated in Fig. 1. The capacitor values required for full soft-charging in a general N-to-1 DIHC with an odd number N, can be defined as in expression 10. This selection of the capacitances enables the converter to achieve complete soft-charging by resulting all effective branch capacitances in each phase equal.

IV. EXPERIMENTAL RESULTS

To demonstrate the feasibility of the new converter topology, a 7-to-1 DIHC converter prototype is implemented for 120V to 0.9-1.8V/20A whose printed circuit board is displayed in Fig. 4. The component selection is tabulated in Table II. Converter average model is employed to design switches and capacitors with the proposed capacitor size optimization strategy. Analytical loss break down according to the model has been shown in Fig. 5. Capacitors in this implemented prototype experience different voltages as they are connected between different levels of the converter. As the capacitance values are highly dependent on the voltages they experience, capacitance degradation occurs differently for capacitors of different levels. To compensate for this problem, the capacitors

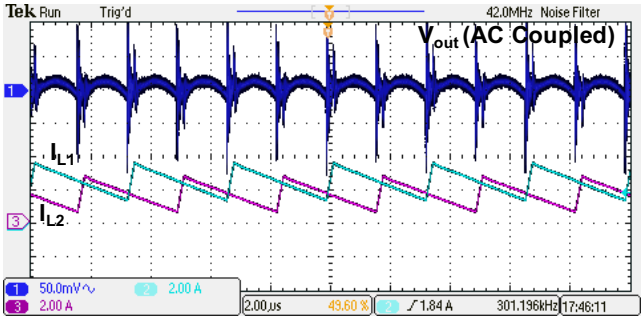

Fig. 6. Key operational waveforms at 120V-to-0.9V/4A

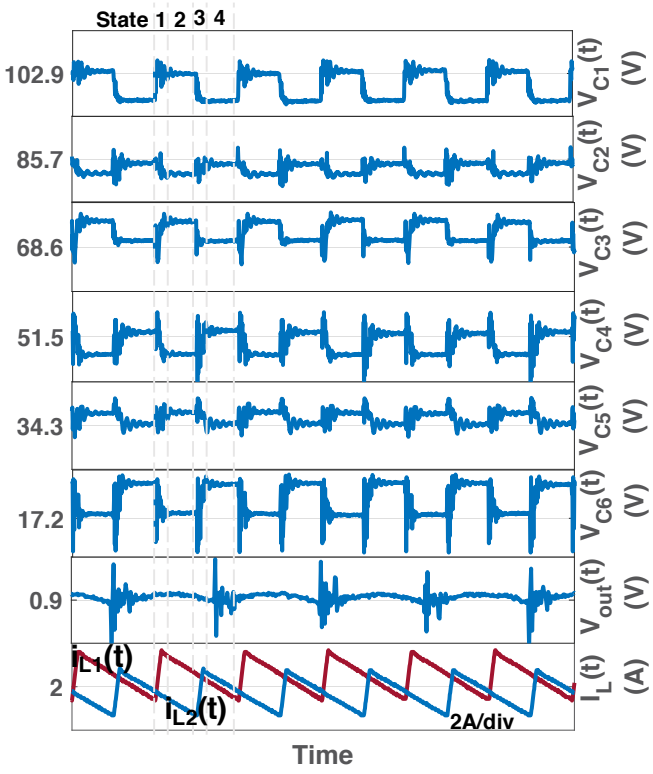

Fig. 7. Flying capacitor voltages at 120V-to-0.9V/4A

are sized according to the data-sheets so that after degradation they maintain the optimal ratio calculated in expression 9.

Pulse width modulated(PWM) signals required to drive the converter were generated from a TMS320F28377S micro-controller[12]. Fig. 6 shows key operational waveforms of the converter in steady state operation with two inductor currents having expected different average values. Experimental capacitor voltages along with inductor currents are illustrated in Fig. 7 verifying the capacitor soft-charging. Note that, Fig. 6 and 7 are achieved at 4A load which is not the optimum operating condition. Converter efficiency data are shown in Fig. 8 and achieved using the stated values of passive components in Table II. The converter achieves 87.3% peak efficiency at an extreme 130:1 conversion ratio from 120V to 0.9V at 15A load, and 91.5% peak efficiency at 66.7:1 conversion ratio from 120V to 1.8V at 15A load, operating at 250kHz frequency, validating its feasibility in applications where high

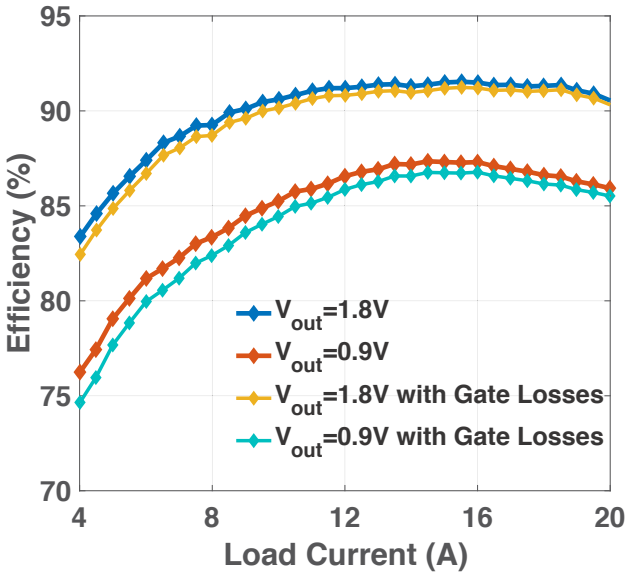

Fig. 8. Efficiency at 120V input voltage

conversion ratio with reasonable efficiency is required. The converter has been tested up to 20A of load currents with input voltage range of 40V-120V at 0.9V-1.8V output voltage. These wide input range also makes this converter suitable for applications where varied range of input voltage is regulated and supplied to very low output voltage.

V. CONCLUSION

This paper presented a new hybrid converter using two interleaved inductors that is verified to be able to support extreme conversion ratios with promising efficiency given the first implementation. The converter works with two interleaving phases sharing the same core capacitor networks achieving natural soft-charging and balance with a simple capacitor sizing strategy. The converter performance can be a very promising candidate for future converters with extreme conversion ratios that can push the limit of point-of-load converters, reducing complexity and cost for bus voltage distributions, as well as enabling conversion stage reduction and thus achieving higher efficiency in data centers and high-performance digital systems. A proof-of-concept DIHC prototype has been verified desirable operations and characteristics of the converter, achieving up to 87.3% peak efficiency at 130:1 conversion ratio, 91.5% peak efficiency at 66.7:1 conversion ratio, and wide input and output voltage ranges.

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