A 95%-Efficient 48V-to-1V/10A VRM Hybrid Converter Using Interleaved Dual Inductors

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***Abstract*—This paper presents a new 48 V-to-1 V hybrid converter. The converter utilizes two interleaved inductors to achieve complete soft-charging of flying capacitors to efficiently support high output currents. This dual inductor hybrid converter (DIHC) features fewer number of switches and more effective switch utilization than a recently reported hybrid Dickson converter, leading to substantially less conduction losses presented by a smaller equivalent output impedance. Experimental results verify the converter's operation principles and advantages in a 300-kHz 20-W prototype achieving 95.02% peak efficiency and 225 W/in3 power density. Its advantages and performance promise a good candidate converter architecture for applications that require large conversion ratios and high output currents, such as data centers and high-performance digital systems.**

Keywords—Hybrid converter, high power density, GaN devices, soft-charging, switched capacitor converter, inductor current sharing

I. INTRODUCTION

With drastically increasing demands for cloud computing and big data processing, the electric energy consumption of data centers in the U.S. is expected to reach 73 billion kWh by 2020 [1] accounting for ~10% of the U.S total electric energy consumption. A large portion of this consumption is caused by losses in inefficient power delivery architectures that require a lot of attentions and improvements [2], [3]. As the required distribution currents keep increasing for more demanding digital loads, the conventional 12-V bus architecture has exposed higher losses, complexity, and cost for interconnects and power delivery network. To address these issues, the 48-V bus architecture has emerged to be a new industry standard, employed by Google, HP and other prominent data center designers and users [4]. However, the large conversion ratio from 48 V to core voltages, i.e. ~1-1.8 V, poses significant challenges in the design of voltage regulator module (VRM) [5], [6], [7], pressing for high efficiency and high power density for installations in the vicinity of CPUs.

To deal with the challenges in the 48-V VRM, new ideas and improvements have been proposed and implemented. The CPES proposed a two stage 48-V VRM architecture using a 48-12-V LLC converter, which uses a matrix transformer to achieve 850 W/in^3 power density, cascaded by 12-1.8-V multiphase buck converters [3]. However, its efficiency is limited to 91% because of the two stage structure. To overcome limited efficiency of two stage structure, hybrid converters bridge the large conversion ratio by efficient utilization of passive components [8], [9]. The 7-level flying capacitor multilevel (FCML) converter presented in [8] converts 48 V to 2 V using 12+1 switches, 5 flying capacitors, and 1 output inductor. While in N-level multilevel converters the inductor can be significantly reduced compared to a conventional Buck converter counterpart, it requires 2(N—1) switches half of which experience the output current in operations, leading to large conduction losses in low-voltage high-current applications such as in data centers. Another hybrid converter based on Dickson switched capacitor converter can be a potentially better candidate for the 48-V VRM thanks to reduced stresses on switch voltage and switch current, and efficient charge delivery performance [9]. The Dickson converter in Fig. 1 reported in [9] uses a single inductor at the output to achieve complete soft-charging for the flying capacitors. The shortcoming of this converter is exposed in low-voltage high-current applications that requires large conversion ratios and thus small duty cycle. Although the upper switches $S_{1\text{-}6}$ only needs to conduct input current, the bottom switch pairs $S_{7,9}$ and $S_{8,10}$ have undesirable series connections when carrying the output current in the inductor's freewheeling mode. That leads to high conduction losses (more details in Section III).

In this paper, a new *Dual Inductor Hybrid Converter* (DIHC), also based on the Dickson switched capacitor converter, is proposed to effectively address the drawbacks of the conventional approaches. The DIHC, shown in Fig. 2, employs two interleaved inductors at the output and eliminates two large synchronous switches S_9 and S_{10} in the hybrid Dickson converter in Fig. 1. These modifications enable DIHC to have nearly 2X lower DC output impedance contribution of conduction of switches and flying capacitors and thus 2X smaller conduction losses than the hybrid Dickson converter. In addition, the two interleaved inductors with naturally self-balanced currents provide DIHC with the same benefits of multi-phase converters for high current application [10] without additional current balancing complexity. Split phase operation proposed in [9] is also employed in DIHC to achieve complete soft-charging for all the capacitors. Section II of this paper describes the proposed DIHC's circuit operation. Section III provides its steady-state characteristics to identify its key features and advantages. Experimental results of the converter prototype are presented in Section IV.

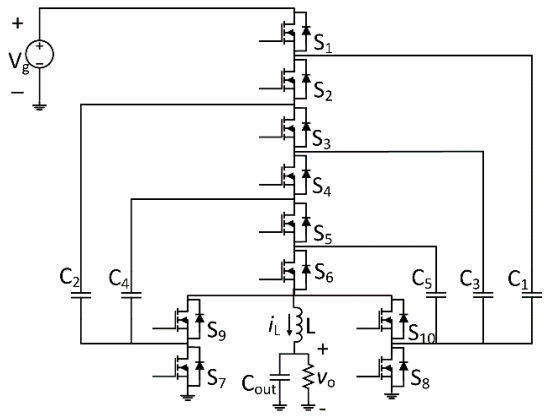

Fig. 1. 6-to-1 hybrid Dickson converter [9].

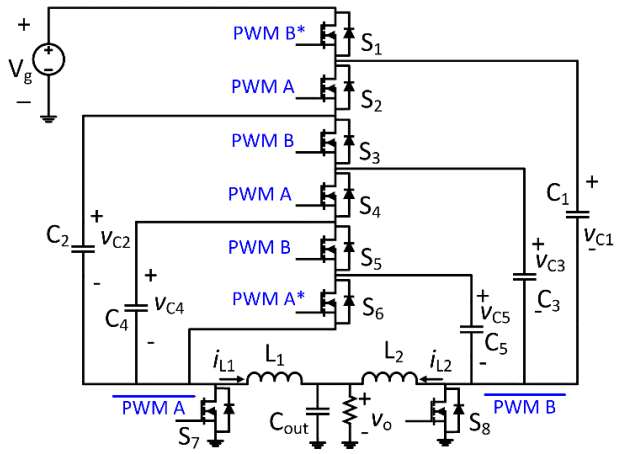

Fig. 2. Proposed dual inductor hybrid converter (6-to-1).

II. CIRCUIT OPERATION OF DIHC

A. Operation Principle of DIHC

This paper investigates a 6-to-1 DIHC shown in Fig. 2 and the following analysis can be extended to other variations using different division, e.g. 10-to-1 using 12 switches and 9 capacitors, for other operating conditions and optimization strategy. The 6-to-1 DIHC employs five capacitors $C_{1\text{-}5}$ with equal capacitance and two identical inductors $L_{1,2}$. In steady-state, it is assumed that the capacitor voltages v_{C1}, v_{C2}, v_{C3}, v_{C4}, and v_{C5} have the same small voltage ripple, Δv_C around $\frac{5}{6}V_g, \frac{4}{6}V_g, \frac{3}{6}V_g, \frac{2}{6}V_g$, and $\frac{1}{6}V_g$, respectively.

The operation of the DIHC can be explained using five equivalent circuits of five operational modes shown in Fig. 3 together with operating waveforms of capacitor voltages $v_{C1\text{-}5}$ and inductor currents $i_{L1\text{-}2}$ in Fig. 4. For simplicity in mode analysis and to deliver the insights of the converter operation, the capacitor voltages and inductor currents are assumed to be small [11]. Having the two sub-modes, Mode 1a and Mode 3a, allows the converter to achieve complete soft-charging in the same mechanism of split phases in the hybrid Dickson converter in [9]. Theoretically, with assumption of small inductor current

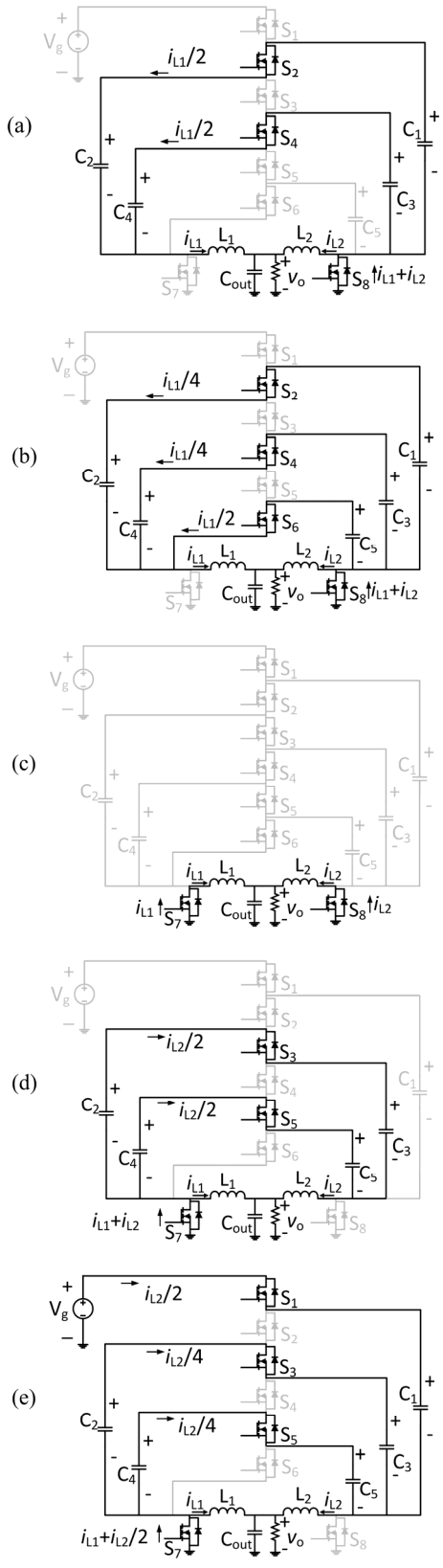

Fig. 3. Equivalent circuits of DIHC in different modes: (a) mode 1a, (b) mode 1b, (c) mode 2, (d) mode 3a, and (e) mode 3b.

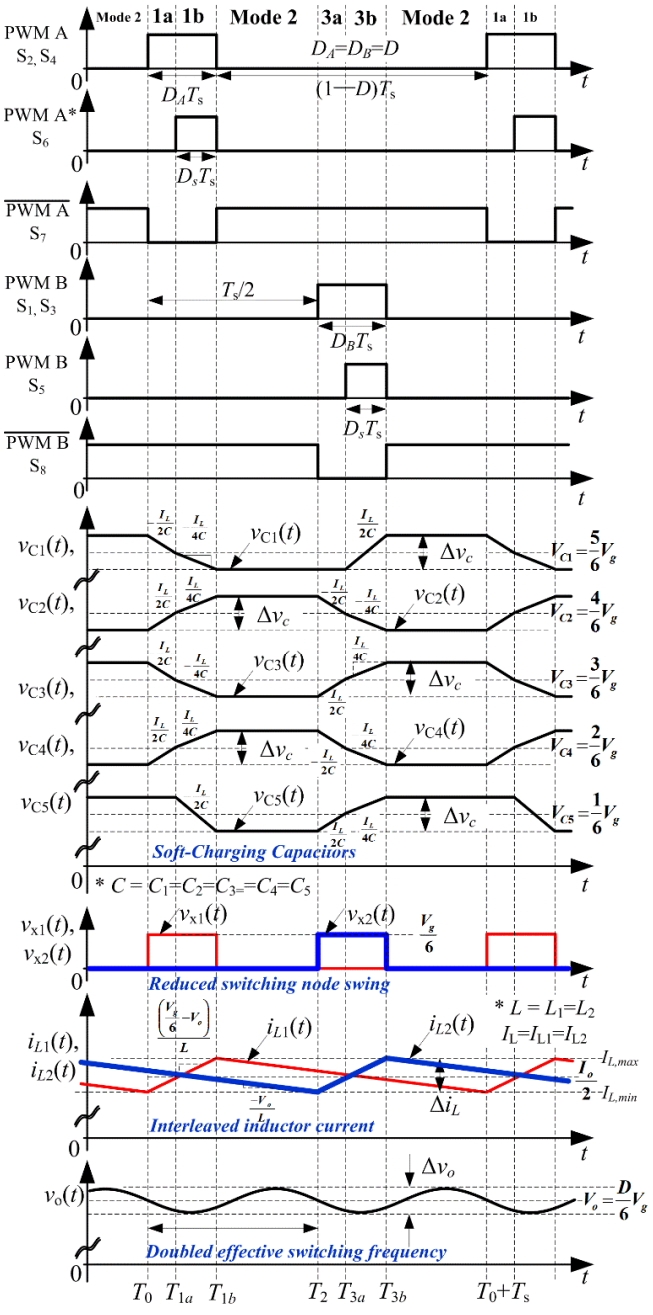

Fig. 4. Circuit operation of DIHC.

ripple, Mode 1b and 3b are equally-timed and twice longer than Mode 1a and 3a or D_s=2/3D. In practice, the ratio would be optimally engineered considering the inductor ripple to achieve complete capacitor soft-charging. The ratio between Mode 1 (1a+1b) or Mode 3 (3a+3b) to the rest of a period determines the converter duty cycle D as illustrated in Fig. 4 and it is used to regulate the converter output similar to conventional pulse width modulated (PWM) power converters.

Mode 1a starts with S_2, S_4, and S_8 turned on, leading to two parallel branches of two series-connected capacitors, C_1-C_2 and C_3-C_4, sharing the current I_{L1}, while C_5 is open-circuited and conducts no current. Switching node v_{x1} receives $\frac{1}{6}V_g$ from the capacitors, charging L_1. S_8 conducts i_{L1}+i_{L2} with L_2 discharging as displayed in Fig. 3(a). Compared with Mode 1a, Mode 1b illustrated in Fig. 3(b) has S_6 turned on to add an additional branch of single capacitor C_5 to the capacitor networks sharing I_{L1}. With half the effective capacitance compared with the C_5 branch, C_1-C_2 and C_3-C_4 branches only conduct $\frac{I_{L1}}{4}$ while C_5 conducts $\frac{I_{L1}}{2}$, leading to 2X lower charging/discharging slopes for $C_{1\text{-}4}$, as illustrated in Figs. 3(b) and 4. Since all capacitor branches equates same voltages, switching node voltage remains at $\frac{1}{6}V_g$ and continue charging L_1 as

$$v_{x1} \approx V_{C1} - V_{C2} = V_{C3} - V_{C4} = V_{C5} = \frac{1}{6}V_g \,. \qquad (1)$$

In Mode 2, similar to synchronous Buck converters, the freewheeling switches S_7 and S_8 conduct discharging inductor currents, i_{L1} and i_{L2}, respectively, while high side switches $S_{1\text{-}6}$ stay turned off, opening the capacitors and leaving their voltages unchanged as illustrated in Fig. 3(c) and Fig. 4.

Mode 3a begins with S_3, S_5, and S_7 turned on, initiating the same charging/discharging currents, $\frac{I_{L2}}{2}$, on two capacitor branches, C_2-C_3 and C_4-C_5, in the opposite direction compared with Mode 1a and 1b. S_7 conducts the sum of two inductor currents, similar to S_8 in Mode 1a as noted in Fig. 3(d). In Mode 3b, C_1 connected to V_g by S_1 conducts $\frac{I_{L1}}{2}$, changing the currents through the other capacitors to $\frac{I_{L2}}{4}$ and, as a result, reducing the current on S_7 by half of I_{L2} stated in Fig. 3(e). Same with Mode 1, switching node voltage v_{x2} is defined by capacitor branch voltages expressed as

$$v_{x2} \approx V_g - V_{C1} = V_{C2} - V_{C3} = V_{C4} - V_{C5} = \frac{1}{6}V_g. \qquad (2)$$

Mode 2 again follows Mode 3 and completes one switching period.

By recognizing the voltages applied to the inductor L_1, the inductor current i_{L1} can be expressed as

$$i_{L1}(t) = I_{L,min} + \frac{\left(\frac{1}{6}V_g - V_o\right)}{L_1}(t - T_o) \qquad (3)$$

in Mode 1a and 1b and

$$i_{L1}(t) = I_{L,max} - \frac{V_o}{L_1}(t - T_{1b}) \qquad (4)$$

in rest of the modes with $T_0 \le t \le T_0 + T_s$. The equation for L_2 can be similarly derived and the two inductors are operated in interleaved manner just like a multiphase Buck converter. It is desirable for high current application since the interleaved inductor operation implies favorable inductor sizing and thus better loss factor compared to single inductor Dickson hybrid converter, which will be discussed further in Section II-B [12].

With the converter operations above, all flying capacitors are soft-charged/discharged by inductor currents without a mode with hard-charging. This is a key benefit of the proposed hybrid converter, promising high potentials for high-power and high-current applications. As flying capacitors achieve complete soft-

TABLE I. AVERAGE MODEL PARAMETER COMPARISON OF DIHC AND DICKSON HYBRID.

	M	DC Output Impedance, R_{out}
DIHC	$\frac{D}{N}$	$R_{out} = D\left(\frac{1}{N}\right)^2\left(\sum_{i=1}^{N} R_{s,i}\right) + \left(\left(\frac{(N-1)^2}{N^2} - \frac{1}{2}\right)D + \frac{1}{4}\right)R_{s,N+1} + \left(\frac{1}{2}D + \frac{1}{4}\right)R_{s,N+2}$
Dickson Hybrid	$\frac{2D}{N}$	$R_{out} = D\left(\frac{2}{N}\right)^2\left(\sum_{i=1}^{N} R_{s,i}\right) + \left(\left(\frac{(N-2)^2}{N^2} - \frac{1}{2}\right)D + \frac{1}{4}\right)(R_{s,N+1} + R_{s,N+3}) + \left(\frac{1}{2}D + \frac{1}{4}\right)(R_{s,N+2} + R_{s,N+4})$

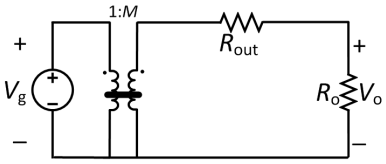

Fig. 5. Average model of a converter with an ideal 1:*M* DC transformer for conversion ratio modulation and a lumped output impedance R_{out} to represent loss factors.

charging, DIHC can significantly reduce capacitor size without increasing switching frequency.

In addition, the inductors can be favorably sized for high power density due to the reduced switching node voltage e.g. $v_{x1,2}$ only switch between $\frac{1}{6}V_g$ and 0 similar to three-level or multilevel topologies [13], [14]. With optimally sized small capacitors and inductors, the DIHC would result in high power density power conversion.

B. DC Characteristic and Inherent Inductor Current Balance

According to voltage-second balance of inductor, DIHC's ideal voltage conversion ratio is defined as

$$\frac{V_o}{V_g} = \frac{D}{N} \tag{5}$$

where N is the number of division (N=6 for the DIHC in Fig. 2), compared to $\frac{V_o}{V_g} = \frac{2D}{N}$ in hybrid Dickson converter, theoretically resulting in 2X larger *D*. That in turn enables DIHC to support larger conversion ratios and relax on-time of high-side switches. Since switching node voltage swing, v_x, is reduced by N times compared to Buck converter counterpart and output capacitor receives interleaved inductor currents, its output filter inductors and capacitor can be significantly reduced for the same output ripple. On the other hand, unlike conventional interleaved Buck converters having inductor current balancing issues, the two inductor currents of DIHC are guaranteed to be balanced, I_{L1}=I_{L2}, by nature because of the flying capacitors' operation. Since periodic charges delivered to L_1 and L_2 are guaranteed to be identical thanks to charge-second balance of flying capacitors in steady state with the same on-time, DT_s, average values of two inductor currents remain same even with different inductance or different resistive components. To be clear, to satisfy charge-second balance of capacitor C_1, the net charge for the capacitor should be zero, that is

$$\int_{T_0}^{T_0+T_s} i_{C1}\,dt = 0. \tag{6}$$

With the analysis in Section II-A and small ripple approximation

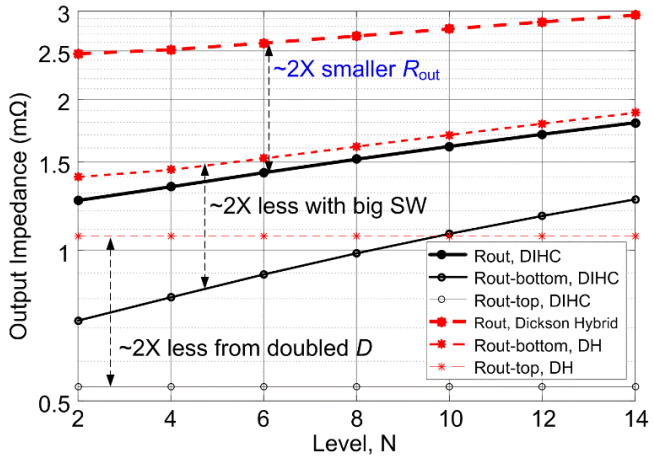

Fig. 6. Output impedance comparison of DIHC to the hybrid Dickson.

$$\int_{T_0}^{T_0+T_s} i_{C1}\,dt = -\frac{I_{L1}}{2}\left(\frac{D_A}{3}T_s\right) - \frac{I_{L1}}{4}\left(\frac{2D_A}{3}T_s\right) + \frac{I_{L2}}{2}\left(\frac{2D_B}{3}T_s\right). \tag{7}$$

As a result, the two inductor current averages are guaranteed to be equal, I_{L1}=I_{L2}, as long as the capacitor charge-balance is satisfied and D_A=D_B which is valid in this even level DIHC.

III. STEADY STATE ANALYSIS OF DIHC

As expressed in the ideal conversion ratio, the DIHC converter will have ~2X longer on-time than a Dickson hybrid and this feature would translates to better switch utilization or reduced conduction loss with same switch and capacitor. To quantitatively evaluate this statement, average models of DIHC and hybrid Dickson converter are derived. Converter average model, shown in Fig. 5, can capture key DC characteristics such as input-to-output voltage conversion ratio incorporating effect of power processing losses and be used to compare different topologies to evaluate figure of merits at different conditions [15], [11]. Therefore, deriving the equations of key loss factors and equivalent output resistance R_{out} for the two converters would help to evaluate the claimed benefits of DIHC.

Since the two converters' switching loss mechanisms are fairly similar without significant difference having two effective turn-on and off time in a period, this paper only characterizes the conduction loss of switches which will be the key factor to drive the converter loss. Identifying current conduction of individual switches illustrated in Fig. 3 and deriving loss equations as a function of output current leads to different coefficients of loss contributions. Table I presents model parameters considering

TABLE II. CIRCUIT COMPONENTS AND PARAMETERS.

Item	Design Selection
Controller	TMS320F28377, Texas Instruments
Switching Freq.	300 kHz
C_1, C_2, C_3, C_4, C_5	2.2, 1.5, 1.5, 1, 1 µF, X7R, 1812/1210, TDK
C_o	6.8 µF, X5R, 0603, 10V, TDK
Inductors, L_1 & L_2	1.5 µH, IHLP-5050CE-01
$S_{1\text{-}6}$	EPC2014C, 40 V, 16 mΩ, EPC
$S_{7\text{-}8}$	EPC2023, 30 V, 1.45 mΩ, EPC
D_7, D_8	CRS08, 30 V, 1.5 A, Schottky with $S_{7\text{-}8}$
Gate Drivers	3 x LM5113, 2 x LM5114
Signal Isolators	Si8422, Silicon Labs

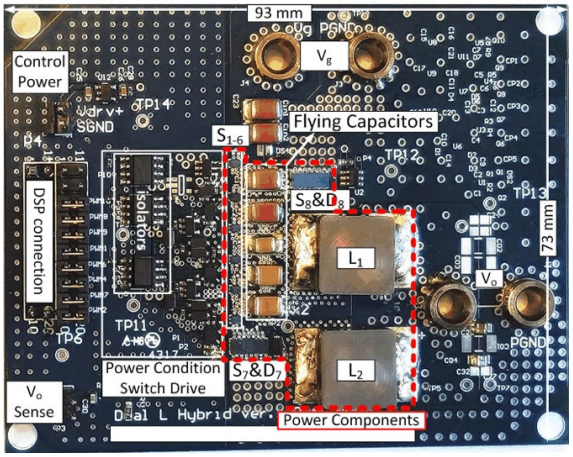

Fig. 7. 6-to-1 dual inductor hybrid prototype.

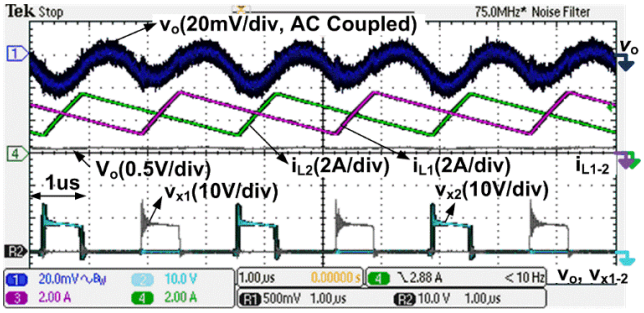

Fig. 8. Operation waveforms of prototype at 48V-1.6V under 5A load.

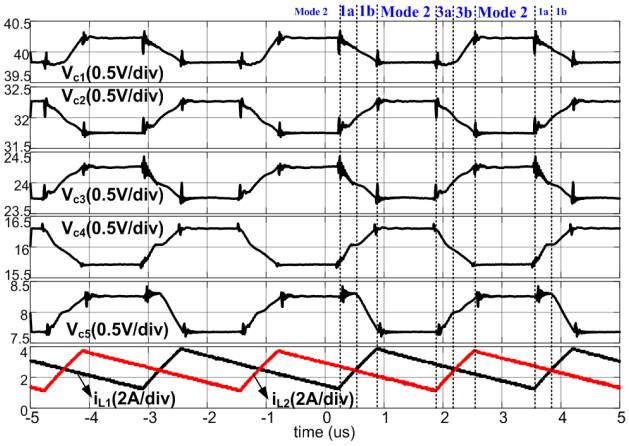

Fig. 9. Flying capacitor voltage waveforms at 48V-1.6V under 5A load.

RMS switch current for the two N-to-1 division converters where $R_{s,i}$ is on-resistance of S_i, which allows one to compare loss contribution of different switches. In both converter average models, switch currents are assumed to conduct constant current (fraction of inductor current) during DT_s.

Fig. 6 illustrates an example set of output impedances with using practical GaN switches in consideration: EPC2014C (40 V, 16 mΩ) for top switches and EPC2023 (30 V, 1.45 mΩ) for bottom switches, i.e. for $S_{1\text{-}6}$ and for $S_{7\text{-}10}$ in 6-to-1 implementation. The analysis shows that DIHC achieves ~2X smaller R_{out} as a result of a combination of 2X longer on-time for top switches (1/2 rms^2 →1/2 loss) and half number of bottom switches, i.e. ~2X less switch conduction loss. This advantage makes DIHC more feasible to applications that require large conversion ratios and high output currents.

IV. EXPERIMENTAL VERIFICATION

To verify the feasibility of the new converter topology, a 20-W 48-V VRM prototype is implemented. The 6-to-1 DIHC prototype is designed based on the developed average model and switch optimization. The printed circuit board implementation with key components is shown in Fig. 7. The component selections and specifications are tabulated in Table II.

The key operation waveforms of prototype at 48V-1.6V/5A condition are shown in Figs. 8 and 9. Comparable to the operation described in Section II and depicted in Figs. 3 and 4, the prototype demonstrates all desirable characteristics. In Fig.

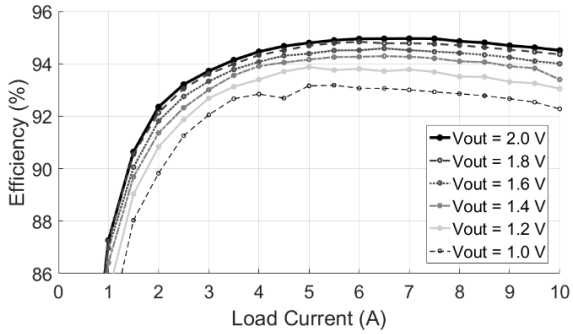

Fig. 10. Measured efficiency at 48-V input with different output voltage.

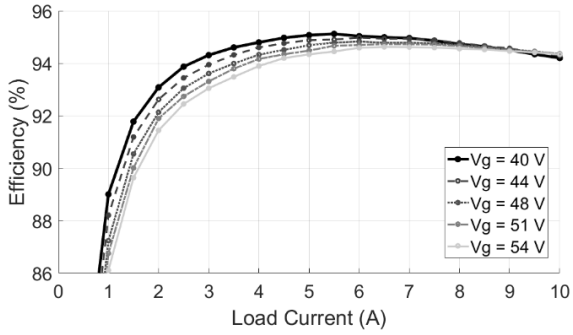

Fig. 11. Measured efficiency at 1.8-V output with different input voltages.

TABLE III. COMPARISON OF DIHC TO DIFFERENT SOLUTION FOR DATA CENTERS.

	This work	Dartmouth [8]	VICOR	CPES [16]	CPES [3]	LMG5200POLEVM
Topology	DIHC	FCML	PRM+VTM	Sigma (DCX|Buck)	LLC+Buck	HB+Current Doubler
Input-Output	48V-1~2V/10A	48V-2V/10A	48V-1.5V/115A	48V-1V/80A	48V-1.8V/120A	48V-1V/50A
Peak Efficiency	95.02%	85%	93%	93.5%	91%	90.7%@20A
# Switches	8 (6-Level)	13 (7-Level)	4+6	12(DCX)+2(Buck)	8(DCX)+2x2(Buck)	2(Pri)+4(Sec)
Capacitors	5(flying)+1(out)	5(flying)+1	1(Cr)+2(HB)+1(out)	1(Cr)+2(output)	1+1(LLC)+2(Output)	2(HB)+1(output)
Inductors/TR	2	1	1(BB)+1(Lr)+1(TR)	1(DCX)+1(Buck)	1(LLC)+N(Buck)	1(TR)+2(Sec)
Passive vol. (mm^3)	1345	2422	-	-	-	1343
Frequency (f_{sw})	300 kHz	83.3 kHz	1 MHz/1.4 MHz	1 MHz/600 kHz	1.6 MHz/1 MHz	600 kHz
Power Density	225 W/in^3	-	-	420 W/in^3	-	-

8 the two interleaved inductor currents are naturally balanced with no need for additional balancing method. Fig. 9 captures the flying capacitor voltages in steady state operation. As expected from the analysis, all capacitors are soft-charging by inductor current and split phase operation without significant voltage jump with hard charging happening in a conventional switched capacitor converters.

Fig. 10 and Fig. 11 display measured efficiency of the prototype converter with different output voltages, 1-2 V, from 48-V input and different input voltages, 40-54 V, for 1.8 V output, respectively. Owing to superior output impedance by reasonable on-time and excellent switch utilization, soft-charging for all capacitors, and interleaving benefits, the converter achieves 95.02% peak efficiency, and 225-W/in^3 power density considering key power conversion components. It is also beneficial the converter efficiency is kept higher than 90% down to 20% load in data center applications where light load efficiency is also important for energy saving.

Table III compares the state-of-the art technologies for 48V-core application highlighting DIHC in superior efficiency, and relatively simple structure (number of active components). Simple operations and increased duty cycle promise high potential to further increase the converter power density with higher switching frequency.

V. CONCLUSION

This paper presented a new hybrid converter using two interleaved inductors for high efficiency and high power density. By streamlining the power conversion structure and, as a result, eliminating two freewheeling switches, the converter achieves ~2X improved output impedance in switch and capacitor conduction losses compared with a hybrid Dickson converter counterpart. Interleaved dual output inductors bring the benefits of multiphase interleaving architecture for high-current applications with naturally balanced inductor currents by the flying capacitors' steady-state operation. A 20-W proof-of-concept prototype verified the converter's desirable operations and characteristics, achieving 95.02% peak efficiency and 225-W/in^3 power density.

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