A Probabilistic Error Model and Framework for Approximate Booth Multipliers

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ABSTRACT

Approximate computing is a paradigm for high performance and low power design by compromising computational accuracy. In this paper, the structure of an approximate modified radix-4 Booth multiplier is analyzed. A probabilistic error model is proposed to facilitate the evaluation of the approximate multiplier for errors from the approximate radix-4 Booth encoding, the approximate regular partial product array, and the approximate 4-2 compressor. The normalized mean error distances (NMEDs) of 8-bit and 16-bit approximate designs are found by utilizing the proposed model. The results from the error model and the corresponding analytical framework are close to those found by simulation, thus confirming the validity of the proposed approach.

CCS CONCEPTS

• **Hardware** → **Hardware test**; **Fault models and test metrics**;

KEYWORDS

Probabilistic error model; approximate multiplier; Booth encoding;

1 INTRODUCTION

As the density of integrated circuits (ICs) continues to increase, power consumption has become one of the main obstacles to attain high performance in a chip. It is becoming extremely difficult to further improve performance and reduce power consumption of digital IC under the requirement of full accuracy. However, in error-tolerant applications related to human perception, such as image processing, pattern recognition and machine learning, it is possible to perform approximate calculations to further improve power and performance [1]. In these cases, computation results do not require absolutely accurate values, and thus, approximate results with appropriate errors are acceptable. Approximate computing has been proposed as a promising paradigm [2], [3] to achieve low power consumption and high performance at the expense of reducing computational accuracy.

The common metrics for error analysis of arithmetic circuits include the error distance (ED), the mean error distance (MED) and the normalized mean error distance (NMED) [5]. However, in most cases the error analysis of approximate arithmetic circuits is based on Monte-Carlo simulation, which is very time-consuming, and unsuitable to analyze large word size designs.

Recently, research has been conducted on error modeling of approximate arithmetic circuits. For approximate adders, [6] proposes qualitative error metrics and a model that links the peak signal to noise ratio (PSNR) and the average error distance based on image processing using approximate adders; [7] proposes a model for an uniform or inhomogeneous length adder. The design of multipliers largely determines the performance of the entire circuit. Compared with an adder, the circuit structure of a multiplier is more complex [4]. [8] studies the error model for a low-power recursive approximate multiplier and proposes a Probability Mass Function (PMF) model to calculate the error which is derived from the basic building blocks. However, the PMF error model is not applicable to the approximate Booth multiplier. In this paper, a probabilistic error model of a state-of-the-art approximate Booth multiplier [9] is proposed by considering its circuit. By using the proposed model, the error for the multiplication results can be obtained quickly through analysis, which facilitates the evaluation of the approximate Booth multiplier in error-tolerant applications.

The paper is organized as follows. Section 2 reviews the structure of approximate Booth multipliers. The probabilistic error model of the approximate Booth multipliers is presented in Section 3. Simulated and analytical results are provided and compared in Section 4. Section 5 concludes the paper.

2 APPROXIMATE BOOTH MULTIPLIER

The approximate Booth multiplier analyzed in this paper is based on [9] and [10]; the approximate compressors are only used in [10]. As mentioned previously, the approximate Booth multiplier consists of three parts: the Booth encoder, the compressor and the final fast adder. Therefore, the Booth

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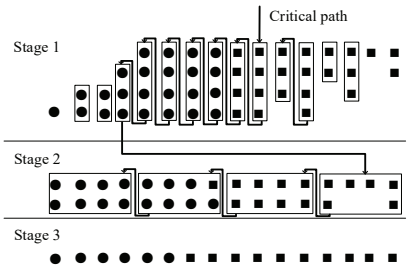

Figure 1: An 8-bit approximate Booth multiplier with p=8.

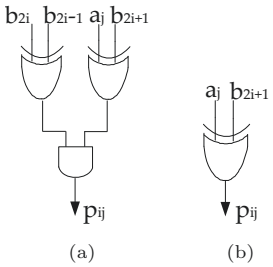

Figure 2: Gate level circuit of: (a) ABE-1, and (b) ABE-2 [9].

encoding, the partial product (PP) array and the 4-2 compression can be approximately designed. An 8-bit approximate Booth multiplier with an approximation factor, *i.e.* p=8 is shown in Fig.1, where $\leq$represents the exact partial products, and ■ represents the inexact partial product.

2.1 Approximate Booth Encoding

Booth encoding plays an important role in the design of a high-performance multiplier. It efficiently generates the PPs by reducing the number of rows and PPs by half. The PP of an accurate Booth encoding is given by:

$$\begin{aligned} pp_{ij} =&(b_{2i} \circ\ b_{2i-1})(b_{2i+1} \circ\ a_j)+ \\ &\overline{(b_{2i} \circ\ b_{2i-1})}(b_{2i+1} \circ\ b_{2i})(b_{2i+1} \circ\ a_{j-1}) \end{aligned} \tag{1}$$

Two designs of an approximate Booth encoder, namely ABE-1 and ABE-2, are proposed in [9]. Fig. 2 shows the gate level circuits of these approximate Booth encodings.

The functions of the approximate Booth encoding ABE-1 and ABE-2 are shown as Eq. (2) and (3), respectively.

$$app_{ij1} = (b_{2i} \circ\ b_{2i-1})(b_{2i-1} \circ\ a_j) \tag{2}$$

$$app_{ij2} = a_j\overline{b_{2i+1}} + \overline{a_j}b_{2i+1} = b_{2i+1} \circ\ a_j \tag{3}$$

2.2 Approximate Regular PP Array

After the Booth encoding, a PP array of N/2+1 rows is generated. There is a symbol for the compensation bit in the last line denoted by Neg. The compensation bit is omitted

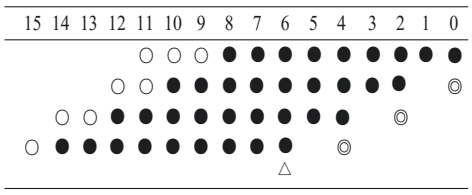

Figure 3: A conventional 8⋄ 8 MBE PP array.

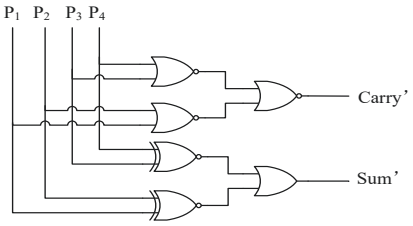

Figure 4: Gate level circuit of an inexact compressor [11].

to convert it into a regular PP array. Fig. 3 shows the conventional 8⋄ 8 modified Booth encoding (MBE) PP array, where $\leq$denotes the pp_{ij} term, • denotes the sign extension term, ◎ denotes the Neg term and { is the ignored Neg term.

The approximate PP array omits the compensation bit in the last line to make the array regular, to reduce the number of rows of the array and the delay of the PP accumulation.

2.3 Approximate Compressor

The 4-2 compressor proposed in [11] consists of two full adders; the approximate compressor omits two parameters: the input variable C_{in} and the output variable C_{out}. Approximate outputs are available as *Sum'* and *Carry'*. The gate-level circuit of an approximate compressor is shown in Fig. 4 with four inputs: P_4, P_3, P_2, and P_1. The logic expressions of the approximate 4-2 compressor are as follows:

$$Sum' = \overline{(P_1 \circ\ P_2)} + \overline{(P_3 \circ\ P_4)} \tag{4}$$

$$Carry' = \overline{\overline{P_1 + P_2} + \overline{P_3 + P_4}} \tag{5}$$

2.4 Error Metrics

The error characteristics of the entire approximate Booth multiplier must be considered. For approximate designs, several metrics have been proposed [5] to measure the error of approximate adders and multipliers, including the error distance (ED), the mean error distance (MED) and the normalization of MED (NMED); these figures of merit are given as follows:

$$ED = \ A \quad A' \tag{6}$$

$$MED = \sum_{i=0}^{n} \frac{ED}{n} \tag{7}$$

$$NMED = \frac{MED}{MAX_{output}} \tag{8}$$

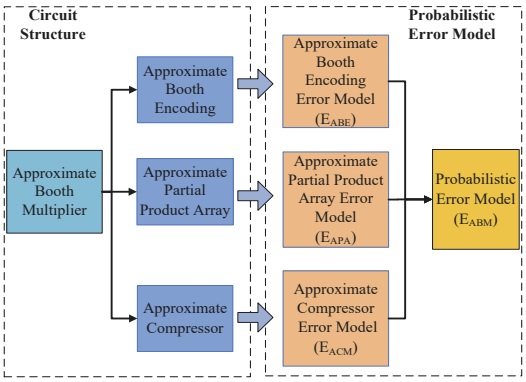

Figure 5: The probability error model based on the circuit.

where, A is the exact value , A' is the approximate value, n is the number of product results, and MAX_{output} is the maximum value of error.

3 PROBABILISTIC ERROR MODEL OF ABMS

The probabilistic error model for the approximate Booth multipliers (ABMs) is proposed in this section. The error model consists of few sub error-models in which each multiplication stage is modeled separately. A sub error-model is based on the structure of the multiplier circuit. The relationship between the circuit structure and the error model is shown in Fig. 5. The error of the entire ABMs (*i.e.*, E_{ABM}) is divided into three parts: the error from the approximate Booth encoding (*i.e.*, E_{ABE}), the error from the approximate regular product array (*i.e.*, E_{APA}) and the error from the approximate 4-2 compressor (*i.e.*, E_{ACM}).

3.1 Approximate Booth Encoding Error Model

The error in the ABEs is generated when a '1' is replaced by a '0' and a '0' is replaced by a '1' in the truth table. The ABEs can produce both positive and negative errors. T_{1-0}=1 denotes the error when a '1' is replaced by a '0' and T_{0-1}=1 denotes the error when a '0' is replaced by a '1'. The accurate PP is obtained by considering the error when using the approximate encoding ABE-1, so

$$pp_{ij1} = (b_{2i} \circ\ b_{2i-1})(b_{2i-1} \circ\ a_j) + T_{1-0} \tag{9}$$

Similarly, the probabilistic error model for the approximate encoding ABE-2 is proposed as

$$pp_{ij2} = b_{2i+1} \circ\ a_j + T_{1-0} + T_{0-1} \tag{10}$$

Changing a '0' to a '1' in the K-map of the ABE causes the approximate result to be higher than its exact counterpart. Therefore, the difference between the exact and the approximate results is negative. However, changing a '1' to a '0' makes the approximate result smaller and the difference between them is positive. Since the outcome of ED is an absolute value, the error of both approximate encoding methods is the same.

Table 1: ED and MED of Approximate Booth Encoding

Encoding	Error Pattern	ED	MED
ABE-1	T_{1-0}	4	0.125
ABE-2	T_{1-0} , T_{0-1}	4	0.125

Table 2: Q and E_{ABE} of Approximate Encoding

Encoding	Q_{0-1}	Q_{1-0}	E_{ABE}
ABE-1	0	4	0.03125
ABE-2	6	2	0.01563

Table 3: Error of PP Array

ED	MED	E_{APA}
3	0.375	0.125

By using the proposed probabilistic error model, the errors resulting from the two approximate Booth encoders are shown in Table 1. The ED in the approximate Booth encoding is the changed value in the truth table. For example, for ABE-1, the change in the K-map is T_{1-0}; therefore, the changed value is positive and the number is 4. For ABE-2, the change in the K-map is either T_{1-0} or T_{0-1}. The value of T_{1-0} is positive and the number is 2, while the value of T_{0-1} is negative and the number is 6, so the result is -4. However, as the ED is an absolute value, the value is finally 4.

A new parameter is utilized for the error model: a value for the approximate Booth encoding is used to represent the number of T_{1-0} and T_{0-1} denoted as Q; Q_{0-1} denotes the number of T_{0-1} and Q_{1-0} denotes the number of T_{1-0} as shown in Table 2. Q is the general name of both Q_{0-1} and Q_{1-0}. In the equation, Q represents the sum value of Q_{0-1} and Q_{1-0}.

When considering the NMED, the new parameter Q is added, and the error of the Booth encoding generated at E_{ABE} is modeled as:

$$E_{ABE} = \frac{NMED}{Q} = \frac{MED}{Q \times MAX_{output}} \tag{11}$$

3.2 Approximate PP Array Error Model

After encoding, a PP array is generated, whose last row is only a compensation bit. The error arises from omitting the sign bit; so, the error caused by omission is expressed as follows:

$$Neg = b_{2i+1}(\overline{b_{2i}} + \overline{b_{2i-1}}) = b_{2i+1}\overline{b_{2i}b_{2i-1}} \tag{12}$$

As 2i+1=N-1, i=N/2-1. Hence,

$$Neg = b_{N-1}\overline{b_{N-2}b_{N-3}} \tag{13}$$

Table 4: Partial Truth Table of Approximate Compressor

P_4	P_3	P_2	P_1	E
0	0	0	0	-1
0	0	1	1	1
1	1	0	0	1
1	1	1	1	1

Table 5: Error of Approximate Compressor

ED	MED	E_{ACM}
3	0.1875	0.046875

This value is utilized for the following objective: when its value is 0, the encoding is consistent with the original code; when its value is 1, the encoding is negative, so complemented. Therefore, when the error is 1, the results appear to be inaccurate and occur only at the three highest bits; as a result, the PP array error, E_{APA}, is given as in Table 3. The ED of the approximate partial product array has a non-zero value when Neg is equal to 1 and E_{APA} is the value that the MED is divided by the number of occurrances when the logic expression of the error is equal to 1.

3.3 Approximate Compressor Error Model

The approximate 4-2 compressor omits two parameters: the input C_{in} and the output C_{out}. For an inexact output, the error E is given by

$$\begin{aligned} E + \overline{(P_1 \circ\ P_2)} + \overline{(P_3 \circ\ P_4)} + (\overline{\overline{P_1 + P_2} + \overline{P_3 + P_4}}) \\ = Sum + Cout + Carry \end{aligned} \tag{14}$$

Table 4 shows the partial truth table with an error value of 1; the error E_{ACM} generated by the approximate compressor is shown in Table 5. The ED in the approximate compression is the sum of E. The error value is the MED divided by the number of occurrances when the absolute value of E is equal to 1.

Thus, the sub error-models based on the design have been formulated and are used to establish the model for the approximate Booth multiplier. The error characteristics of the Booth encoding, the PP array and the tree compression have been presented and for each, the corresponding error parameter NMED can be found; next the error model of the approximate Booth multiplier is established by combining the sub error-models.

3.4 Probabilistic Error Model of ABMs

Among the four designs, ABM1 and ABM2 use an approximate Booth encoding and a regular partial product array. They are referred to as single designs [9]. The error of an ABM increases exponentially, as related to the number of bits of the multiplier operand, *N*. The error of the exponent is given by $log_2\ N\text{-}1$. The error model is generated by combining the above presented sub error-models into a single (design) error model (*i.e.*, E_{ABM-S}), which denotes the error of approximate Booth multipliers with approximate Booth encoders and approximate PP array; this error is given by

$$\begin{aligned} E_{ABM-S} = k_i\}[\frac{1}{N}(E_{ABE}\frac{[(N/2+1)\times 2 \quad Q]Q}{(N/2+1)\times 2})]^{\log_2 N-1} p \\ + (E_{APA}/N)^{\log_2 N-1} \times p/2| \end{aligned} \tag{15}$$

where, k_i=p_i/p_{i-1}. If $p_i/p_{i-1} \Leftarrow 1.5$, k_i=k_{i-1}+1. p is an approximation factor that denotes the number of approximate radix-4 Booth encoding units used in the design of the approximate multiplier.

Compared with a single design (E_{ABM-S}), the so-called composite designs (*i.e.*, ABM3 and ABM4) also utilize approximate 4-2 compressors [10]. The error model for a composite design (*i.e.*, E_{ABM-C}) is given by

$$E_{ABM-C} = k_i(E_{ABM-S} + \frac{1}{N}{E_{ACM}}^{\log_2 N-1}) \tag{16}$$

The proposed approach to calculate the probabilistic error model of the ABMs based on the sub error-models is shown in Algorithm 1.

Table 6: Four Designs of Approximate Booth Multiplier(♦ denotes a used unit, while ⊕denotes an unused unit)

Multiplier	ABE-1	ABE-2	Array	Compressor
ABM1	♦	⊕	♦	⊕
ABM2	⊕	♦	♦	⊕
ABM3	♦	⊕	♦	♦
ABM4	⊕	♦	♦	♦

4 RESULTS

The difference between the values obtained by the error model and simulation is investigated for the four approximate Booth encoded multipliers at different values of p. For simulation results, all designs are described at gate-level in Verilog HDL and verified by Synopsys VCS [9]. There are different modules in the four approximate multipliers, and the analysis of the model must calculate the error for each module (Table 6).

Table 7 provides the NMED comparison between the simulation and analytical results for the 8-bit ABMs; it lists four different ABMs. Among them, p has a value in a range from 4 to 14. The error values grow very fast, almost exponentially with an increase of p. The error of a single design (ABM1, ABM2) is smaller compared to a composite design (ABM3, ABM4), because the single design only contains the approximate Booth encoding module and the approximate partial

Table 7: NMED Comparison of 8-Bit ABMs between Simulated and Analytical Results using Error Model (p is from 4 to 14 and the order of magnitude is 10^{-2})

Multiplier	p	4	6	8	10	12	14
ABM1	**simulated**	0.082	0.137	0.427	1.269	3.369	7.022
	analytic	0.08398	0.12598	0.37794	1.13382	3.40146	6.80292
ABM2	**simulated**	0.076	0.104	0.409	1.4	4.089	10.138
	analytic	0.06445	0.09668	0.29004	0.87012	2.61036	7.83108
ABM3	**simulated**	0.082	0.137	0.607	2.447	9.827	20.871
	analytic	0.11145	0.16715	0.50145	2.00581	8.02324	24.0697
ABM4	**simulated**	0.076	0.162	0.598	2.377	9.778	17.24
	analytic	0.09193	0.13789	0.41369	1.65474	8.2737	15.5474

Table 8: NMED Comparison of 16-Bit ABMs between Simulated and Analytical Results using Error Model (p is from 8 to 20 and the order of magnitude is 10^{-4})

Multiplier	p	8	10	12	14	16	18	20
ABM1	**simulated**	0.2547	0.2557	0.3082	0.9303	3.1026	12.295	46.134
	analytic	1.2373	1.546625	1.85595	2.165275	2.574027	10.28611	51.48054
ABM2	**simulated**	0.2545	0.255	0.2671	0.6243	3.0173	11.241	40.973
	analytic	1.1471	1.4333	1.71995	2.0071	2.2932	9.17306	45.8653
ABM3	**simulated**	0.2616	0.2957	0.3423	1.4043	5.6545	24.106	98.903
	analytic	1.88103	2.35129	2.82155	3.29181	3.76207	18.81032	112.86192
ABM4	**simulate**	0.2676	0.315	0.4632	1.6014	4.1534	22.402	91.853
	analytic	1.79083	2.23854	2.68625	3.13395	3.58166	17.9083	107.4498

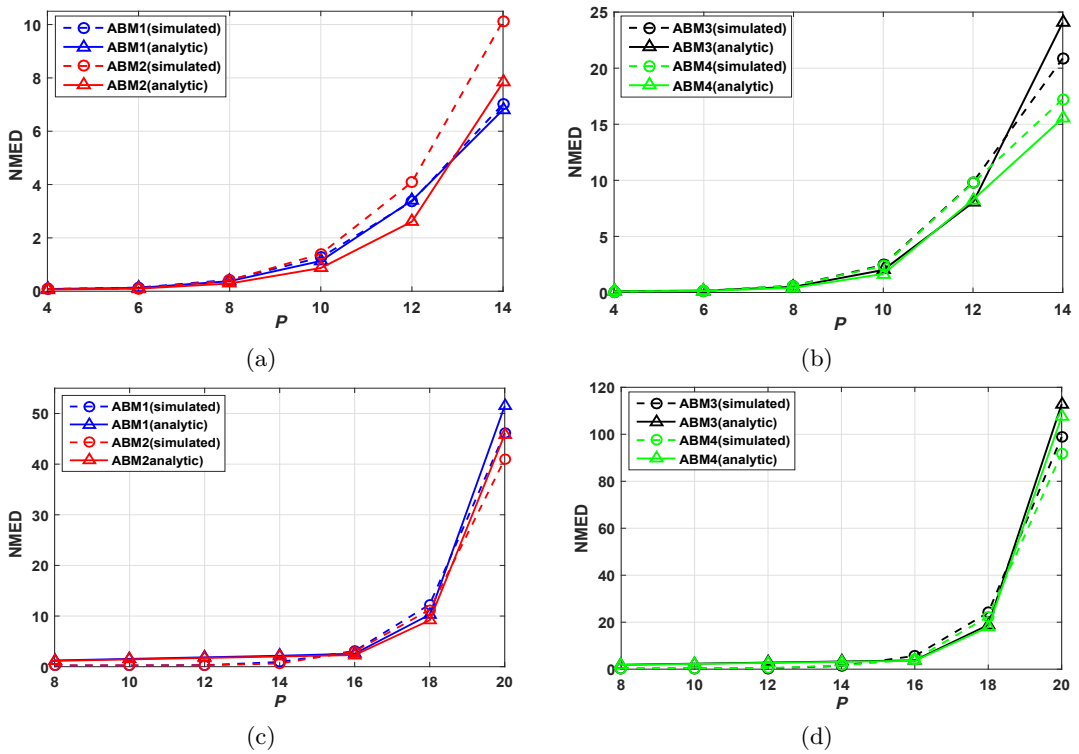

Figure 6: Simulated and analytical NMED values for ABM: (a) 8-bit ABM by E_{ABM-S}, (b) 8-bit ABM by E_{ABM-C}, (c) 16-bit ABM by E_{ABM-S}, (d) 16-bit ABM by E_{ABM-C}.

Algorithm 1 Probabilistic Error Model.

Require:
Bits of the multiplier operand, N;
Approximate factor, p; Operands, b_i, a_j;
Modification of K-Map, T;
Number of the Error in K-Map, Q;

Ensure:
Probabilistic Error Model of ABMs, E_{ABM}

1: **Define:** Probabilistic of the value "1" of logic expression [P(x)];
%Based on circuit structure to analyze sub-model
2: $E_{ABE} \triangle$ P(T)/Q, 1 $\triangle$ 0 and 0 $\triangle$ 1 denoted as T;
%The error model of ABE, *i.e.* E_{ABE};
%The logical expression of T, *i.e.* Eq. (9) and (10);
3: $E_{APA} \triangle$ P(G),
G: the last symbol compensation bit Neg;
%The error model of approximate partial product array, *i.e.* E_{APA};
%The logical expression of G, *i.e.* Eq. (12);
4: $E_{ACM} \triangle$ P(E), E: the difference between exact compressor and approximate compressor;
%The error model is approximate compressor, *i.e.* E_{ACM};
%The logical expression of E, *i.e.* Eq. (14);
5: **Define:** Function of error model [F(x)];
6: **for** the sub-model **do**
7: $E_{ABM-S} \triangle$ F(N, p, Q, E_{ABE}, E_{APA});
8: $E_{ABM-C} \triangle$ F(N, p, Q, E_{ABE}, E_{APA}, E_{ACM})
9: **end for**
%The probabilistic error function expression of E_{ABM-S} and E_{ABM-C}, *i.e.* Eq. (15) and(16);
10: **return** E_{ABM};

product array module, while the composite design also uses the approximate compressors.

Fig. 6(a) and Fig. 6(b) show plots of the NMED (the analytical value from the proposed model and the simulated value) versus p for 8-bit ABMs, respectively, which are denoted as E_{ABM-S} and E_{ABM-C}, respectively. The analytical values are very close to the simulated values and the model for the ABM1 has the best estimate. Generally, the analytical error value is smaller than the simulated value.

The NMED comparison for the 16-bit designs has similar results as the 8-bit designs. The value of p is in a range from 8 to 20 as shown in Table 8. The difference between the simulated and the analytical values is marginally larger when p is less than 14, because the NEMD values grow faster by simulation than the exponential model assumption. When p>14, the analytical results are close to the simulated results.

As shown in Fig. 6(c) and Fig. 6(d), for the 16-bit ABMs, when p becomes larger, the NEMD values increase exponentially. The model of a simple design shows slightly better results than the composite one for 16-bit designs.

5 CONCLUSION

This paper has presented a probabilistic error model for approximate Booth multipliers (ABMs). The error model of the ABMs has been formulated by taking into account each part of the overall multiplier structure and then combining them to form a complete analytical framework. Each proposed sub error-model has been established based on the circuit structure in every approximate unit of the designed multiplier, such as for the approximate Booth encoding, the approximate PP array and the approximate compression; finally the model combines them analytically. This framework has provided the results for one of the most important error metrics (*i.e.*, NMED). This analytical model can also be used for a fast yet mostly accurate assessment of the ABMs. The results have shown that, for 8-bit designs, the probabilistic error model for ABM1 achieves the best results. The analytical NEMD values are generally smaller than the simulated results; for 16-bit ABMs, the model for the simple design is better than the composite design with approximate compressors.

Future work will investigate the impact of the input distribution for a more generalized analysis. The model will also be applied to other approximate multipliers such as approximate redundant multipliers and consider the relationship between the NMED and different application metrics, such as the PSNR in image processing.

6 ACKNOWLEDGEMENTS

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