

A Flexible Phased-Array Architecture for Reception and Rapid Direction-of-Arrival Finding Utilizing Pseudo-Random Antenna Weight Modulation and Compressive Sampling

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Abstract—The direct space-to-information converter (DSIC) unifies conventional delay-and-sum analog conventional beamforming (CBF) with compressive sampling (CS) rapid direction-of-arrival (DOA) finding into a single, reconfigurable phased-array receiver architecture. Where current CBF-based DOA scanners need to exhaustively search through multiple DOA angles, the DSIC is able to receive energy from all possible angles by modulating its antenna weights pseudo-randomly. The DSIC RF-ASIC can operate from 1 to 3 GHz, was fabricated in 65-nm CMOS, and includes eight direct-conversion paths each delivering 32-dB conversion gain, 3.3-dBm in-band IIP3, and 6.4-dB NF while consuming 19.8 mW from 1.2 V. The DSIC RF-ASIC has two modes of operation, CS-DOA and CBF-Reception and can switch between them in less than 1 μ s. In CS-DOA mode, the DSIC RF-ASIC finds the DOA of a single signal in 1 μ s consuming 158 nJ which is 4x faster and 1.5x less energy than a comparable CBF-based DOA scanner.

Index Terms—Angle of arrival, compressive sampling (CS), direction of arrival (DOA), phased arrays, sub-Nyquist.

I. INTRODUCTION

THE rapidly growing wireless connectivity demand for people and machines is leading to an increasingly congested electromagnetic frequency spectrum. The angle space has become an important resource to address this congestion. However, the current paradigm of pre-allocating frequency and angle resources for use by designated classes of devices will no longer be sufficient to guarantee access to all. Advances in cognitive radio (CR)-based dynamic shared medium access (DSMA) systems will force us to rethink the radio transceiver. Future terminal devices will need to rapidly gain awareness of their fast-changing ambient environment and opportunistically gain access to a shared pool of resources in the frequency-angle plane. Rapid and

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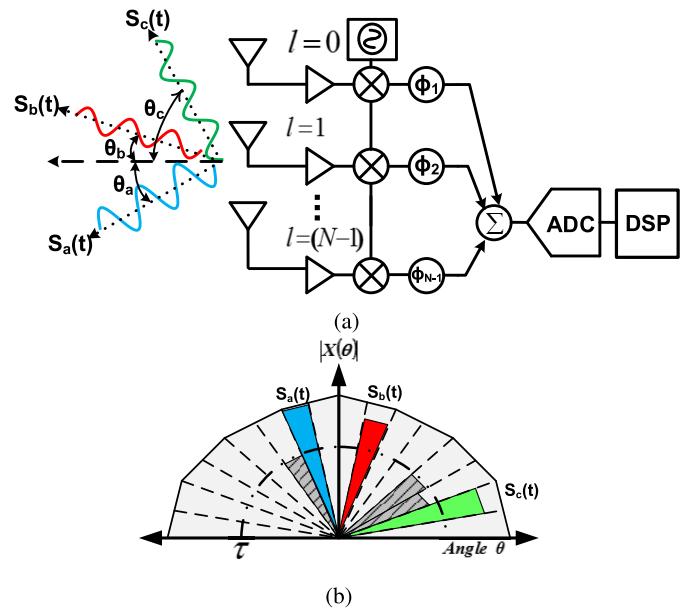


Fig. 1. (a) CBF phased array with N elements can receive in one direction at a time. (b) Using a sequential scan, the CBF receiver finds, e.g., six signals, but only $K = 3$ signals break a threshold τ .

energy-efficient direction-of-arrival (DOA) finders and spectrum scanners are key to enabling future ambient-aware CR-DSMA terminals. Current DOA scanning methods fall into three main categories—analog or conventional beamforming (CBF), as shown in Fig. 1(a), digital beamforming, and multiple-input multiple-output (MIMO) methods. There are also combinations of these methods known as “hybrid beamforming,” i.e., a combination of analog and digital beamforming. The CBF is a popular method due to its ability to function in an interferer-rich environment by spatially filtering unwanted signals, as shown in Fig. 1, and its ease of implementation. Recently proposed radio frequency integrated circuits (RFIC) designs perform CBF in the analog domain since it only requires a single set of I/Q baseband outputs and ADCs per signal of interest (SOI) [1]–[3].

However, the CBF’s ability to scan quickly for multiple SOI’s is limited. The CBF must scan the spatial

environment trading off the number of antennas in the array and scan time linearly that possibly limits its scalability. MIMO techniques have been used to speed up the search process at the cost of significantly increasing hardware complexity by introducing multiple I/Q paths. This allows the system to find more SOI's per scan or scan faster by partitioning the field of view (FoV) in a hierarchical manner [4], [5]. Hierarchical scans that broaden the antenna pattern might require less scan time than an exhaustive swept search but have a number of issues that make implementation less attractive. Broader patterns often have sidelobes that are difficult to control and substantial unwanted signal energy can enter into scan sectors [6]. Finally, hierarchical scans exhibit decreased detection sensitivity and, therefore, higher mis-detection probabilities. In realistic channel environments, exhaustive scans are typically still preferred [7]–[9]. Precoding techniques have been proposed to find mobile units [10] but require a coding circuit to be implemented on both the array used for DOA finding and the emitter making them unsuited for detection of unknown signals.

Interferer-rich environments are often *sparse* in the *angle space*. Fig. 1(b) illustrates a polar plot depicting the directions of six incident interfering signals from six unique directions in the angle space. When compared to a threshold τ , only three signals from three directions remain out of 16 possible directions. Therefore, the angle space is *sparse* since the number of incident signals K after thresholding is $K \ll N$, where N is the number of possible directions, which for a CBF is typically equal to the number of antennas in the array.

For sparse sensing problems, compressive sampling (CS) offers a technique to find signals with fewer “compressed” samples compared to traditional sampling approaches [11]. CS-based approaches have been proposed that reduce the number of active antennas with the goal of reducing the overall number of downconversion paths in use, while keeping the array aperture constant and the scan resolution high [12]. In [13] and [14], a CS beamforming approach is compared to MIMO-based methods, such as MUSIC and ESPRIT [15], [16]. However, such methods require at least $K - 1$ downconversion paths, where K is the number of signals, as well as an estimate of the antenna covariance matrix.

In [12] and [18], CS was used to locate targets using a large array and an MIMO-based architecture; implementation of this architecture on a chip would still require many elements, as well as separate ADCs for each downconversion path.

In [17], a parallel CS architecture for DOA finding was proposed, where a separate receive path is used for each CS measurement as shown in Fig. 2(a). For instance, to obtain m CS measurements in an N -antenna receiver, $m \cdot N$ receive paths would be required. For example, four measurements in an eight-channel receiver would require 32 receivers. This leads to a few severe design problems, the greatest being excessive circuit complexity as antennas are added, limited operational frequency due to large loading, and a very large chip area.

In [19]–[21], wideband spectral scans for signal detection are performed using CS techniques. The pseudo-random noise (PN) modulation of a receiver's local oscillator (LO) signal [21] can be used to compress a wideband spectral scan

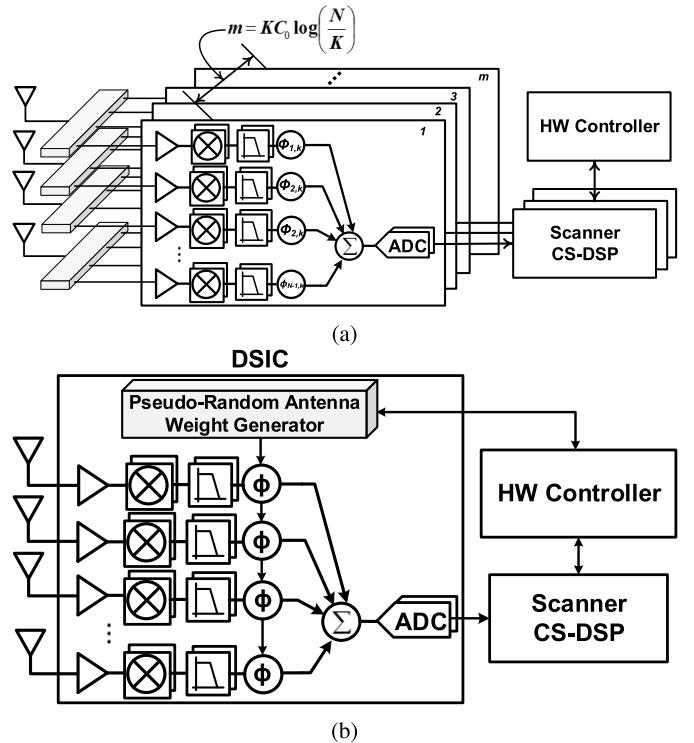


Fig. 2. (a) Fully parallel CS-based phased array where $m \cdot N$ receive paths are needed to obtain m measurements at once [17]. (b) Proposed DSIC CS-DOA architecture where only N antenna paths are needed, and m measurements are obtained consecutively through time segmentation.

into a small, single channel bandwidth to perform spectral scanning in the frequency domain. In [22], it is shown that for DOA finding, it is possible to also use PN modulation techniques and custom PN sequences to gather energy from signals in all directions using *composite antenna patterns* which are then used with CS to find signals in the angle space.

We present a direct space-to-information converter (DSIC) that unifies a delay-and-sum CBF with rapid, compressive-sampling DOA finding into a single, reconfigurable, and scalable receiver array architecture [23]. The DSIC is able to take CS measurements in a *time-segmented* manner eliminating the need for additional receivers to implement CS, beyond those already needed for a CBF, resulting in a unified phased-array architecture [Fig. 2(b)]. The DSIC operates in two modes; *CBF-Reception mode* where it functions as a CBF-based receiver and *CS-DOA Mode* where it performs rapid and energy efficient DOA scans. Unlike [17], the number of CS measurements is flexible and can be varied dynamically without the need to modify the CBF-based architecture assuming the input signal remains stationary over the measurement timeframe. In addition, the DSIC is able to perform DoA scans over the entire FoV using only a single bit of resolution in its vector modulators (VMs). Finally, the requirements posed on the DSIC's off-chip digital baseband section are not at all different than that of a CBF, making system integration less demanding. This paper is organized as follows. Section II describes the theory of operation of the DSIC. Analysis of the progressive phase relationship across antennas and how it pertains to the DSIC's operation is also discussed. Next,

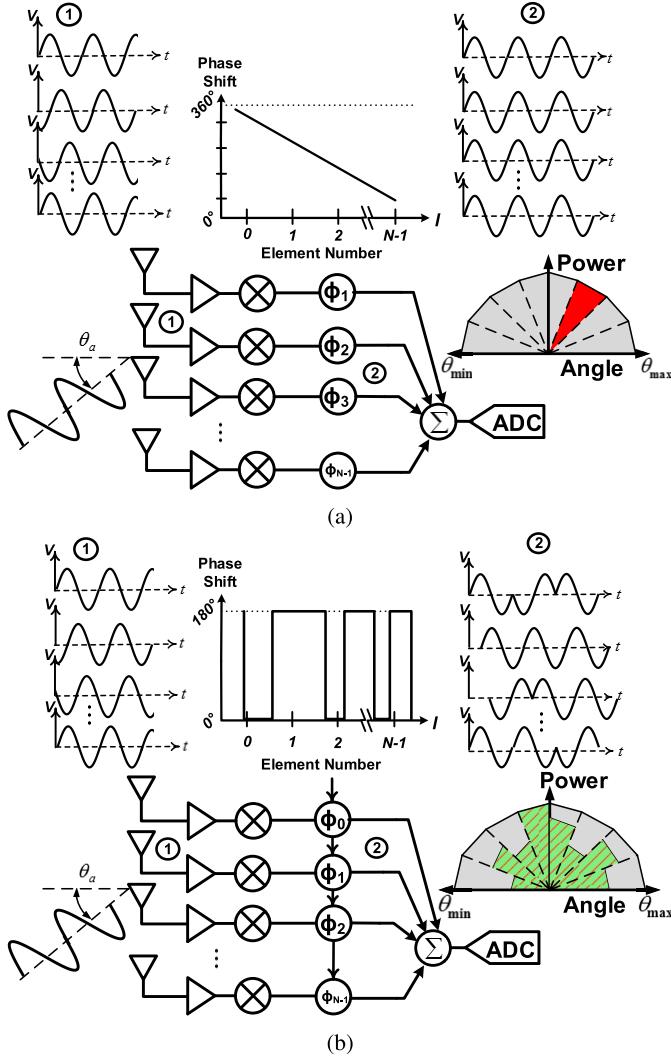


Fig. 4. (a) Operation of the CBF: the phase shifts in the RF signals (1) are compensated (2) with a linear phase profile, and a constructive addition is obtained for one particular direction. (b) Operation of the DSIC: with a pseudo-random phase profile, the array receives energy from all directions with an angular gain profile determined by the PN sequence.

results in the angular spectrum as shown in (8). This is similar to a discrete Fourier transform (DFT) operation performed on the antenna elements \mathbf{x} and sampled at a rate of d , an angle bin-width of $\Delta_{3dB} = (\lambda/N \cos(\theta))$ and N number of unique DOAs [26].

1) *Scanning in CBF-Reception Mode*: Fig. 4(a) illustrates that a CBF must scan all possible directions to determine the DOA of all possible signals. At **point 1**, $\mathbf{x}[n]$ is shown across antenna elements; the phase shifters across elements; $\phi_1, \phi_2 \dots \phi_{N-1}$ have a linear phase relationship as shown in (6). This results in **point 2**, coherently combined downconversion paths and a power versus angle depiction of incident power being received at a single DOA angle.

2) *Energy Consumption for a Scan*: The scan time per DOA angle for a CBF is $t_{\text{detect}} = t_s n_s$ where n_s is the number of samples used by the ADC, and t_s is the sampling period. The total scan time for all N unique DOAs is $t_{\text{scan}} = N \cdot t_{\text{detect}}$. Therefore, the total energy consumption of a CBF is (9) where

P_{ant} is the power consumption for each antenna path

$$E_{\text{CBF}} = N^2 t_{\text{detect}} P_{\text{ant}}. \quad (9)$$

The swept CBF scanners suffer from an inherent tradeoff between the number of antenna elements and scan time. For swept CBF scanners with constant sensitivity, the energy consumption for a complete spatial scan scales quadratically with the the number of antennas since there are N antennas and N possible DOAs.

For the DSIC, *CBF-Reception mode* is only used for *reception* of signals once the SOI is found via scanning in a much faster and efficient *CS-DOA mode*.

C. Rapidly Sensing the Angle Space in CS-DOA Mode

In [19]–[21], CS measurements are used for recovering the spectral locations of signals. The DSIC uses a similar approach but instead of creating measurements in the frequency spectrum, it creates measurements in the angle space for recovery of DOAs.

1) *Compressed Sensing*: It has been shown that it is possible to detect signals with fewer random measurements than are required by a Nyquist-rate-based system [11]. For a vector $\mathbf{x} \in \mathbb{C}^N$, where $\mathbf{x} = \Psi \mathbf{X}$, Ψ is the $N \times N$ dictionary matrix and \mathbf{X} is an $N \times 1$ vector with $K \ll N$ non-zero entries, with K the number of signals, CS theory shows that the angular spectrum, \mathbf{X} can be recovered using m linear projections on to a $m \times N$ sensing matrix Φ that is incoherent with Ψ [27]. The DSIC system equation can be written as $\mathbf{y} = \Phi \Psi \mathbf{X}$

$$m = K C_0 \log \left(\frac{N}{K} \right) \text{ where } 2 \leq C_0 \leq 4. \quad (10)$$

Recovery of \mathbf{X} can be performed by a multitude of algorithms. For this paper, we used *orthogonal matching pursuit* (OMP) due to its simplicity and efficiency for highly sparse problems as shown in [28].

2) *Composite Gain Patterns*: For the DSIC in *CS-DOA mode*, the matrix Ψ rows are equivalent to the conjugate transpose \mathbf{w} , each corresponding to a different angle θ and \mathbf{X} is the spectrum of the signal vector across elements where each element of \mathbf{X} corresponds to incident signal power at a particular angle θ .

CS theory allows the DSIC to calculate the DOAs of \mathbf{x} using fewer scan sectors and, hence, less time than dictated by (8) by using m random mixtures of antenna branches called *composite antenna patterns* [27], [28].

The DSIC instantaneously senses signals from all directions by PN modulation of the phase shifters. It does this by using a custom Rademacher based, PN sequence $P_l(i)$ of length N , where $i \in [1, m]$ indicates the PN sequence index and $l \in [0, N - 1]$ is the antenna number. Similar to work done in the spectral domain, while the DSIC only uses Rademacher PN sequences for this paper, other types of sequences could be used [19]. Each PN sequence corresponds to a row in the CS sensing matrix Φ . By PN modulating the phase shifter phases, the phase shifter weight vector \mathbf{w} no longer has a linear phase relationship between antenna elements. This can be shown in Fig. 4(b) where the DSIC's phase relationship

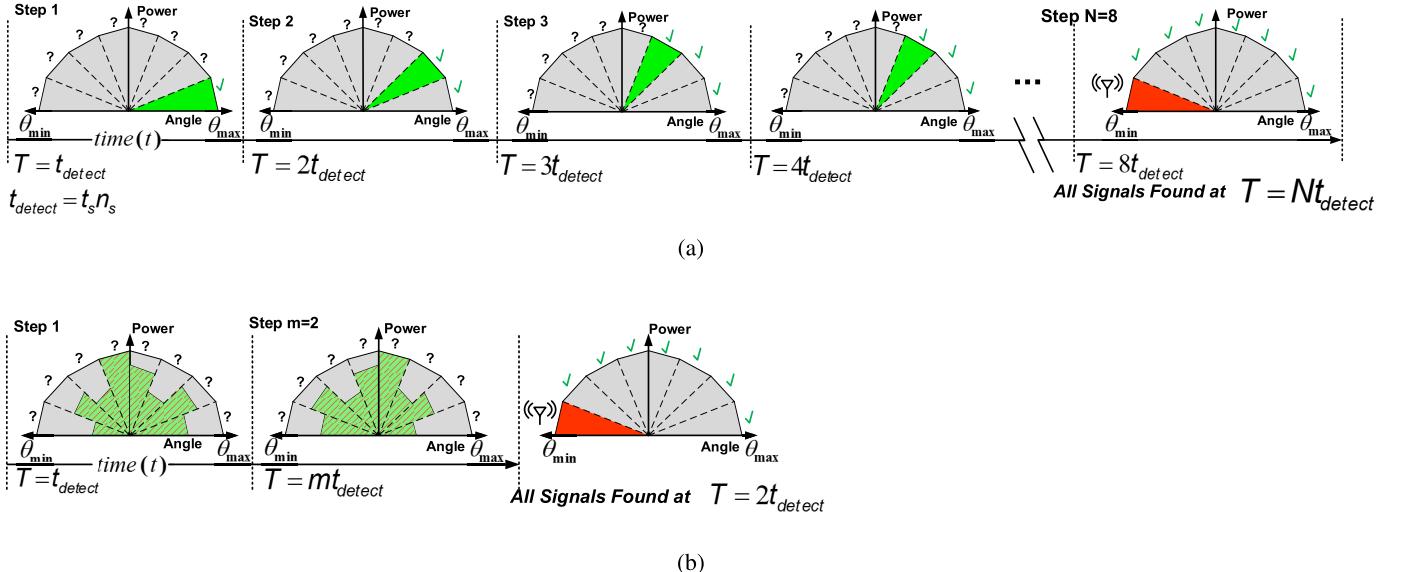


Fig. 5. (a) Traditional CBF finds the DOA of a SOI by performing a sequential scan of all N angles. (b) DSIC only takes m composite measurements to find the signal using CS DSP with $m \ll N$; for each measurement, n_s time samples are taken at a rate $1/t_s$ for both approaches.

between elements is $P_l(i)$. The results of the phase shifts can be seen in **point 2**; the random perturbations between elements causes incident power to be collected from all possible DOA directions within the antenna array's FoV from θ_{\min} to θ_{\max} . This results in a *spread composite antenna pattern* with a wide spatial response. For this paper, the phases corresponding to the elements of the Rademacher sequence are 0° or 180° . $P_l(i)$ is changed m times where $m \ll N$, each time resulting in a new composite antenna pattern and complex measurement consisting of n_s samples at the output of the summer shown in Fig. 4(b). The array factor (AF) of the DSIC in *CBF-Reception mode* and *CS-DOA mode* is shown in the following equations where i is the PN sequence number:

$$\text{AF}_{\text{cbf}}(\theta) = \sum_{l=0}^{N-1} e^{j l (2\pi d \sin(\theta) + \phi)} \quad (11)$$

$$\text{AF}_{\text{dsic}}(\theta, i) = \sum_{l=0}^{N-1} e^{j l \left(2\pi d \sin(\theta) + \frac{P_l(i)}{l}\right)}. \quad (12)$$

D. Comparison Between the CBF and CS-DOA Modes

Since the DSIC in *CS-DOA mode* only needs to make m measurements instead of the N sector scans that a CBF needs, the *CS-DOA mode* compression factor over the CBF is

$$\Lambda = \frac{N}{m}. \quad (13)$$

The DSIC loses sensitivity when compared to a CBF performing an exhaustive scan at minimum sector resolution [29]. This loss in sensitivity Γ is proportional to the number of CS measurements used and in essence, the DSIC trades off detection speed for signal detection sensitivity and vice versa via (14)

$$\Gamma = 10 \log(\Lambda) \text{ (dB)}. \quad (14)$$

Fig. 5 illustrates an implementation example comparing a spatial scan using the CBF and the CS-DOA approach

proposed here. For both Fig. 5(a) and (b), the number of antennas N is eight and the number of incident signals K is 1. Although the CBF needs to search through N angles and takes Nt_{detect} seconds, the DSIC in *CS-DOA mode* needs only mt_{detect} seconds. This results in an energy consumption that is no longer quadratically related to N as shown in the following equation but rather through m :

$$E_{\text{DSIC}} = m N t_{\text{detect}} P_{\text{ant}}. \quad (15)$$

Note that this comparison assumes the CBF does not change its sensitivity level and that only the DSIC is trading off speed for sensitivity as shown in (14).

E. Scalability in CS-DOA Mode

The DSIC is scalable in multiple ways; the first and foremost is that if a degradation in sensitivity is allowed when in *CS-DOA mode*, the DSIC's scan energy is related to the number of compressed sensing measurements m which is logarithmically related to the number of potentially active DOAs.

The second scalability aspect of the DSIC is the number of signals it can detect. The DSIC can scale to the number of signals present without hardware changes by dynamically changing its number of CS measurements to compensate for a varying number of interferers present in the electromagnetic (EM) environment.¹ By increasing the number of PN sequences, m , and, therefore, *composite antenna patterns*, the maximum number of detectable interferers increases. The number of CS measurements, e.g., *composite antenna patterns* needed is given by (10). The DSIC's CS measurement scalability is shown in Section IV-G, where two sub-modes of operation are showcased; *high-efficiency CS-DOA mode* and *high-sensitivity CS-DOA mode*.

¹This assumes the input signal is stationary over the measurement time frame. This is a reasonable assumption in many applications given the high scan speed of the CS DoA approach. Moreover, other techniques, like CBF, also need to make this assumption and over a longer time frame.

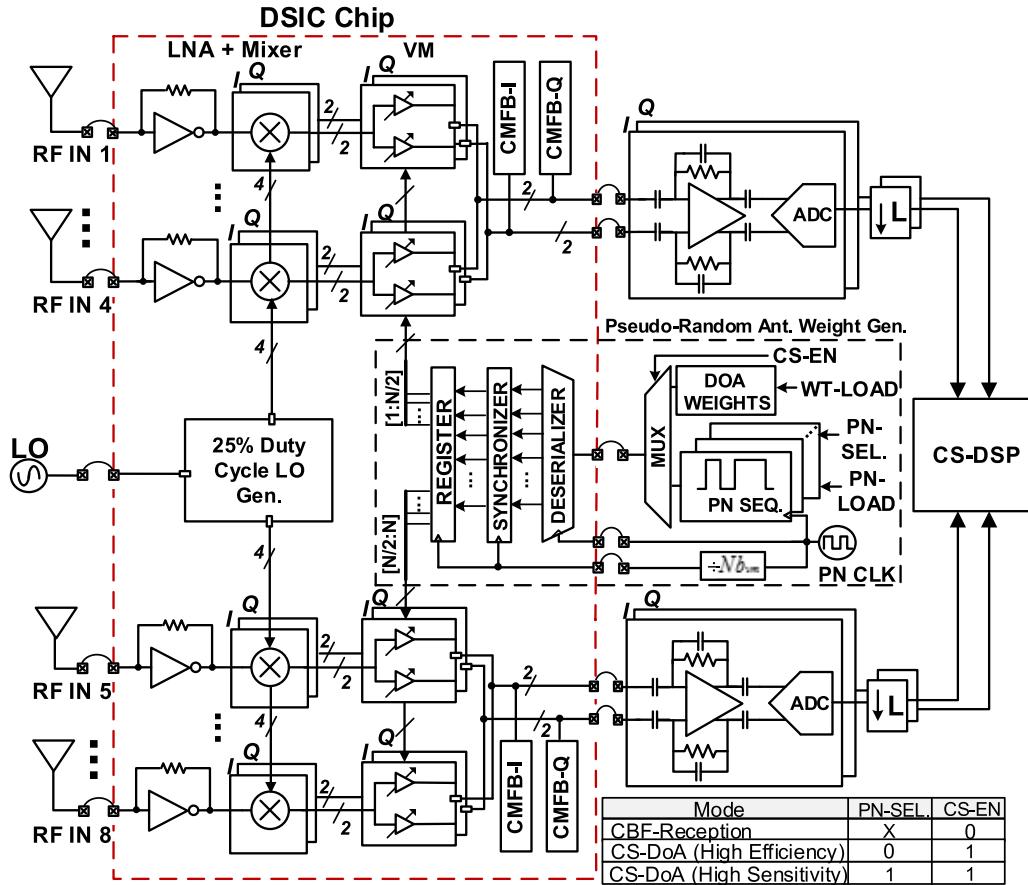


Fig. 6. Implementation of the eight-channel DSIC RF-ASIC system; a custom RFIC performs low noise RF amplification, downconversion, and baseband phase shifting with VMs; off-chip filters and ADCs provide samples to the CS DSP engine.

For the case where an unknown number of signals (and hence DOAs) are present, an unknown number of measurements will be needed. For this scenario, analysis of the OMP residue and signal detection threshold can be used to help reconfigure the DSIC. For example, if five signals are present in the environment and the DSIC is configured to find two signals with 90% probability of detection, the OMP residue will be large, indicating one of two things; more than one signal is present and, therefore, more CS measurements are needed, or the signal detection threshold should be set higher. For most cases, a pre-defined OMP threshold can be used. However, if needed and assuming the signal and DoA conditions are stationary and have not changed, finding the correct OMP threshold to guarantee sparsity only needs to happen once at the beginning of a scan. Previous measurements can be reused [30].

For instances where a signal occupies two effective bins in CS-DOA mode, two bins will be considered “active.” This scenario is related to “basis mismatch” and while there are techniques to mitigate this, they are beyond the scope of this paper [31].

III. DSIC IMPLEMENTATION

A. Architecture and Modes of Operation

The DSIC RF-application-specified integrated circuit (ASIC) contains eight RF front ends (Fig. 6). Phase shifting

is performed at baseband using VMs that are configured for either *CBF-reception mode* or *CS-DOA mode*. The DSIC chip can be “daisy chained” into other DSIC chips, increasing the number of possible antenna elements easing design integration and allowing the DSIC to conform to arbitrary antenna array geometries. Finally, the DSIC chip has two current-mode outputs that can either be fed to separate off-chip TIAs or combined.

B. RF Front-End Circuit Implementation

Fig. 6 depicts the DSIC system. At the antenna input, a shunt-shunt feedback inverter-based LNA design was chosen for the DSIC chip due to its simplicity and compactness in the overall layout (Fig. 7). The input matching and gain tradeoff with the size of feedback resistor R_f . A feedback resistance of $R_f = 353 \Omega$ and a PMOS and NMOS transconductance of 22.6 mS resulted in the most favorable tradeoff in gain and input matching. The mixers are passive, transmission gate based and require a four-phase LO. The ON resistance R_{on} of the mixer transmission gates is 7.5Ω .

C. LO Generation

The LO path consists of eight, matched LO lines fed by a 25% duty-cycle LO generator. The LO lines are buffered at both the generator and the mixer inputs and were carefully routed to ensure equal length and parasitics. An accurate LO

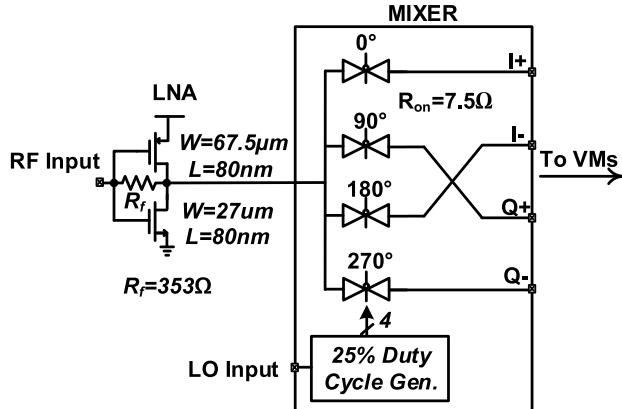


Fig. 7. Circuit details of the LNA and transmission gate-based mixer.

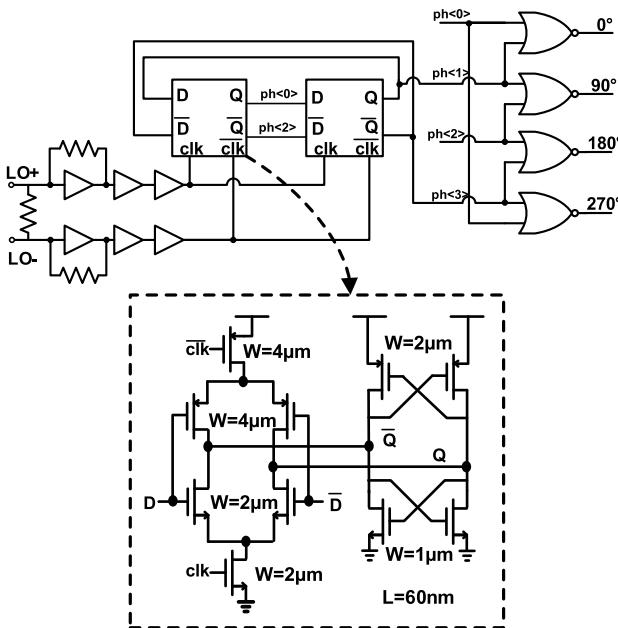


Fig. 8. Circuit implementation of the four-phase clock generator.

generator is required because phase errors in the LO path translate to the VM's resulting in unwanted phase rotations in the baseband outputs, which would manifest themselves as off-center beam errors and nulls. The LO generator and clock buffers are implemented on chip and shown in Fig. 8.

D. Vector Modulator Circuit Design and Properties

Phase shifts are performed using the VMs. By adjusting the weights α and γ (see Fig. 9), the phase of the input signal can be changed via a rotation of its Cartesian coordinates.

For *CBF reception mode*, the VM's crossover paths are enabled. The weighted I and Q outputs are

$$I_{\text{out}} = I_{\text{in}}\alpha_1 + Q_{\text{in}}\gamma_1 \quad (16)$$

$$Q_{\text{out}} = I_{\text{in}}\alpha_2 + Q_{\text{in}}\gamma_2. \quad (17)$$

The VM weights are, therefore; α_1 is $\cos \phi$, γ_1 is $\cos \phi$, γ_1 is $-\sin \phi$, and α_2 is $\sin \phi$, where ϕ is the desired phase shift.

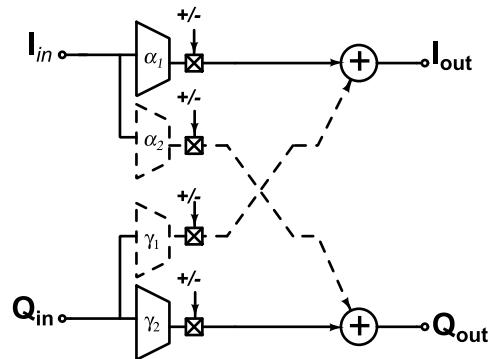


Fig. 9. Block diagram of the complex VM; in CS-DOA mode, only the blocks in solid lines are used; in CBF mode, the blocks in dotted lines are also turned on.

For *CS-DOA mode*, the VM's crossover paths are disabled as shown in Fig. 9. Since now only the polarities of the I and Q paths are changed, a VM's output at element l and PN sequence chip i is

$$I_{\text{out},l}(i) = P_l(i)I_{\text{in}}(\alpha_1) \quad (18)$$

$$Q_{\text{out},l}(i) = P_l(i)Q_{\text{in}}(\gamma_2) \quad (19)$$

where $P_l(i)$ is the PN sequence described in Section II-B2.

The VM weights $\alpha_{1,2}$ and $\gamma_{1,2}$ are controlled by multiple transconductance cells sized in $1\times$, $2\times$, and $4\times$ unit cells to deliver 5-bits of phase-amplitude resolution when in *CBF-Reception mode* (3-bits per quadrant) and 4-bits of phase-amplitude resolution in *CS-DOA mode*. Each VM unit cell is a current reuse, degenerated common-source amplifier (Fig. 10) and is enabled/disabled via the **en** and **en_b** pins. The VMs are connected to a switch matrix constructed from transmission gates that perform a complex multiply in *CBF-reception mode* and polarity switching of the I/Q outputs in *CS-DOA mode*. The total number of control bits each VM requires is 17; 3 bits for $\alpha_{1,2}$ and $\gamma_{1,2}$ as well as 5 bits for polarity and mode control (Fig. 9). The pseudo-random antenna weight generator sends the control bits to the VMs via a serialized bitstream sent at a clock rate of $(f_{\text{PN}}/N \cdot b_{\text{vm}})$ where f_{PN} is the rate of the PN sequence clock and b_{vm} is the number of control bits used for each VM. Each bank of four VMs is connected to a common-mode feedback (CMFB) circuit with a unity-gain bandwidth of 90 MHz. The current outputs of the VM's are combined off-chip and summed and converted to voltages via a bank of TIAs before being sampled. The maximum VM resolution of 5-bits was chosen so that the beam-pointing accuracy in *CBF-Reception mode* is high (less than 5° quantization error). Also, VMs were chosen over regular phase shifters for their ability to weigh both amplitude and phase, allowing the DSIC chip to create nulls to reject interferers [24].

The off-chip circuitry after the I/Q paths are summed does not have any special requirements for operation in CS-DOA mode when compared to CBF-Receive mode and the same TIAs and ADCs can be used for both modes interchangeably. For the narrowband signals used in Section IV-G, the off-chip filter BW was set to 6 MHz.

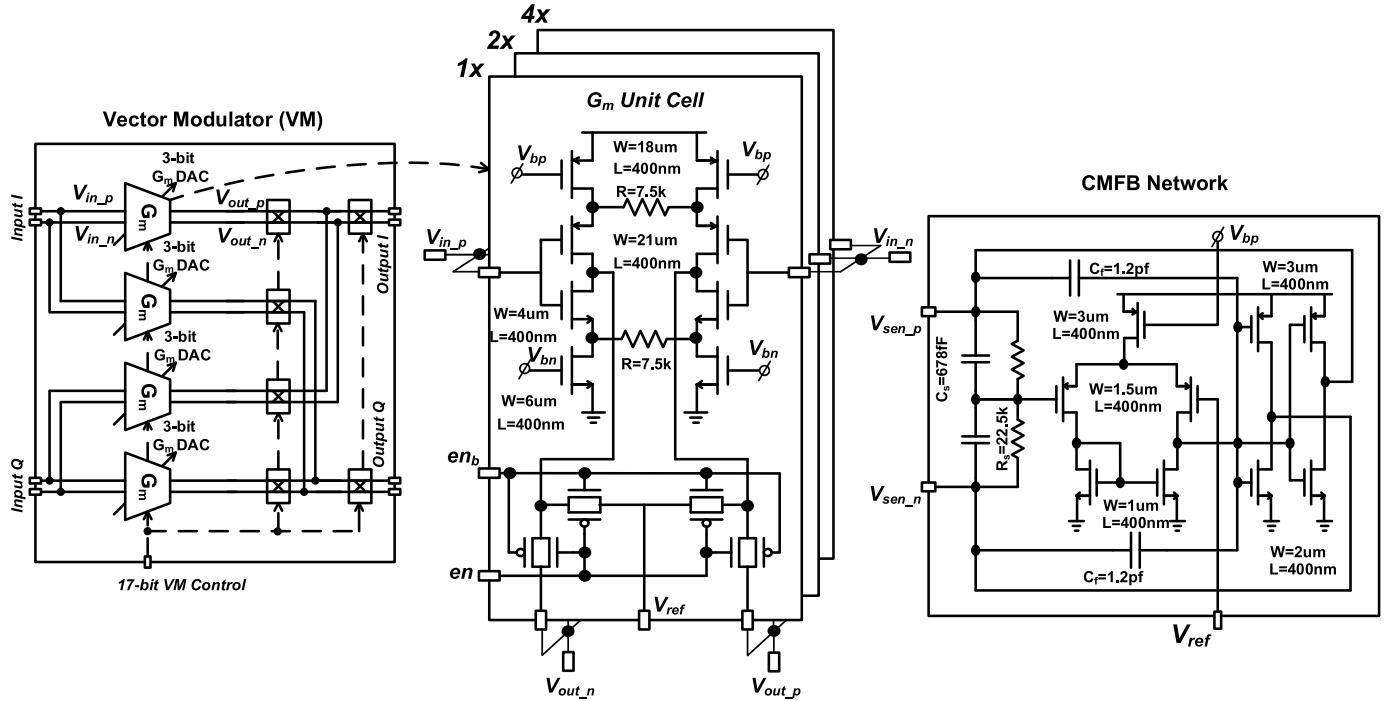


Fig. 10. Circuit details for the VM including the gm DAC and CMFB network.

E. Pseudo-Random Antenna Weight Generator

The pseudo-random antenna weight generator consists of on-chip and off-chip sections. The on-chip section is designed as a shift-register-based serializer-deserializer (SERDES) receiver (Fig. 11) with a maximum clock rate of 300 MHz. The SERDES receiver is loaded via an off-chip lookup table that contains multiple PN sequences each corresponding to a *composite antenna pattern*. The pseudo-random antenna weight generator is separated into two halves, each with 68 flip-flops. Each group of 17 flip-flops holds the state for 17 VM control bits. The pseudo-random antenna weight generator and the CMFB circuits of the VM's determine the maximum rate that the PN sequences can propagate across the downconversion paths. This rate, in turn, limits the maximum speed that an SOI can be moving spatially. For this paper, we assume a static SOI but the max speed is determined in [22]. When in *CS-DOA mode*, PN sequences are selected and loaded by the **PN-SEL** and **PN-LOAD** signals shown in Fig. 6. When in *CBF-Receive mode*, antenna weights are controlled by the **WT-LOAD** signal. The **CS-EN** signal controls which mode is currently selected.

IV. EXPERIMENTAL RESULTS

The DSIC RF-ASIC with eight RF front ends, baseband VMs, four-phase 25% duty-cycle LO generator, LO drivers, bias and control circuitry was implemented on 4.28 mm² (1.58 mm² active area) in 65-nm GP CMOS (Fig. 12) and operates from 1.2 V. The entire DSIC RF-ASIC, including eight downconversion paths (LNA, mixer, VM), pseudo-random antenna weight generator and LO generator consume a total of 158 mW. The DSIC chip layout was done with careful consideration to symmetry between all eight downconversion paths. The vertical and horizontal symmetries of the layout

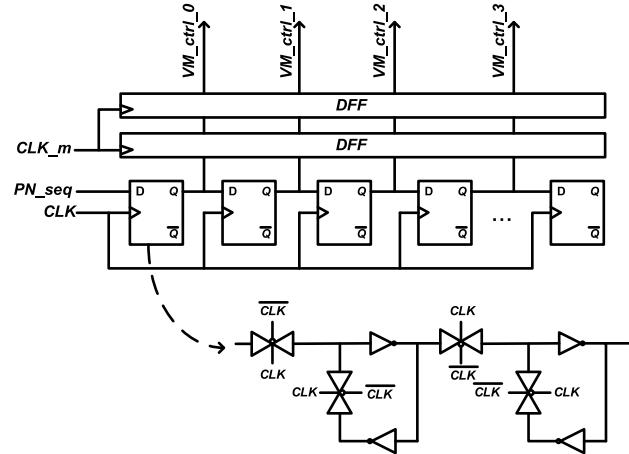


Fig. 11. Block diagram of the SERDES receiver for the pseudo-random antenna weight generator; the flip-flop circuit implementation is also shown.

of the front ends and the VM's are not only ideal for LO path routing but also the floorplan was optimized so all the bond-wire inductances to the RF inputs are roughly the same.

A. RF Performance of a Single Channel

The measured RF performance of a single RF channel is shown in Fig. 13. Conversion gain, NF, IIP3, and P1 dB are measured after the off-chip TIA shown in Fig. 6.

The return loss S_{11} at the antenna inputs is nominally better than -10 dB from 1 to 3 GHz. Conversion gain of each single receiver path with the VM adjusted to maximum amplitude is 32 dB across an IF BW of 25 MHz, which is close to our simulated value of 33 dB. The NF, P1 dB, and in-band IIP3 of each path at 1.5 GHz are 6.4 dB, -11.3 dBm, and 3.3 dBm, respectively. NF, conversion gain, and S_{11} versus RF

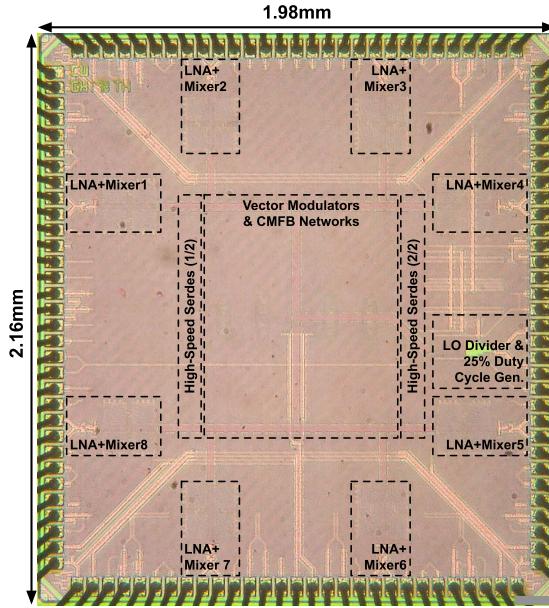


Fig. 12. Annotated photograph of the 65-nm CMOS prototype.

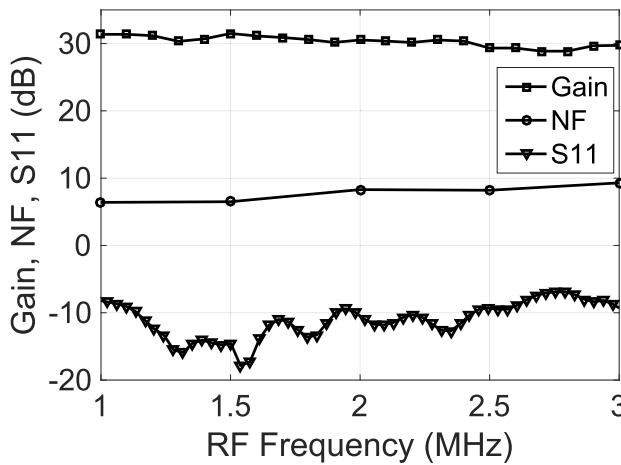


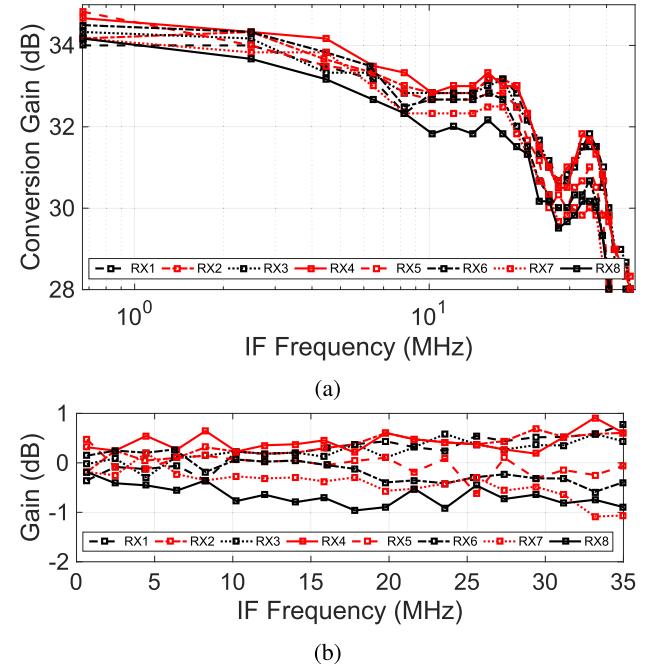
Fig. 13. Measured RF performance characteristics for a single downconversion path.

frequency are shown in Fig. 13. Overall, each downconversion path was optimized for small size and the design goal was to fit as many downconversion paths on the chip as possible. This high density approach would allow the DSIC chip to find more interferers on a single chip when in *CS-DOA* mode and also be able to use an antenna array with a wide aperture, thus providing as fine a detection resolution as possible.

The conversion gain versus IF is shown for all individual paths shown in Fig. 14. This was measured by fixing the LO at 1.5 GHz and sweeping an RF input signal. The gain variations across the 25-MHz IF are within ± 1 dB.

B. Vector Modulator Performance

The full 4-bit operational range of the VMs in *CS-DOA mode* is demonstrated with a constellation plot shown in Fig. 15. The constellation plot was measured using a 1.5-GHz input signal fed into a single antenna port of the DSIC chip. The VMs were first digitally calibrated to correct for gain

Fig. 14. (a) Conversion gain for all eight paths versus IF frequency. (b) Detailed gain variation plot; the gain variations are within ± 1 dB.

mismatch across all downconversion paths. The maximum VM phase error of 2° corresponds to an antenna pattern null increase of less than 2 dB (see in the following). The VM constellation shows a worst case VM amplitude variation of 0.65 dB most likely due to coupling between LO traces.

C. Multi-Antenna Emulation Testbed

For multi-antenna measurements in *CBF-Reception* and *CS-DOA* mode, the DSIC chip was tested by feeding the antenna inputs with emulated far-field emitters from different directions. The far-field signals for emitters with wavelength λ were created via a custom RF spatial signal generator (Fig. 16) emulating a ULA with $(\lambda/2)$ antenna spacing. The FoV was set to be -80° to $+80^\circ$. The complete benchtop testbed is shown in Fig. 17 which includes the spatial signal generator as well as other RF test equipment. The worst measured error in the spatial signal generator was 2.5° between paths for phase and 0.3 dB for amplitude. For linearity measurements, the TIA and ADC driver gain in the off-chip circuit was reduced by half to ensure that the PCB circuit is not the measurement bottle-neck.

D. CBF Mode: Antenna Patterns and Linearity

Fig. 18 shows the normalized beam patterns for five directions in *CBF-reception mode* and the theoretical AF. The 2-dB difference in theoretical versus measured null depth is due to the quantized nature of the VM's, the gain differences between the VM's as well as the nominal 2.5° error in the spatial signal generator's simulated antenna outputs.

E. CBF Mode: Linearity

Fig. 19 shows the $B1dB$ and $P1dB$ versus angle with in *CBF-Reception* mode. The $B1dB_{NF}$ is a measurement of the

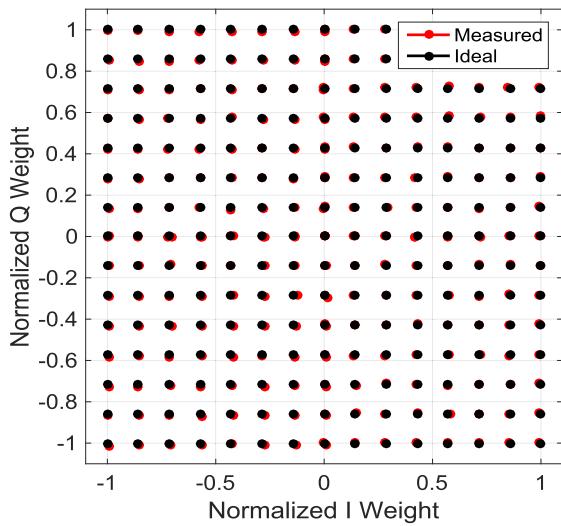


Fig. 15. Measured performance of the VM of a single downconversion path in CS-DOA mode; a constellation plot for an 1.5-GHz input signal and the associated gain and phase errors for each constellation point.

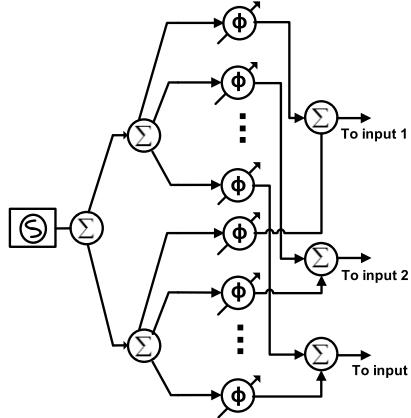


Fig. 16. Block diagram of the custom far-field antenna-array spatial signal generator used for testing built RF power splitters/combiners (Σ) and tunable phase shifters (Φ). It is capable of generating signals from two arbitrary directions.

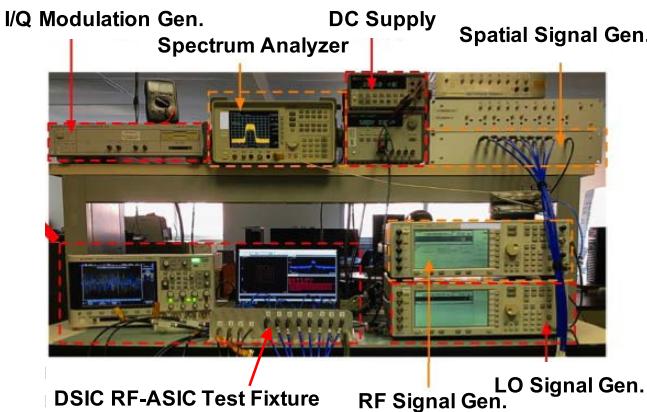


Fig. 17. DSIC testbed showing DSIC RF-ASIC test fixture and custom test equipment.

excess noise created by harmonics of the LO mixing with a blocker [32]. Measurement of $B1dB_{NF}$ was performed by positioning a blocker at 0° and 200 MHz away from the LO. The DSIC chip performed a scan in *CBF-reception mode* and

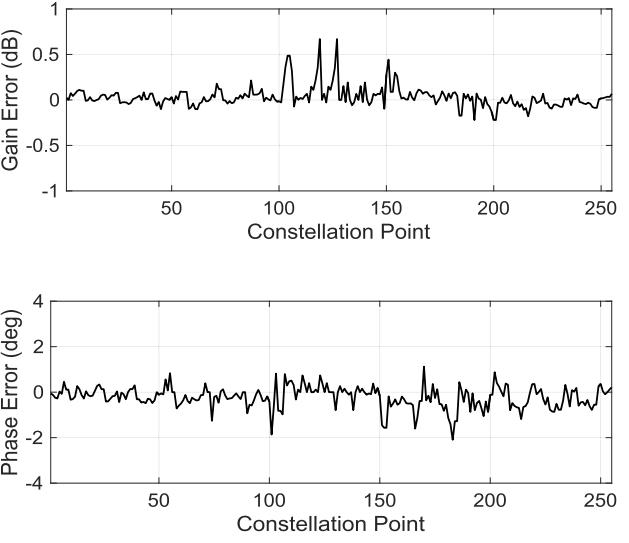


Fig. 18. Measured antenna patterns in CBF-reception mode compared with the theoretical AF for 0° , $\pm 15^\circ$, and $\pm 30^\circ$.

for each DOA angle, the $B1dB_{NF}$ was measured by observing at what blocker power the receiver noise floor increased by 1 dB. For the $P1dB$, a similar procedure was used, however, in this case, the $P1dB$ versus angle profile was calculated by placing an input signal at the same frequency as the LO and at 0° using the spatial signal generator. Similarly, with the DSIC RF-ASIC, in *CBF-Reception mode*, a DOA scan was performed and the $P1dB$ versus angle was measured.²

F. CS-DOA Mode: Antenna Patterns

Fig. 20 shows the measured composite beam patterns in *CS-DOA mode* for four distinct PN sequences. Also, illustrated is the AF for a CBF and the average gain of the four *composite antenna patterns*. The DSIC gain is lower since it trades off

²Measured with all elements but power referred to the single-element input.

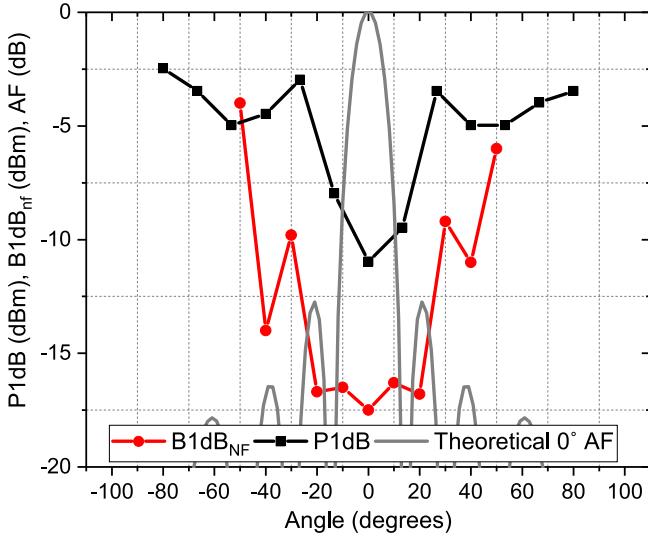


Fig. 19. Measured P_1 dB and B_1 dB_{NF} versus angle; the blocker is at 0° while the receiver in CBF mode sweeps its angle of reception; the corresponding AF for a CBF pointing at 0° is also shown for reference.

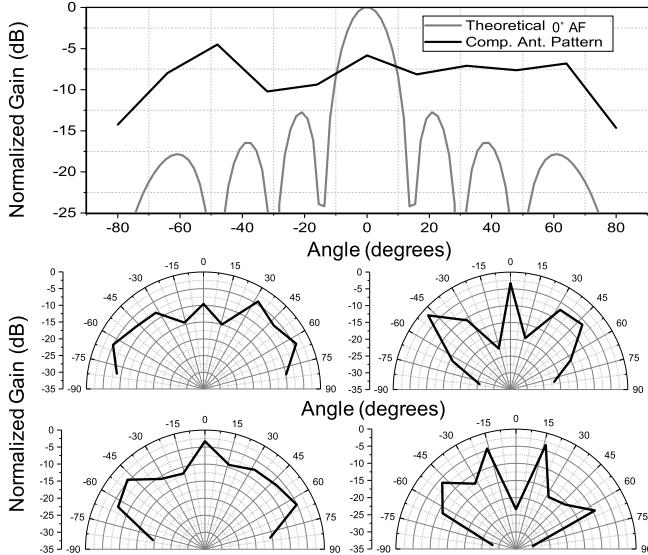


Fig. 20. Measured composite antenna patterns in CS-DOA mode for four different PN sequences (bottom). Theoretical AF for a 0° CBF versus the average gain of the composite patterns for gain comparison (top).

sensitivity for its ability to sense signals from all directions. In contrast to CBF antenna gain patterns, in the CS DoA patterns, the gains for all directions are relatively large, but they intentionally vary so CS reconstruction can be done later.

G. CS-DOA Mode: Signal Detection Performance

Fig. 21(a) shows the probability of detection, P_d , and probability of false alarm, P_{fa} , for one signal versus received signal strength at the antenna in *high-energy-efficiency* CS-DOA mode. The performance goal is to use the minimum number of CS measurements for the fastest scan time of $1\ \mu\text{s}$, while maintaining $P_d > 90\%$ and a $P_{fa} < 10\%$. The DSIC is able to detect one signal with a $P_d > 90\%$ at an incident

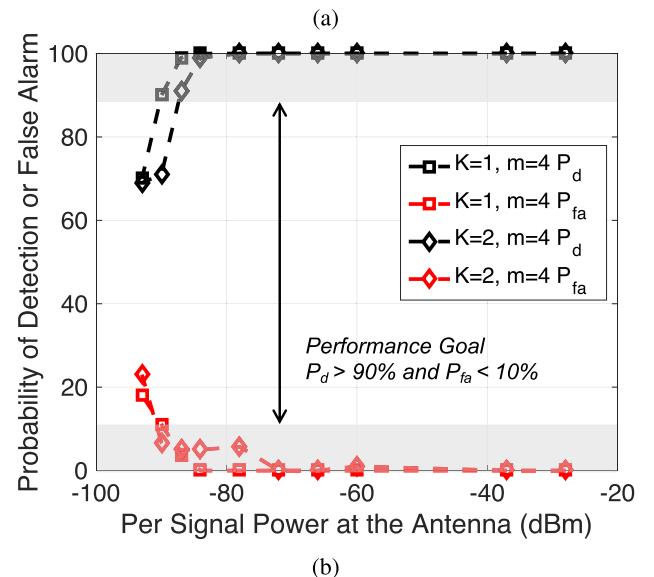
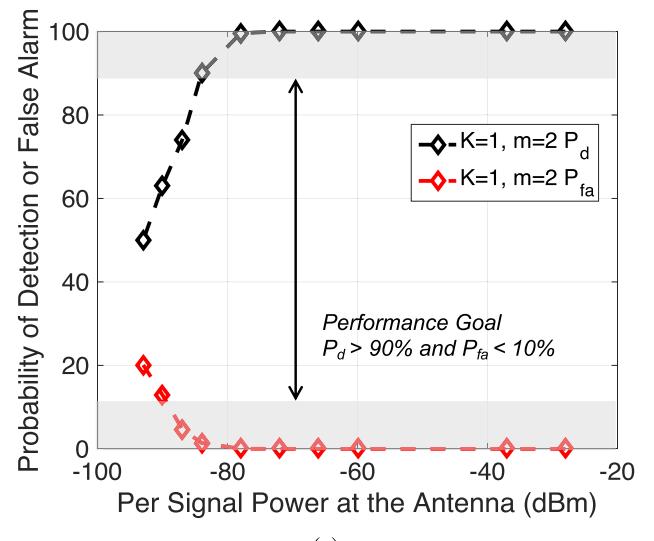


Fig. 21. Measured probability of detection P_d and false alarm P_{fa} for the CS-DOA mode for one ($K = 1$) or two ($K = 2$) SOI in (a) high-efficiency mode with two measurements ($m = 2$) and (b) high sensitivity mode with four measurements ($m = 4$). The number of time samples n_s used is 25.

power > -84 dBm using two CS measurements, i.e., two composite antenna patterns.³

Fig. 21(b) shows P_d and P_{fa} for one and two SOIs versus received signal strength in *high-sensitivity* CS-DOA mode where four CS measurements are used. In this case, the scan time is increased to $2\ \mu\text{s}$, but sensitivity is improved; the DSIC can detect a single signal at -90 dBm and two signals at -87 dBm. In both cases, $P_d > 90\%$.

All measurements use 25 time samples per measurement ($n_s=25$). The effective sensitivity level (ESL) of the DSIC can be calculated using

$$ESL = 10 \log(KT_0BW) - G_a + \Gamma + S + 10 \log(F) \quad (20)$$

³These measurements use more optimal PN sequences as well as a test setup with better dynamic range than in [23], resulting in a better sensitivity than presented in [23].

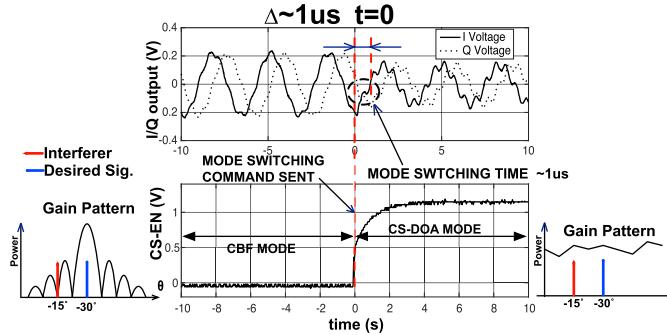


Fig. 22. Measurement showing the fast switching between CBF mode and CS-DOA mode.

TABLE II
SINGLE-ELEMENT RF PERFORMANCE COMPARISON WITH CURRENT SOA

	Reference	[1]	[2]	[3]	[4]	[5]	This Work
Single Element	Technology	65nm	65nm	65nm	65nm	65nm	65nm
	RF Frequency	GHz	0.6-3.6	1-2.5	1-4	0.1-3.1	0.1-1.7
	Number of Antennas/chip	#	4	4	4	4	8
	Power Consumption/ant. ¹	mW	26.5	7.3	53	32.6	37
	Active Area/ant.	mm ²	0.24	0.05	0.27	0.36	0.42
	IF Bandwidth	MHz	5	30 ²	65	NR	NR
	In-Band IIP3	dBm	6	1	-1	-29	-41
	NF	dB	3-6	6	7	2.1-5.8	2.2-4.6
	Compression Point	dB	-5	-9	-14	-25	NR
	Return Loss ¹	dB	< -10	-14	NR	NR	-10
Array	Single Element Conv. Gain	dB	-1	12	16	43	41
	Min Phase-Shifter Res.	Deg.	32.5	8.18	11.25	NR	5.625
	SNR Improvement	dB	6	6	6	6	9

¹Adjustable, ²Measured at 1.5GHz, NR = Not Reported

where G_a is the SNR increase due to the array, and Γ is the effective sensitivity loss due to using CS, BW is the IF bandwidth, and S is the required SNR margin. An experimentally established SNR margin of ≈ 13 dB was found to be sufficient for $P_d > 90\%$ for all modes of operation [22].

The measured ESLs shown in Fig. 21(a) and (b), come to within 3 dB of the predicted values in (20) for the $K = 1$, $m = 4$ case. In the $K = 2$, $m = 4$ case, a 3 dB drop in sensitivity is noted and corresponds to behavior observed in [22]. For the $K = 1$, $m = 2$ case, a further 3 dB drop in sensitivity is noted that is most likely due to the small set of measurements m used in relation to the system size or to non-optimal PN sequences being used; we have noticed similar behavior in simulation. For strong signals, we believe that the linearity limitations will be similar to previous efforts to characterize the effect of linearity on CS-based signal recovery in the spectral domain [21].

H. Switching Between CBF and CS-DOA Modes

The fast switching speed between CBF and CS-DOA modes is demonstrated in Fig. 22. A desired signal at the center of the CBF beam and an interferer offset by 15° in angle and 1 MHz in frequency are applied. At first, in *CBF-reception mode*, only the in-beam signal is received. After the DSIC switches to *CS-DOA mode*, both signals are received. The mode switch takes less than $1 \mu\text{s}$.

V. COMPARISON WITH THE CURRENT STATE-OF-THE-ART

Table II shows the comparison of the single-element RF performance of the DSIC to other multi-antenna receivers that

TABLE III
WIDEBAND SCANNER COMPARISON WITH CURRENT SOA

DoA Scanner Measurements	DoA Method	CBF based DoA					CS-DoA Mode
		[1]	[2]	[3]	[4]	[5]	
Num. of Antennas Per Chip	#	4	4	4	4	4	8
Num. of ADC's Required	#	4	4	4	4	4	2
Num. of Chips in Scanner	#	2	2	2	2	2	1
Scanner Pow. Consumption ²	mW	212	58	424	261	296	158
Number of Scan Angles	#	8	8	8	8	8	8
Sector Scan Time ³	ns	500	500	500	500	500	N/A
Total Scan Time*	μs	4	4	4	4	4	1
Energy Per Scan	nJ	848	234	1,696	1,043	1,184	158
Energy Per Scan (4x8) array ⁴	nJ	13,580	3,750	27,136	16,704	18,944	1,580
Energy Per Scan (8x8) array ⁴	nJ	54,323	15,001	108,544	66,816	75,776	3,792

¹Measured at 1.5GHz, ²ADC requirements for each scanner are the same so only RF front end power is shown. ³sampling rate = 50MHz, 25 samples, ⁴Extrapolated using measured data,

⁵Adjustable, ⁶K=1 SOI ⁷Baseband processing energy consumption is not included because DSP requirements are similar.

could be used for DOA finding. While the DSIC compares favorably to the current SOA for RF performance, it performs significantly better than the current SOA when used for DOA finding. In Table III, we estimate the performance of a CBF-based DOA scanner using published CBF-Receiver chips for the comparison to the presented CS-DOA DSIC scanner. The DOA scanning approach with the highest likelihood of discovering an emitter is the “exhaustive search” introduced in Section II-B2. All antenna elements are active meaning that the angular resolution of the scanner is at its maximum. This guarantees that the SNR of the received signal is at its highest; however, the narrow beam means that the total scan takes longer as the main-beam sensitivity is kept constant and not adjusted. Because of the complexities in comparing a multitude of search methods and architectures, we compare solely to a CBF with this single-beam exhaustive search. We assume an eight-antenna DOA scanner identifying one signal out of eight possible scan angles. For all hypothetical scanners, we use $n_s = 25$ samples and $f_s = 50$ MHz which equates to a scan time of 500 ns. The DSIC in *CS-DOA mode* requires two CS measurements, requiring a total scan time of $1 \mu\text{s}$. As a result, the CS-DOA approach offers a much faster estimate of the DOA of the signal with a significantly lower energy usage. Also, Table III gives extrapolated measurements from calculated data for 32 and 64 antennas, demonstrating the scalability advantages of the DSIC.

VI. CONCLUSION

The DSIC phased-array receiver architecture offers in one unified architecture two major functions that are currently typically provided by separate blocks: a fast DOA scanner and a CBF-based receiver. The DSIC uses CS for rapidly finding the DOA of SOI. In *CS-DOA mode*, compressed samples are obtained consecutively using PN-sequence-based *composite antenna patterns*, allowing the DSIC to quickly scan the spatial environment. In *CBF-reception mode*, the DSIC receives an emitter in a particular direction.

Thanks to CS, the DSIC has the ability to sense all scan angles simultaneously, allowing it to detect signals faster, and

while consuming less energy, than the current SOA. In *high-energy-efficiency CS-DOA mode*, a single signal with incident power above -84 dBm can be recovered in $1\ \mu\text{s}$ with only two CS measurements by our eight-channel DSIC chip. This is $4\times$ faster and at least $1.5\times$ more energy efficient compared to swept CBF scanners using receivers from [1]–[5]. With four CS measurements in *high-sensitivity CS-DOA mode*, multiple signals as small as -87 dBm can be found and the DSIC is still $2\times$ faster than comparable CBF scanners. For applications using larger antenna arrays and while trading off for sensitivity, the DSIC architecture is projected to scale favorably for DOA finding with an energy efficiency that is an order of magnitude better than similar CBF-based architectures.

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