An 8-Element, 1-3GHz Direct Space-to-Information Converter for Rapid, Compressive-Sampling Direction-of-Arrival Finding Utilizing Pseudo-Random Antenna-Weight Modulation

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***Abstract*— The Direct Space-to-Information Converter (DSIC) unifies conventional delay-and-sum analog beamforming (CBF) with compressed-sampling (CS) rapid DoA finding into a single reconfigurable phased-array architecture. The DSIC chip includes 8 direct-conversion paths each delivering 32dB conversion gain, 3.3dBm in-band IIP3 and 6.4dB NF while consuming 19.8mW from 1.2V. The DSIC is able to switch between CBF-reception mode and CS-DoA mode in less than 1us. In CS-DoA mode, the DSIC finds the DoA of a single emitter in 1us consuming 158nJ which is 4x faster and 1.5x less energy than a comparable CBF scanner. For applications where many antennas are used, the DSIC uses an order of magnitude less energy than similar architectures.**

I. Introduction

The continuously growing demand for wireless connectivity for people and machines is making the RF spectrum increasingly crowded and spatial diversity is becoming an important technology to address this congestion. Finding the direction of arrival (DoA) of an emitter requires a receiver to have multiple antennas, increasing system complexity. Recently proposed hardware designs still perform conventional beamforming (CBF) in the analog domain since it only requires a single set of I/Q outputs and ADCs [1]–[3]. However, a CBF receiver can only receive a signal in one direction at a time and to spatially find a signal of interest (SOI) it must *scan* the spatial environment sequentially. Hybrid and iterative search techniques have been proposed that require less scan-time than an exhaustive *swept* search but they exhibit higher mis-detection probabilities and in realistic channel environments, swept scans are still preferred [4].

We present a direct space-to-information converter (DSIC) that unifies a delay-and-sum CBF with rapid, compressed-sampling (CS) DoA finding into a single, reconfigurable and scalable receiver-array architecture [5]. Previous work [6] proposed a CS architecture for DoA finding, however, using a separate receive path for each CS measurement. For example, to obtain four CS measurements in an 8-antenna receiver, 32 receive chains are required. This leads to a very large chip area. Moreover, in realistic environments with a varying number of SOIs, the number of CS measurements needs to be easily *scalable*. The DSIC architecture is more efficient for ASIC implementation and can adapt to the spatial environment. This adaptability is reflected in the DSIC's multiple modes of operation; a receive mode that functions as a beamforming, multi-antenna receiver (CBF-reception mode), and a fast-scanning mode (CS-DoA) mode. In CS-DoA mode, the number of CS measurements can further be scaled for high-sensitivity or high-energy-efficiency operation.

II. Background

Figure 1 contrasts the traditional CBF method for direction finding with the CS-DoA approach proposed here. To find the DOA of an SOI, an N-antenna CBF must step through all possible DoAs. In this paper, we assume a uniform linear array (ULA) is used. The CBF sequentially scans the angle-space consisting of N angles[1], spatially filtering them with a narrowband response. This is performed by multiplying the downconverted signal for each antenna path with an element of weight vector $\mathbf{w} = \frac{1}{N}[1...e^{-j\beta}, e^{-j2\beta}, e^{-j(N-1)\beta}]$. The relative phase between antenna elements is $\beta = 2\pi d \sin(\theta)$, θ corresponds to a DoA, and antenna element spacing is d. The weighted outputs from all antenna paths are summed (point A in Fig. 1) and when the aggregate power is above a threshold, a signal is said to be detected.

For a receiver with N antenna elements and N unique scan angles, the energy usage for a complete spatial scan with the CBF scales quadratically with N. Scan-angle resolution is inversely proportional to N, illustrating the fact that swept CBF scanners suffer from an inherent tradeoff between scan-angle resolution and scan-time or energy. A CBF scanner can detect a signal in each scan-angle, however, in many practical applications, we only need to determine the DoA of few large signals.

III. Using a Pseudo-Random Sensing Waveform to Create a Wideband Spatial Filter

In **CBF-reception mode**, the baseband weight vector $\mathbf{w}$ is statically programmed for a desired DoA θ and the summed, downconverted signal only contains information

[1]Typically with N antennas, N distinct direction-of-arrival angles can be distinguished with a beamwidth of $\Delta_{3dB} = \frac{\lambda}{N\cos(\theta)}$.

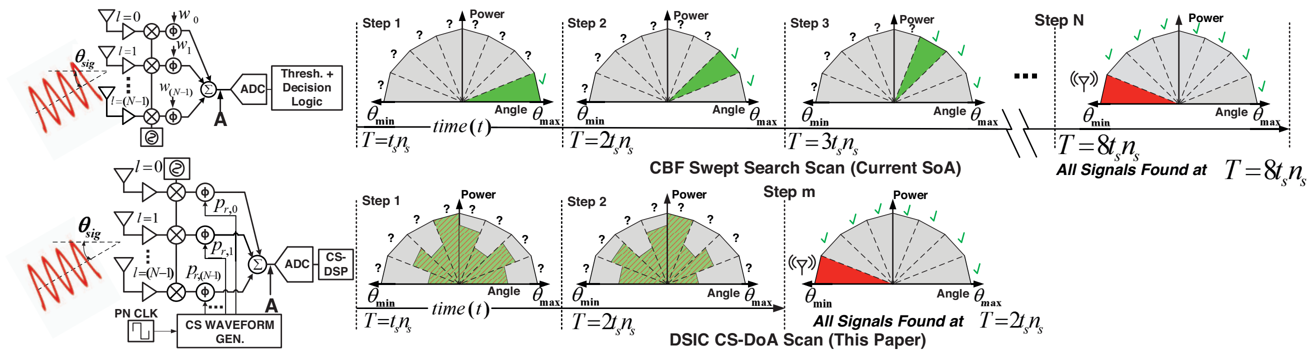


Fig. 1. Operation of the traditional CBF scan method for finding the DoA of a signal (top) vs. the CS-DoA method (bottom) used by the DSIC. The red signal incident on the array is a SOI and n_s is the number of samples and m the number of CS measurements.

from θ. In other words, the angle spectrum has been spatially filtered with a narrowband response around θ.

In **CS-DoA mode**, the weight vector **w** is created by randomly selecting the relative phases β between antenna elements. In this case, the phases are randomly generated to be either $0°$ or $180°$. This results in a *composite beam pattern* which consists of a series of lobes containing energy from all DoA's within the antenna array's field of view from θ_{min} to θ_{max}, giving the DSIC a wide spatial response (Fig. 1 (bottom)). The randomly generated phases are distributed across signal paths via a Rademacher based, pseudo-random noise (PN) sequence $P_{r,l}(t)$ of length N, where $r \in [1, m]$ indicates the PN sequence index and $l \in [0, N-1]$ is the antenna number. $P_{r,l}(t)$ is changed m times where $m \ll N$, each time resulting in a new composite beam pattern and complex measurement consisting of n_s samples at the output of the summer (A in Fig. 1 (bottom)). K DoAs can be recovered with $m = C_o K log\left(\frac{N}{K}\right)$ CS measurements [7].

In **high-energy-efficiency CS-DoA mode**, m=2 PN sequences are applied resulting in 2 unique composite beam patterns and 2 orthogonal measurements. Using only 2 measurements, this mode requires a small scan-time. In **high-sensitivity CS-DoA mode**, m=4 PN sequences are used resulting in 4 unique composite beam patterns and 4 orthogonal measurements. More measurements provide more processing gain and allow the DSIC to find more SOIs at lower incident powers at the expense of a longer scan-time.

Recovery of the DoAs from the CS measurements is performed by CS-DSP using *Orthogonal Matching Pursuit* (OMP) chosen for its simplicity and efficiency for sparse problems [7].[2]

[2]The estimated number of complex multiplications required is $M = N \cdot m$ per SOI, i.e. 16 for high-efficiency mode and 32 for high-sensitivity mode.

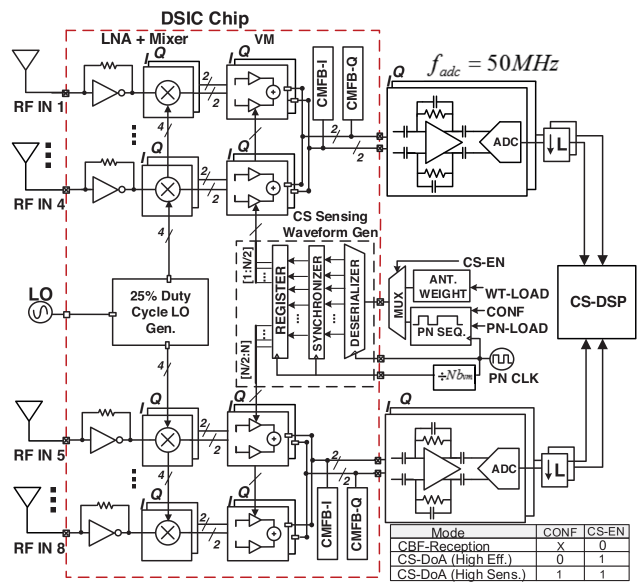


Fig. 2. The DSIC system architecture.

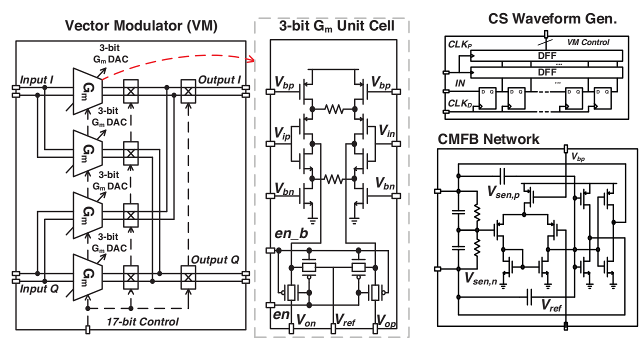


Fig. 3. Transistor level detail of key circuit components.

IV. DSIC System Implementation

A. System Architecture

The DSIC chip and associated system (Fig. 2) consists of 8 reconfigurable antenna paths that are separated into 2 banks of 4. The values of **w** are controlled by the CS waveform generator. Each downconverted bank is summed and sent to off-chip TIAs. The sampled IQ output pairs are summed digitally before being processed by the CS-DSP.

B. Circuit Implementation

The DSIC with 8 RF front ends, baseband vector-modulators (VM)s, 4-phase 25% duty-cycle LO generator, LO drivers, and bias and control circuitry was implemented on $4.28mm^2$ ($1.58mm^2$ active area) in 65nm CMOS (Fig. 7) and operates from 1.2V.

Each RF front end contains a shunt-shunt feedback inverter-based LNA and transmission-gate based passive mixers. The baseband VMs perform a complex multiplication on the down-converted signal by creating a weighted sum of the I and Q paths to generate an output with adjustable phase and amplitude. The VMs consist of multiple transconductance cells sized in 1x, 2x and 4x unit cells to deliver 5-bits of phase-amplitude resolution (3 bits per quadrant); cells are enabled/disabled via the the **en** and **en_b** pins (Fig. 3). The VM unit cell is a current reuse, degenerated common-source amplifier. Each bank of 4 VMs is connected to a common-mode feed-back (CMFB) circuit with a unity-gain bandwidth of 90MHz. The VMs are connected to a switch matrix constructed from transmission gates that performs a complex multiply in CBF-reception mode and polarity switching in CS-DoA mode. In total, the VMs require 17 control bits each for gain and polarity switching.

The CS sensing waveform generator is shift-register based and is programmed with a PN sequence provided off-chip. The output of the sensing waveform generator is deserialized and sent to the VM's at $\frac{f_{PN}}{N \cdot b_{vm}}$ where f_{PN} is the rate of the PN sequence clock and b_{vm} is the number of control bits used for each VM. The CS sensing waveform generator is designed for a maximum clock rate of 300MHz. The maximum clock-rate and the bandwidth of the VMs CMFB networks determine the maximum frequency that the PN sequence $P_{r,l}(t)$ can be updated. All 8 downconversion paths (LNA, mixer, VM), CS waveform and LO generators consume a total of 158mW.

V. Measurement Results

The DSIC chip was tested by feeding the antenna inputs with emulated far-field emitters at different directions assuming that the antenna inputs are connected to a ULA with $\frac{\lambda}{2}$ spacing between antenna elements where λ is the emitters wavelength. The field of view was set to be $-80°$ to $80°$. The return loss at the antenna inputs is nominally better than -10dB from 1GHz to 3GHz. Conversion gain of each single receiver with VM adjusted to maximum amplitude is 32dB for an IF BW of 25MHz. The NF, P1dB, and in-band IIP3 of each path at 1.5GHz are 6.4dB, -11.3dBm, and 3.3dBm respectively.

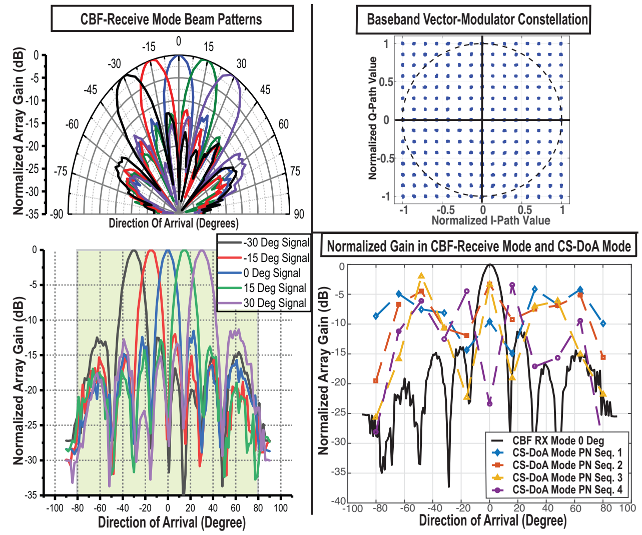


Fig. 4. DSIC operation measurements: beam patterns for five directions in CBF-reception (left); baseband VM constellation (top-right); normalized array gain in CBF-reception mode and the gain patterns for various PN sequences in CS-DoA mode(bottom-right). The green area is the array field-of-view.

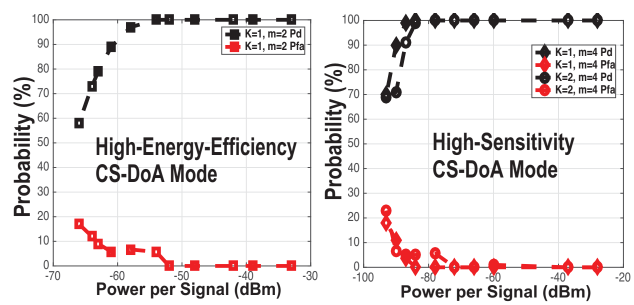


Fig. 5. Measured probability of detection (P_d) and probability of false alarm (P_{fa}) in CS-DoA mode for different numbers of signals K, and number of CS measurements m.

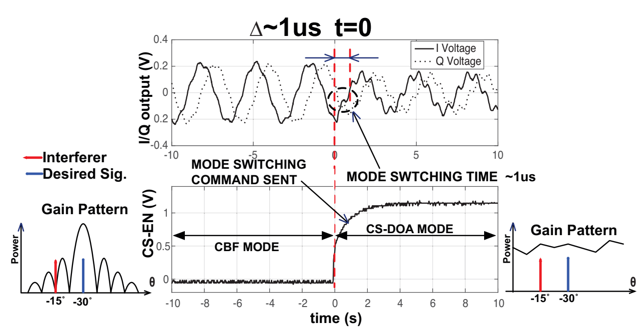
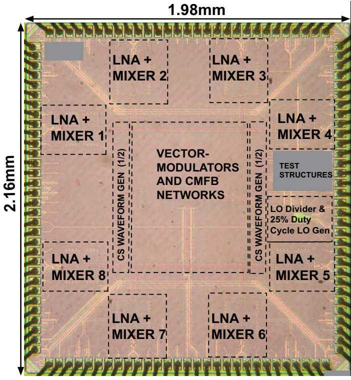


Fig. 6. Demonstration of the DSICs ability to switch between CBF-reception mode and CS-DoA scanning mode in 1us.

Figure 4 (left) shows the beam patterns for five directions in *CBF-reception mode*. The full 5-bit operational range of the VMs is represented by a



		This Paper
Single-Element	Architecture	DSIC
	CMOS Process	65nm
	Chip Area (mm^2)	4.28/1.58[1]
	Supply Voltage	1.2
	Frequency Range (GHz)	1.0 - 3.0
	Single Element IF BW (MHz)	25
	Single Element NF (dB)	6.4
	Power Consumption (mW)	158
	Power Consumption / Element (mW)	19.8
	Single Element Gain (dB)	32
	Single Element P1dB (dBm)	-11.3
	Single Element IIP3 (dBm)	3.3
	Single Element IB B1dB (dBm)	-18
	Single Element OOB B1dB (dBm)	-7.75
CBF RX	Phase/Amplitude Resolution (bits)	5
	Number of Elements	8
	8 Element SNR Improvement (dB)	9
CS-DoA	Mode Switching Speed (uS)	1
	Phase/Amplitude Resolution (bits)	3
1. Active Area		

Fig. 7. Die photo and performance summary at 1.5GHz.

TABLE I
THE DSIC COMPARED TO RECENT CBF BASED RECEIVERS

			[3]	[1]	[2]	This Work
	RF Frequency	GHz	1-2.5	0.6-3.6	0.1-3.1	1-3
Single Element	Number of Antennas/chip	#	4	4	4	8
	Power Consumption/ant.[1]	mW	7.3	26.5	32.6	19.8
	Active Area/ant.	mm^2	0.05	0.24	0.36	0.20
	IF Bandwidth	MHz	30[@]	5	NR	25
	In-Band IIP3	dBm	1	2	5	3.3
	NF	dB	6	3	2.8-4	6.4
	Single Element Conv. Gain	dB	12	NR	43	32
DoA Scanner Measurements	DoA Method		CBF based DoA			CS-DoA Mode
	Number of Antennas in Scanner	#	8	8	8	8
	Number of Chips in Scanner	#	2	2	2	1
	Scanner RF Power Consumption[2]	mW	58	212	261	*158*
	Number of Scan Angles	#	8	8	8	*8*
	Sector Scan Time[3]	ns	500	500	500	N/A
	Total Scan Time[*]	us	4	4	4	**1**
	Energy Per Scan[$]	nJ	*234*	*848*	*1,043*	**158**
	Energy Per Scan (32 Antennas)[4]	nJ	*3,750*	*13,580*	*16,704*	**1,580**
	Energy Per Scan (64 Antennas)[4]	nJ	*15,001*	*54,323*	*66,816*	**3,792**

[1]Values used for 1.5GHz operation, [2]ADC requirements for each scanner are the same so only RF front end power is shown. [3]sampling rate = 50MHz, 25 samples, [4]Extrapolated using measured data, [@]Adjustable, [*]K=1 SOI, [$] Baseband processing needed for CBF decision-logic and CS-DSP is assumed similar.

constellation plot Fig. 4 (top-right). Figure 4 (bottom-right) shows the composite beam pattern for 4 CS measurements with distinct PN sequences when in *CS-DoA mode*, in comparison with a beam pattern in CBF mode, illustrating the tradeoff in sensitivity that the DSIC makes for the ability to sense all angles simultaneously.

Figure 5 (left) shows the probability of detection, P_d and probability of false alarm, P_{fa} of 1 signal vs. received signal strength at the antenna in *high-energy-efficiency CS-DoA mode*. The DSIC is able to detect 1 signal with $P_d > 90\%$ at a power as low as -60dBm using 2 CS measurements. Figure 5 (right) shows P_d and P_{fa} of 1 and 2 signals vs. received signal strength at the antenna when in *high-sensitivity CS-DoA mode*. In this case, the DSIC can detect 2 signals with $P_d > 90\%$ but at a lower received power, -84dBm using 4 CS measurements. Both figures use 25 samples per measurement (n_s=25).

Two incident signals were applied to the DSIC in Fig. 6. In *CBF-reception mode*, only the in-beam signal is received. When *CS-DoA mode* is activated, both signals are received, showing that in 1us or less, the DSIC can switch from receiving to scanning mode (and vice-versa).

VI. COMPARISON TO THE STATE OF THE ART

In Table I we estimate the performance of a CBF-based DoA scanner using published 4-antenna CBF-receiver chips for the comparison to the presented CS-DoA DSIC scanner. We assume an 8-antenna DoA scanner identifying one signal among 8 scan angles. For all scanners, we use n_s=25 samples and f_s=50MHz so an angle scan-time of 500ns. The DSIC with CS-DoA requires two CS measurements, requiring a total scan-time of 1us. As a result, the presented CS-DoA approach offers a much faster estimate of the DoA of the signal with a significantly lower energy. Also shown in Table I are extrapolated measurements from calculated data for 32 and 64 antennas.

VII. CONCLUSIONS

The DSIC is able to operate in two main modes, *CS-DoA mode* for rapidly scanning the spatial environment, and *CBF-reception mode* for reception in one direction. Using CS-DoA, the DSIC can trade-off sensitivity for the ability to sense all scan-angles simultaneously, allowing it to detect signals faster and more efficiently than the current state-of-the-art (SoA). In *high-energy-efficiency CS-DoA mode*, a single SOI with incident power above -60dBm can be recovered with as little as 2 CS measurements and in 1us. This is 4x faster and at least 1.5x more energy efficient when compared to multi-antenna swept CBF scanners using receivers from [1], [2], or [3]. While 4 CS measurements are needed in *high-sensitivity CS-DoA mode* for finding multiple signals (as low as -84dBm), the DSIC is still 2x faster than comparable CBF scanners. For applications using large antenna arrays ($>$ 32 antennas), the DSIC's energy efficiency is an order of magnitude better than similar architectures used for DoA finding.

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