8.4 Fully Integrated Buck Converter with 78% Efficiency at 365mW Output Power Enabled by Switched-Inductor-Capacitor Topology and Inductor Current Reduction Technique

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Fully integrated buck converters can improve performance and reduce the power consumption of system-on-chip by providing point-of-load regulation with dynamic voltage scaling [1]. As a core component of a buck converter, an inductor with large inductance and small resistance is desirable for high power efficiency, but on-chip inductor integration is challenging due to silicon-area constraints and parasitic effects. Common techniques to integrate on-chip inductors include using on-die spiral inductors [1-3], package bond wires [4], and magnetic cores [5,6], resulting in inductors on the order of nH with resistances of several hundred mΩ. Switching frequencies approaching 100MHz and beyond are often used to reduce the current ripple of such small inductors [1-6] at the cost of switching loss. A special hybrid topology, known as a 3-level converter, has been shown to reduce inductor current ripple and the associated power loss by doubling the effective switching frequency [1]. Compared to the conventional buck converter, the 3-level topology uses two more power switches that contribute toward switching loss and conduction loss. Some other hybrid topologies have demonstrated unique characteristics and benefits [7], but none have been proposed to improve the performance of fully integrated buck converters.

This paper presents a switched-inductor-capacitor (SIC) step-down converter that can improve power efficiency by reducing the average current of on-chip inductors relative to the load current. Figure 8.4.1 illustrates a diagram of the converter consisting of a power stage, switch drivers, and a feedback controller. The core devices of the power stage include inductor L, flying capacitor C_{FLY}, output capacitor C_{OUT}, and three power switches that are controlled in two phases by a PWM signal with frequency f_{SW} and duty-cycle D. In contrast to the conventional buck converter, the SIC topology places the inductor at the input instead of the output, effectively reducing the inductor average current relative to the load current. Thus, for a specific load, the SIC converter endures lower power loss from its inductor. The working principle of the SIC converter in steady-state is shown in Fig. 8.4.2. In phase 1, switches ϕ_{1HI} and ϕ_{1LO} are turned on for a duration of D/f_{SW}, and current I_L through inductor L increases by ΔI_{L1} with slope S_{L1}. In phase 2, switch ϕ_2 is turned on for a duration of $(1–D)/f_{SW}$, and I_L decreases by ΔI_{L2} with slope S_{L2}. The relationship between V_{IN} and V_{OUT} can be derived as $V_{OUT}=V_{IN}/(2\text{-}D)$ by applying inductor volt-second balance. Therefore, the voltage conversion ratio, $VCR=V_{OUT}/V_{IN}$, can be adjusted from 1/2 to 1 by controlling the duty-cycle D from 0 to 1. The error amplifier produces an error signal from the difference between V_{OUT} and the reference voltage, V_{REF}. From the error signal and a 450MHz ramp signal, the comparator outputs a PWM signal to drive the power switches such that V_{OUT} is regulated to V_{REF}.

The average inductor current of the SIC converter can theoretically be expressed as $I_{L,DC}=VCR\times I_{OUT}$ because $V_{IN}\times I_{IN}=V_{OUT}\times I_{OUT}$ and $I_{IN}=I_{L,DC}$. In contrast, the average inductor current of the conventional buck converter and the 3-level converter is equal to I_{OUT}. Since VCR is smaller than 1 for a step-down conversion, the SIC converter has lower average inductor current and lower conduction loss than the other two converters. Figure 8.4.3 illustrates the current flows in each of the three converters. All current paths in the 3-level converter include three resistive elements in series, i.e., two power switches and one inductor. In contrast, any current path in the conventional buck converter and the SIC converter only includes two resistive elements in series, i.e., two power switches in series or one power switch and one inductor in series. Thus, the power switches in the conventional buck converter and the SIC converter can be sized smaller for lower conduction loss and lower switching loss. With proper switch sizes and switching frequency, the SIC converter can outperform the conventional buck converter and the 3-level converter in terms of power efficiency.

To verify the concept, all three types of converters using identical inductors were simulated under the same supply voltage and load conditions, and the performance metrics were compared by observing the conduction loss of the inductors and the power switches. The inductors have conduction loss arising from the average current ($I_{L,DC}$) and current ripple (ΔI_L), and the power switches have both conduction loss and switching loss. The buck converter, the 3-level converter, and the SIC converter were designed to operate at 654MHz, 178MHz, and 450MHz, respectively, to have similar inductor current ripple and similar power losses from the switches. Figure 8.4.4 shows the simulated inductor currents, power losses, and power efficiencies of the three converters. The SIC converter outperforms the other two at any VCR between 1/2 and 1 due to the lower average current through the inductor and fewer resistive components in the current paths.

The SIC converter was fabricated in a 65nm CMOS process with an area of $1.3\times0.5mm^2$, excluding test pads. By using a top metal layer, the inductor was designed to have an inductance of 0.85nH and a resistance of 340mΩ at 450MHz. The flying capacitor C_{FLY} and the output capacitor C_{OUT} were 1.72nF and 3.1nF, respectively, implemented by metal-oxide-semiconductor capacitors and metal-oxide-metal capacitors, with a capacitance density of $10nF/mm^2$. The substrate-coupling capacitance of the bottom plate of C_{FLY} is 30pF. The power loss from switching this parasitic capacitance at 450MHz is 2.4mW, 3.3mW, 4.3mW, and 5.5mW at V_{OUT} = 600mV, 700mV, 800mV and 900mV, respectively, which contributes to less than 10% of the total power loss. Charge-sharing loss between the C_{FLY} and C_{OUT} is found to be insignificant, on the order of microwatts. Due to conduction loss of the inductor and power switches, V_{OUT}=600mV can be produced with a duty cycle of 12%. Figure 8.4.5 shows the measurement results, including power efficiency, load transient response, reference tracking, and output voltage ripple at V_{IN}=1.2V. A peak efficiency of 78% is measured at an output voltage of 900mV and a load current of 406mA. The transient response overshoot is between 16.1% for a 3.6× load step at 900mV and 20% for a 6.1× load step at 600mV. The reference tracking response shows a rising time of 40ns and a settling time of 300ns. In steady-state, the output voltage ripple is below 56mV for the entire range of output voltages and load currents. Figure 8.4.6 summarizes the performance of the SIC converter against existing fully integrated buck converters. The SIC converter delivers the highest power and current density while maintaining comparable power efficiency to the best of the class.

Acknowledgements:
This work was supported in part by the U.S. NSF under Grants CNS-1705026, the gift funding from Intel Corporation, and the NSF Center for Design of Analog–Digital Integrated Circuits (CDADIC).

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 978-1-5386-8531-0/19/$31.00

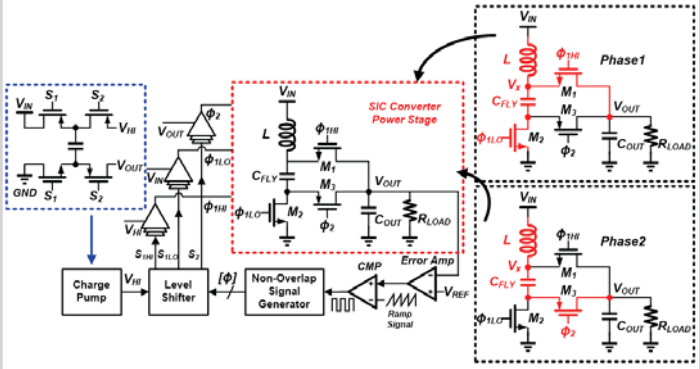

Figure 8.4.1: Block diagram and basic operation of the SIC converter.

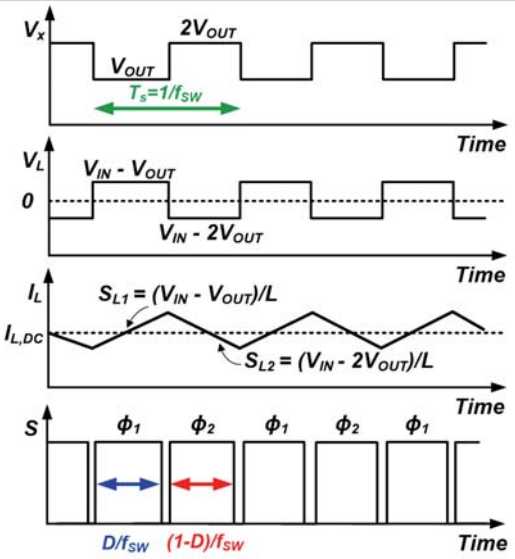

Figure 8.4.2: Steady-state operation of the SIC converter.

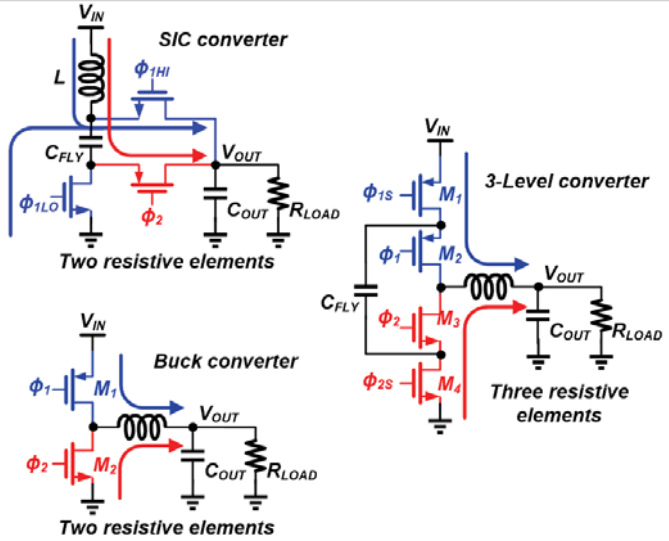

Figure 8.4.3: Current paths in the SIC converter, the 3-level converter, and the buck converter.

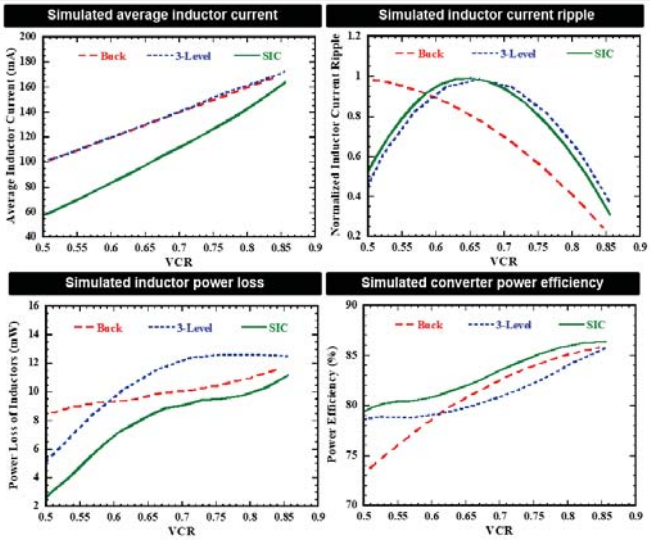

Figure 8.4.4: Comparison of the inductor current, current ripple, and power loss, and the power efficiency of the three converters in simulation.

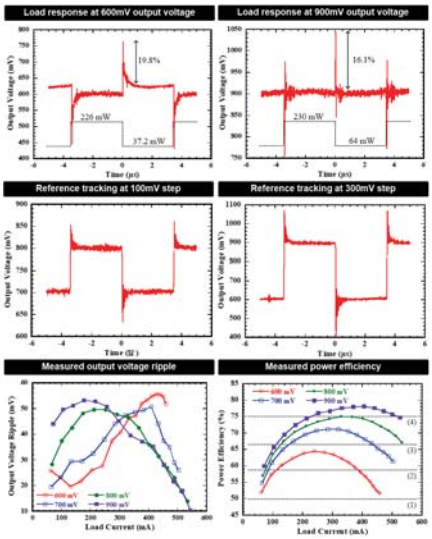

Figure 8.4.5: Measured load response, reference tracking, output voltage ripple, and power efficiency at V_{IN}=1.2V.

	[1]	[2]	[3]	[5]	This Work
Process (nm)	130	22	130	180	**65**
Topology	3-Level	Conventional Buck	Conventional Buck	R²SC*	**SIC**
Supply Voltage (V)	2.4	1.5	1.2	1.8	**1.2**
Output Voltage (V)	0.4 – 1.4	1	0.3 – 0.9	0.1 – 1.5	**0.6 – 0.9**
Frequency (MHz)	50 – 240	500	170	1 - 100	**450**
Number of Phases	4	1	1	1	**1**
Total Ind. (nH)	4	1.5	4	18	**0.85**
Total Cap. (nF)	28	10	5.2	3	**4.82**
Max Load Current (mA)	800	250	350	120	**533**
Max Output Power (mW)	1000	250	315	210	**475**
Output Ripple (mV)	< 100	~ 10	~ 40	NA	**< 56**
Area (mm²)	5	1.5	1.5	NA	**0.65**
Power Density (mW/mm²)	200	167	210	210	**730**
Current Density (mA/mm²)	160	167	233	140	**820**
Eff. @ Max Power (%)	63	N/A	76	NA	**74.6**
Peak Eff. (%)	77	68	77.9	73.3	**78**
EEF**	0.15 – 0.5	0.02	0 – 0.56	-0.06 – 0.36	**0.04 – 0.22**

* Recursive resonant switched capacitor converter (R²SC) with an on-package inductor

** Efficiency enhancement factor: $EEF = 1 - Efficiency_{LDO}/Efficiency_{Converter}$

Figure 8.4.6: Performance summary of the SIC converter and comparison with prior art.

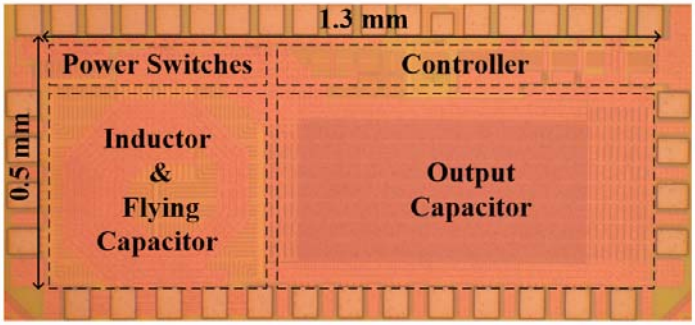

Figure 8.4.7: Die micrograph of the SIC converter fabricated in a 65nm CMOS process.

978-1-5386-8531-0/19/$31.00