# A Sub-1V Analog-Assisted Inverter-Based Digital Low-Dropout Regulator with a Fast Response Time at 25mA/100ps and 99.4% Current Efficiency

Bai Nguyen, Nghia Tang, Zhiyuan Zhou, Wookpyo Hong, and Deukhyoun Heo
Dept. Electrical Engineering and Computer Science
Washington State University
Pullman, WA 99164, USA
bai.nguyen@wsu.edu

Yangyang Tang and Philipp Zhang
HiSilicon Technologies Co., Ltd.
Shenzhen 518129, China

***Abstract*— To mitigate large voltage droop caused by sub-ns dynamic current transitions in system on chips (SoCs), this paper proposes a fully integrated analog-assisted inverter-based digital low dropout regulator (LDO) to obtain a fast response time with 160mV droop at 25mA/100ps featuring 99.4% current efficiency, and 16mV DC load regulation in sub-1V operating range by using a dynamic-step quantizer and a trip-point controller. The proposed quantizer is implemented with an inverter-based flash ADC to achieve high speed without consuming large power while the trip-point controller corrects the DC error of the inverter-based ADC. Besides, the assistant analog LDO is employed to provide fine-grain regulation and remove ripple from the output voltage.**

***Keywords—fast transient response; digital low-dropout regulator; analog-assisted digital LDO; inverter-based flash ADC; dynamic-step quantizer***

## I. INTRODUCTION

To reduce the number of external passive components and suppress voltage ringing caused by parasitic inductance on power supply rails, fully integrated low-dropout regulators (LDOs) are widely employed in modern SoCs [1]. However, as the switching activity of digital circuits in SoCs tends to generate highly dynamic load current changing within a few hundred ps [2], voltage regulators require an extremely fast response to minimize output voltage ($V_O$) droop due to small on-chip output capacitor ($C_O$) [3]. Previous high-speed LDOs employ either output drivers with replica biasing [4] or high-side power NMOS with NAND-based control [5]. However, these designs have relatively poor load regulation (e.g. 60mV DC variation of $V_O$ in [5]). A dual-loop comparator-based architecture [2] improves the load regulation at the cost of low current efficiency (77.5% peak) because of high switching loss at steady state. The LDO with tri-loop control [3] shows 105mV droop against a 10mA load step with 1ns rise time, and this is significantly longer than the load rise time expected in SoCs. In this work, an analog-assisted inverter-based (AA-IB) digital LDO is introduced, featuring a dynamic-step quantizer and trip-point modulator (TPM) to achieve fast response while maintaining high efficiency and power integrity.

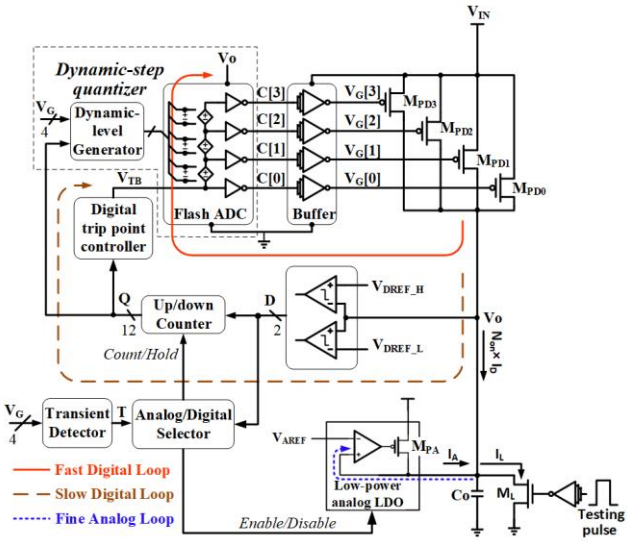



Fig. 1. System architecture of the proposed LDO

## II. THE PROPOSED LDO

### A. System Architecture of the Proposed LDO

Fig. 1 illustrates the overall architecture of the proposed AA-IB LDO consisting of three loops: a fast digital loop controlled by an IB flash ADC, a slower digital loop operated by a double-bound (DB) digital controller, and a fine analog loop implemented by an assistant low-power analog LDO. Design techniques for flash-ADC based LDO [1], shift-register based LDO [1, 3], and analog LDO [3] are applied to ensure the stability of these loops. The IB flash ADC consists of four IB comparators $CMP_{0\text{-}3}$, as shown in Fig. 2. Each $CMP_i$ is an inverter with its gate biased by $V_{TB}$ from the TPM, and the input of this comparator is the positive power supply rail of the inverter that is directly connected to $V_O$ to form a fast feedback path. Different trip points $V_{TP0\text{-}3}$ of $CMP_{0\text{–}3}$ are created by different width ratios $(W_P/W_N)_{0\text{-}3}$ of $M_{P0\text{-}3}$ and $M_{N0\text{-}3}$ in Fig. 2. Then, $V_O$ is compared with $V_{TP0\text{-}3}$ to generate a thermometer code $C[0{:}3]$ that is then inverted and buffered into $V_G[0{:}3]$ to control the number of turned-on power MOSFETs ($M_{PD0\text{-}3}$).

Operation of this LDO is explained in detail during both steady state and transient events.

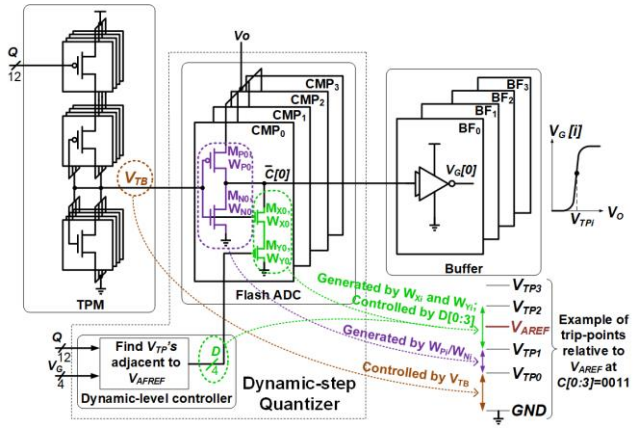



Fig. 2. Circuit implementation of the trip-point controller and dynamic-step quantizer

## B. Steady State of the LDO

In steady state, $V_G[0:3]$ is settled to one of the thermometer codes shown in Fig. 3 while $V_{TP0\text{-}3}$ are set to respective levels and $V_O$ is regulated to the target voltage $V_{AREF}$. $M_{PDi}$ is turned on if $V_{TPi} > V_O$, or off otherwise. The analog LDO is sized such that the peak value of its output current ($I_A$) is equal to the current of one turn-on $M_{PDi}$ ($I_D$). For a given number of turn-on $M_{PD}$ devices ($N_{on}$), the total output current of the LDO is $I_O = N_{on} \times I_D + I_A$, with $0A < I_A < I_D$. Because of the continuous nature of $I_A$, the LDO can deliver a continuous range of load current between 0A and $5 \times I_D$ without output voltage ripple in the steady state.

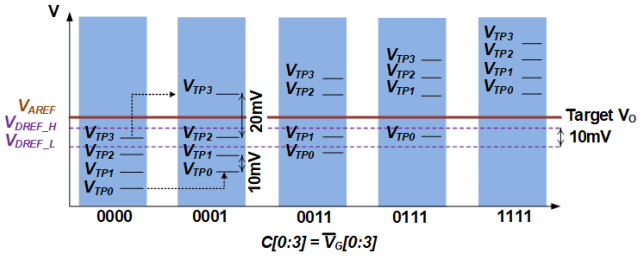



Fig. 3. Dynamic quantization steps

## C. Dynamic Behavior at Transient Events

When the load current $I_L$ rises (falls), $V_O$ quickly decreases (increases), crosses the trip points below (above) $V_{AREF}$ (e.g. $V_{TP0\text{-}2}$ in Fig. 4 when $I_L$ rises during a transient event), and changes $V_G[0:3]$. Accordingly, more of $M_{PD0\text{-}3}$ are turned on (off) to deliver more (less) output current, and $V_O$ stops decreasing (increasing) when $I_O > I_L$ ($I_O < I_L$). Afterward, $V_O$ cycles around a particular $V_{TPi}$ below $V_{AREF}$ (e.g. $V_{TP0}$ in Fig. 4) as $V_G[0:3]$ fluctuates between two adjacent values, toggling one of $M_{PD0\text{-}3}$ continuously such that the average $I_O$ is equal to $I_L$. At that point, the analog LDO tends to pull up (down) $V_O$ to $V_{AREF}$ but the stronger digital LDO holds $V_O$ at a lower (higher) level corresponding to the $N_{on}$ required to deliver new $I_L$ since $N_{on}$ is determined by the number of $V_{TPi}$ above $V_O$. The transient contention between analog and digital loops is resolved by temporarily disabling the analog LDO, and the system decides when to disable the analog LDO based on bit $T$ of the transient detector, which senses the toggling activity of $V_G[0:3]$. To bring $V_O$ back to $V_{AREF}$, $V_{TP0\text{-}3}$ are then shifted up (down) by the DB digital controller, which increments (decrements) a 12-bit code $Q$ and raises (reduces) $V_{TB}$. Since $N_{on}$ is determined by the number of $V_{TPi}$ above $V_O$, $V_O$ is shifted up (down) in accordance with $V_{TPi}$ to maintain the required $N_{on}$ until $V_O$ is bounded between $V_{DREF\_L}$ and $V_{DREF\_H}$. Afterward, the DB digital controller is disabled to hold the code $Q$ and keep $V_{TPi}$ levels unchanged. The analog LDO is then enabled to pull $V_O$ to $V_{AREF}$ and completes the load regulation. In steady state, the analog LDO and the digital LDO together satisfy the required load current, i.e., $I_L = I_O = N_{on} \times I_D + I_A$. The current from the analog LDO replaces the fractional current from the toggling $M_{PDi}$ to fill in the gap between $N_{on} \times I_D$ and $I_L$. Therefore, $M_{PDi}$ stops toggling, and $V_O$ is free of ripple. Because the analog LDO can only source a positive current, the two bounds $V_{DREF\_H}$ and $V_{DREF\_L}$ should be lower than $V_{REFA}$ so that $V_O$ will be only pulled up to $V_{REFA}$ when the analog LDO is reenabled. By placing $V_{AREF}$ above $V_{DREF\_H}$, this LDO can eliminate the voltage ripple in a similar manner to the digitally-assisted LDO formed by a combination of the comparator and the amplifier in [6].

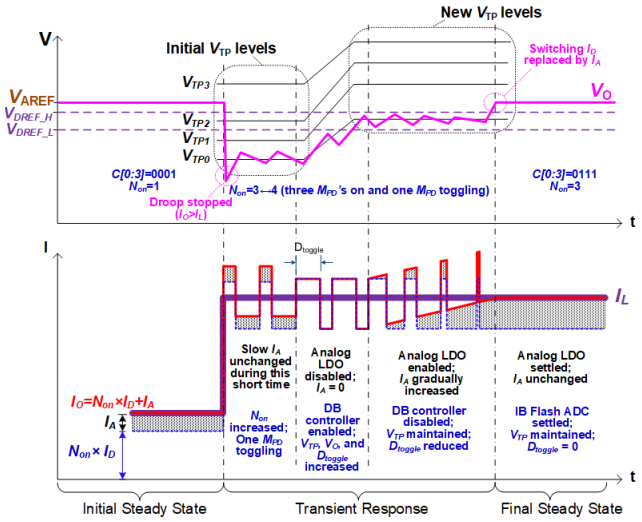



Fig. 4. A transient example for $C[0:3]$ changing from 0001 to 0111

To assure that none of $M_{PD0\text{-}3}$ toggles in steady state, there should be a sufficiently large margin between $V_{AREF}$ and adjacent $V_{TPi}$ for any $C[0:3]$. A simple approach to provide this assurance is to increase the quantization step size of $V_{TP0\text{-}3}$ at the cost of a bigger voltage droop at transient events. To avoid this compromise, a dynamic-step quantizer is proposed as illustrated in Fig. 2 and Fig. 3. The figures show that the step sizes are unequal and dynamically varied with respect to $C[0:3]$ such that the step between $V_{TP}$'s adjacent to $V_{AREF}$ is large (eg. 20mV) while those between the other $V_{TP}$'s are small (eg. 10mV). This mechanism is realized by the circuit in Fig. 2. $V_{TB}$ is adjusted by changing the pullup strength of a self-connected inverter in the TPM, thus shifting $V_{TP0\text{-}3}$ by the same amount. In this case, $V_{TB}$ can be considered as a common adjustable offset for $V_{TP0\text{-}3}$. On the other hand, $M_{Xi}$ and $M_{Yi}$ are utilized to control the pulldown strength of each inverter in $CMP_i$, thus its individual $V_{TPi}$ level, depending on the status of $C[0:3]$. Turning on/off these transistors hence dynamically resizes the gap between $V_{TP}$'s

levels adjacent to $V_{AREF}$, and the synthesized step patterns corresponding to different values of $C$[0:3] are shown in Fig. 3.

## III. Measurement Results

The proposed LDO has been fabricated in the 130nm CMOS process, and the micrograph of the chip is presented in Fig. 5. To generate a sharp rise/fall edge of $I_L$, a tapered inverter chain is employed to quickly switch on/off an on-chip NMOSEFT ($M_L$) used as a load device. Then, the performance of the LDO is verified in the measurement.

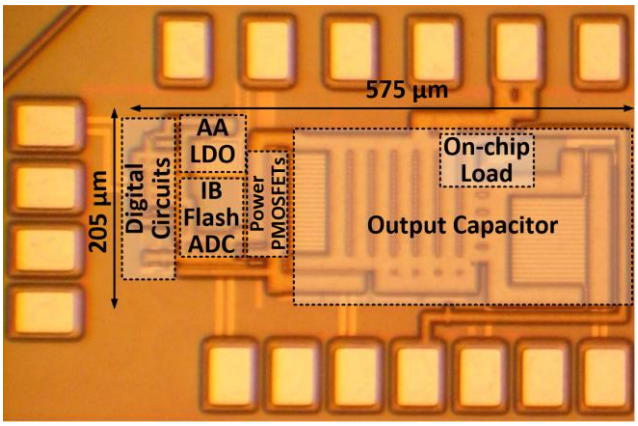



Fig. 5. Micrograph of the fabricated chip

The current efficiency of the proposed LDO is depicted in Fig. 6. The LDO achieves fast response without consuming much power thanks to the low-power high-speed IB flash ADC, which draws a small current ranging from 10 – 90 µA (depending on levels of $V_{TPi}$, which are determined by the load current) per 4 bits. The current efficiency of this LDO peaks to 99.4% at full load condition.

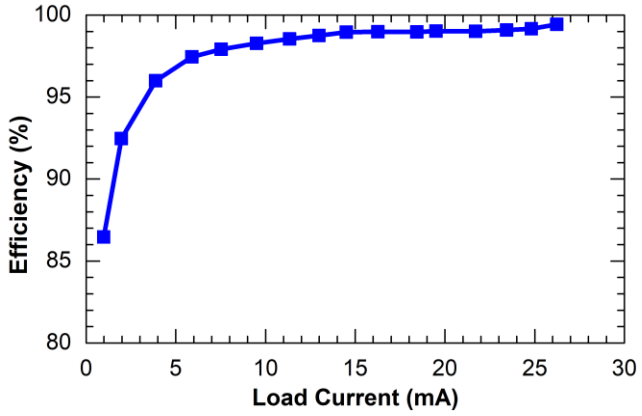
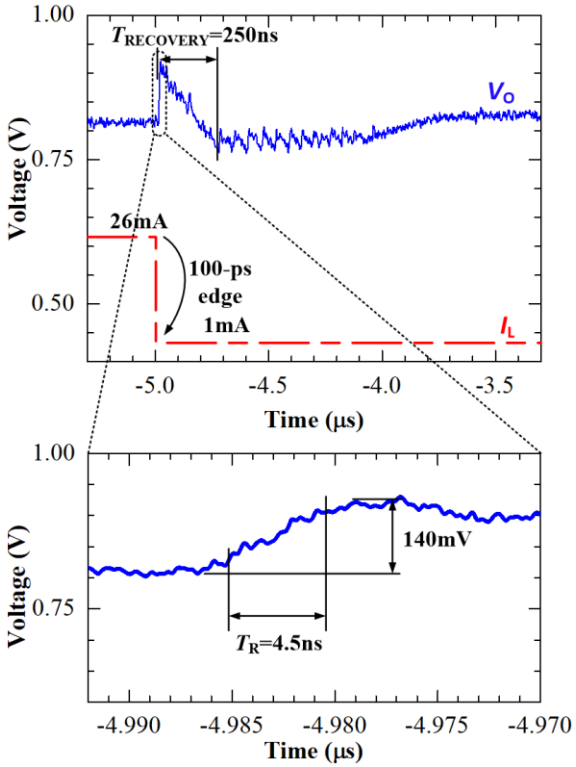
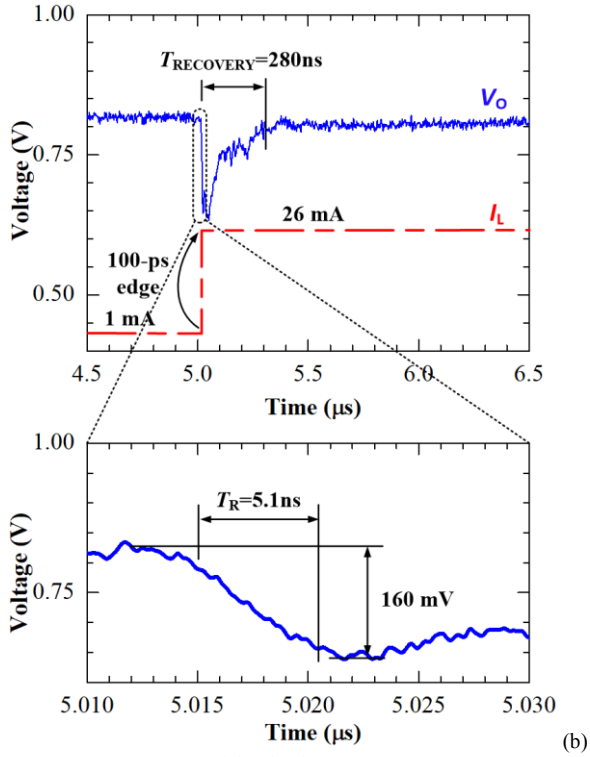



Fig. 6. Measured current efficiency

Fig. 7 shows the measurement results of the transient response at 1V input and 0.8V output. When $I_L$ drops from 26mA to 1mA in 100ps, the overshoot is clamped to 140mV with 4.5ns response time. In contrast, when $I_L$ rapidly rises from 1mA to 26mA within 100ps, the voltage droop is limited within 160mV and the respective response time is 5.1ns. In fact, IB comparators of the flash ADC create only 1-ns delay. Nevertheless, most of the total 5.1ns transient response time resulted from the delay of the buffer from the output of this ADC to the power MOSFET.




(a) Falling load current




(b) Rising load current

Fig. 7. Measured transient response

Table I shows a comparison chart. Regarding transient response testing, previous works have used a long $T_{EDGE}$ of $I_L$ in ns range to report a low voltage droop ($\Delta V_O$) and short response time ($T_R$) calculated by the following equation: $T_R=\Delta V_O \times C_O/\Delta I_L$ (while ignoring $T_{EDGE}$). In contrast, this work has applied a testing $T_{EDGE}$ on the order of ps. Besides, the proposed work offers significantly better load regulation compared with [5] (e.g. 16mV vs. 60mV). In addition, significant ripple is generated in [2] (e.g. 28mV) while the proposed LDO is ripple-free in the steady state due to the continuous current delivered by the AA LDO. This mechanism also eliminates the switching loss in power MOSFETs that has been encountered in [2]. On the other hand, pure analog approach in [4] requires a large voltage headroom, thus high operating voltage (e.g. 3.6V input and 1.8V output), making it not suitable for the low-voltage processes utilized in modern SoCs. In contrast, the AA LDO in the proposed architecture only delivers a small fractional output current so it does not require a big overdrive voltage. As a result, the proposed hybrid LDO can work at low input (e.g. 0.83 – 1V) and output (e.g. 0.6 – 0.8V) voltage levels. Besides, the current efficiency and recovery time ($T_{RECOVER}$) of this work outperform all the others.

## IV. Conclusion

This paper presents a fast response analog-assisted digital LDO including three key components: a low-power high-speed IB flash ADC to achieve rapid transient response without compromising the power consumption, a digital controller to correct the DC level of $V_O$, and an assistant low-power analog LDO to provide fine-grain regulation and eliminate voltage ripple. To fully validate the speed of the dynamic response, an on-chip load has been implemented to generate a sharp step load current at a slew rate of 25mA/100ps. In addition, the measurement results show a droop voltage of 160mV and 5.1ns response time. In addition, this LDO demonstrates a high current efficiency, up to 99.4% at full load as well as a small DC voltage variation of 16mV over the whole load range. This proposed structure overcomes the conventional design trade-off among the dynamic speed, power consumption, and power integrity.

## Acknowledgment

This work was supported in part by the U.S. NSF under Grants CNS-1705026, the gift funding from Intel Corporation, and the NSF Center for Design of Analog–Digital Integrated Circuits (CDADIC).

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Table I. Pefromance comparison of LDOs

| Parameters | This work | [2] | [3] | [4] | [5] |
|---|---|---|---|---|---|
| Process | **130nm** | 65nm | 45nm | 180nm | 28nm |
| $\Delta I_L/T_{EDGE}$ | **25mA/100ps** | 36mA/4ns | 10mA/1ns | NA | 20mA/3ns |
| $\Delta V_O$ @ $\Delta I_L/T_{EDGE}$ | **160mV** | 7.6mV | 105mV | 180mV | 117mV |
| $T_{RECOVERY}$ | **280 ns** | NA | 3us | NA | 9us |
| Load regulation | **16mV** | 9.8mV | NA | NA | 60mV |
| Total capacitor | **800 pF** | 1.46nF | 100pF | 50pF | 24pF |
| Input voltage | **0.83 – 1V** | 1.179 – 1.625V | 0.5 – 1V | 3.6V | 0.4 – 0.55V |
| Output voltage | **0.6 – 0.8V** | 0.9 – 1V | 0.45 – 0.95V | 1.8V | 0.35 – 0.5V |
| Output ripple | **Ripple-free**† | 28mV | NA | NA | NA |
| Current efficiency | **99.4%** | 77.5% | NA | 90% | NA |

† At steady state