A 25–35 GHz Neutralized Continuous Class-F CMOS Power Amplifier for 5G Mobile Communications Achieving 26% Modulation PAE at 1.5 Gb/s and 46.4% Peak PAE

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***Abstract*— This paper presents a high-efficiency neutralized continuous class-F (CCF) CMOS power amplifier (PA) design technique for millimeter-wave (mmW) 5G mobile communications. A parasitic-aware tuned-load with a high-order harmonic-resonance network is proposed to shape the current and voltage waveforms for the CCF PA. At mmW frequencies, the gate–drain capacitance (C_{gd}) creates adverse capacitive loading on harmonic-tuned output load networks. As a result, a CCF PA suffers from compromised power efficiency. To address this, we integrate a transformer with a tunable coupling coefficient between gate–drain of the power-device. This proposed technique allows accurate neutralization of C_{gd}, reducing detrimental loading effect on harmonic-tuned load while enhancing power efficiency and stability. We fabricated a CCF PA in 65-nm CMOS technology achieving >40% power-added efficiency (PAE) over 33.3% fractional bandwidth (25–35 GHz) and 46.4% peak PAE at 29 GHz. The measured peak saturated output power ($P_{o,sat}$) is 14.8 dBm at 30 GHz. The PA is tested with 64-quadrature-amplitude-modulated signal at a data rate of 1.5 Gb/s. Under this test setup, the PA achieves modulated PAE of 26%/24%/21.4% and average output power ($P_{o,avg}$) of 9.2/8.8/8.6 dBm at 28, 32, and 34 GHz, respectively, while maintaining better than −25 dB of error vector magnitude and −27 dBc of adjacent channel leakage ratio. To the authors' knowledge, this design presents one of the highest reported PAEs among mmW CMOS PAs.**

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***Index Terms*— 5G, CMOS, millimeter wave (mmW), 28 GHz, continuous class-F, inverse class F, power amplifier (PA), mobile communications, cellular, high efficiency, stability, neutralization, phased-arrays, wideband, tunable coupling coefficient, beamforming, tunable transformer, error-vector-magnitude (EVM), MIMO, quadrature-amplitude-modulation (QAM).**

I. Introduction

With the race to millimeter-wave (mmW) fifth generation (5G) wireless technology, implementation of highly power-efficient transceivers has become an important research topic [1]–[6]. Particularly, the design of high-efficiency power amplifier (PA) for 5G mobile communications in CMOS technology is in paramount importance as it offers longer battery life and improved thermal management at a low cost in portable devices [7]–[10]. At the same time, a PA with a large bandwidth is highly desirable for 5G mobile communications as it can cover multiple-wideband channels while ensuring robust performances against process-voltage-temperature (PVT) variations [8], [10]–[17].

Harmonically-tuned PAs are often developed to achieve high efficiency. Recently, several high-efficiency tuned mmW PAs have been demonstrated based on class-E [18]–[20] and inverse class-F (class-F^{-1}) [21], [22] topologies using CMOS and SiGe technologies respectively. However, the reported high efficiency is achieved only over a narrowband range. This limited-band performance is mainly attributed to the inherent architectural limitations associated with narrowband tuned-load based class-E and class-F/F^{-1} PAs. In addition, another work is also reported recently to improve the efficiency over a wide bandwidth at mmW frequencies using continuous class-AB mode [11].

At low-GHz frequencies (0.5-3 GHz), continuous class-F (CCF) PAs show promising high efficiency over one-octave/multi-octave bandwidth by waveform engineering of the voltage signal at the drain terminal of a standard class-F PA using GaN HEMT devices [23]–[27]. In the context

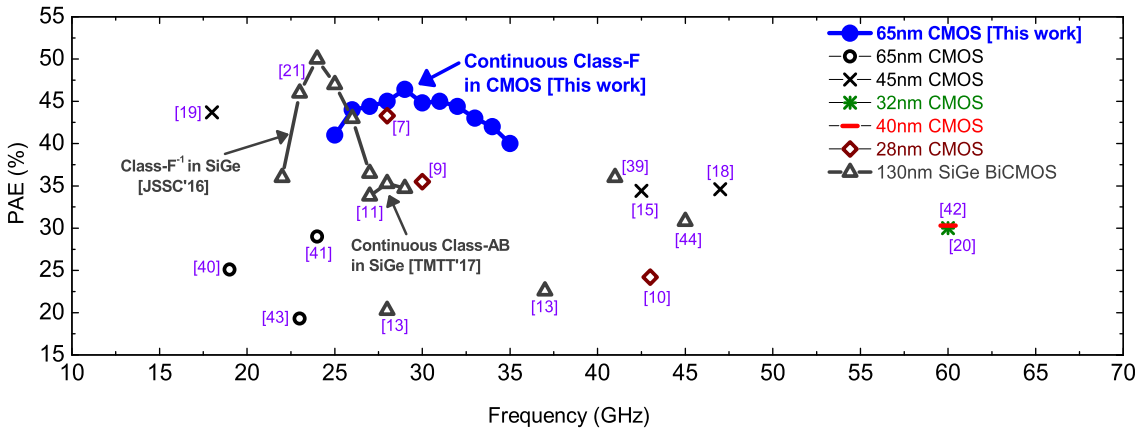


Fig. 1. Measured power added efficiency (PAE) comparison with recently reported state-of-the-art mmW silicon PAs.

of 5G communication a CCF PA can facilitate multiple advantages. Such as, very high efficiency can be demonstrated thus increasing the battery life of the future smart portable devices. Moreover, high efficiency can be maintained over a large bandwidth therefore supporting high data rates at a high efficiency level. So far, no research effort is presented at mmW frequencies for realizing integrated CCF PA in silicon technologies. This is partly because highly efficient CCF PA design requires precise reactive load mapping at fundamental (f_o) and 2nd harmonic ($2f_o$) bands which is difficult to achieve in silicon technologies due to large parasitic capacitances associated with power device. Specifically, the large C_{gd} in deep-submicron CMOS power device creates an undesirable capacitive loading-effect on harmonic-tuned load at drain terminal making it difficult to retain appropriate output load conditions [16], [28]. This effect severely compromises efficiency, degrades stability, and counteracts the benefits of a CCF PA at mmW frequencies. Prior arts reported C_{gd} neutralization using cross-coupled capacitors in differential amplifiers [7], [9], [16], [29], while single-ended amplifiers adopted transforms with fixed coupling coefficient [30], [31].

A literature survey of mmW PAs reveals that the concept of harmonic-tuned load network with tunable-neutralization is not reported in high-efficiency modes of PAs such as class-F, class-F^{-1}, class-E, etc. In this work, for the first time we present a comprehensive design guideline for practical realization of a CCF PA at mmW frequencies [32]. An in-depth analysis is performed to examine the adverse effect of C_{gd} on harmonic-tuned load using a deep-submicron CMOS power device. To address the solution, a parasitic-aware resonance-based harmonic-tuned load network and a transformer with a tunable coupling-coefficient are adopted. The operational principle and design methodology with necessary equations are discussed in-depth of the realized transformer. The tunability of the transformer enables accurate neutralization of C_{gd} over wideband by mitigating design limitations associated with inaccurate electromagnetic (EM) modeling of the device and interconnect parasitic, and mismatches due to PVT variations. The concept of series-parallel harmonic-resonance based tuned-load network in the context of a mmW CCF PA is investigated, and design equations are formulated. These techniques facilitate mapping of the required harmonic-tuned load at f_o (25-35 GHz) while generating the desired reactive load at $2f_o$ precisely, and a high impedance at the 3rd harmonic ($3f_o$). As a proof-of-concept, a CCF PA is fabricated in a 65-nm CMOS technology which achieves state-of-the-art PAE of 40-46.4% over 33.3% fractional BW at 30 GHz. To demonstrate its capabilities for 5G mobile communications, the PA is tested under 64-QAM signal with 250 MHz of channel-bandwidth (i.e., data- rate of 1.5Gb/s) at 28, 32 and 34 GHz and comprehensive measurement results of large-signal, error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) are presented. Fig. 1 shows the PAE comparison of the recently reported silicon PAs at mmW frequencies. The proposed CCF PA clearly demonstrates its high-efficiency over wide frequency range compared to recently reported high-efficiency PAs.

This paper is organized as follows. Section II discusses the limiting factors of CCF CMOS PA design at mmW frequencies. The proposed harmonic-tuned load network and C_{gd} neutralization transformer with tunable coupling coefficient is presented in Section III. Section IV demonstrates the implementation of CCF PA, while the measurement results and comparison are reported in Section V. Finally, the conclusions are summarized in Section VI.

II. Analysis of Limiting Factors of mmW CCF PA

The CCF PA offers a wide range of drain voltage (v_{DS}) waveforms which can be manipulated across the desired wide-bandwidth to maintain high-efficiency. The v_{DS} is defined as [23],

$$v_{DS}(\theta) = \left(1 - \frac{2}{\sqrt{3}}\cos\theta + \frac{1}{3\sqrt{3}}\cos 3\theta\right)(1 - \gamma \sin\theta) \quad (1)$$

where, γ is an empirical parameter with a range of, $-1 < \gamma < 1$ and θ is the phase angles of v_{DS}. This γ range is essential to maintain positive v_{DS} across all angles, otherwise, the drain current of device (i_{DS}) will drop to zero resulting dramatic reduction of power efficiency [23]. For $\gamma = 0$, it behaves as a standard class-F PA [23], while for all other values of γ (i.e., [-1 to 1, except 0]), the PA can maintain the same power efficiency as a standard class-F. Note that, i_{DS} remain

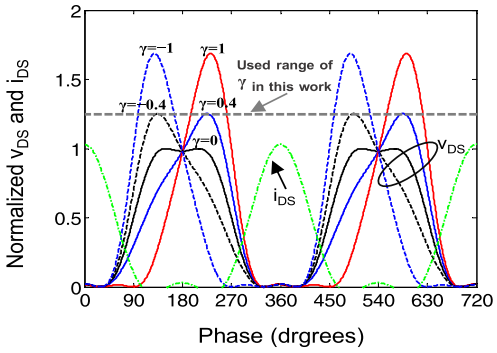


Fig. 2. Normalized drain voltage and current waveforms of a theoretical continuous class-F PA with marking the design range of γ as used in this work.

the same as a standard class-F (i.e., half-wave sinusoidal) for all conditions of drain voltage. Fig. 2 shows the theoretical drain voltage and current waveforms for $-1 < \gamma < 1$. The load impedances at fundamental, second and third harmonic bands (i.e., f_o, $2f_o$ and $3f_o$) for a CCF PA can be written from [24] as,

$$Z_{CCF,f_o} = \frac{2}{\sqrt{3}} R_{CCF} + jR_{CCF}\gamma \quad (2)$$

$$Z_{CCF,2f_o} = 0 - j(\pi/2) R_{CCF}\gamma \quad (3)$$

$$Z_{CCF,3f_o} = \infty \quad (4)$$

here, R_{CCF} is modeled as an unit resistive element to provide a relation between Z_{CCF,f_o} and $Z_{CCF,2f_o}$, and this can be obtained from class-B optimum fundamental load impedance [27]. The key to designing a CCF PA is changing the reactive part of the fundamental load (Z_{CCF,f_o}) while varying the phase of the 2nd harmonic load ($Z_{CCF,2f_o}$) as required by (2) and (3). Notice that, as shown in (3), a CCF PA can alleviate the strict requirement of a second-harmonic short impedance in comparison to a standard class-F mode (i.e., $Z_{CCF,2f_o}$ is short for $\gamma = 0$), thereby removing the requirements for narrowband resonators at 2nd harmonic impedance. As a result, the device and/or interconnect parasitic components can be modeled as an integral part of external harmonic-matching circuits to construct the drain voltage and current waveforms over a large bandwidth while maintaining high-efficiency. This is in part analogous to a class-J mode, which can alleviate the wideband PA performance limitations in a class-B/AB mode [33].

First three harmonic impedances are considered for this work as the inclusion of other high-order (such as, 4th) harmonic impedances complicates the load network design while delivering only an incremental improvement of efficiency (theoretically, ~3-4%) [27].

A. Effect of C_{gd} on Harmonic-Tuned Load

Fig. 3 shows the small-signal model of the simplified CCF PA core consisting of net gate-source (C_{gs}), drain-source (C_{ds}) and gate-drain (C_{gd}) parasitic capacitances (intrinsic and extrinsic) of a NMOS transistor used as a power device (M_1). The transconductance (g_m) and input resistance (R_{in}) of M_1,

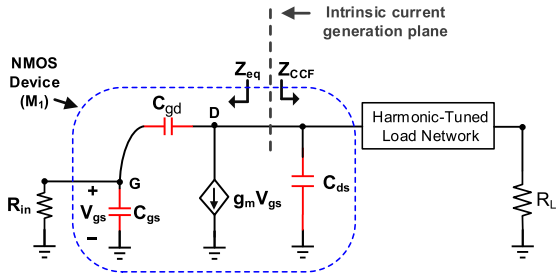


Fig. 3. Simplified small-signal circuit diagram of a CCF PA core to evaluate the loading effect of C_{gd} on harmonic-tuned load.

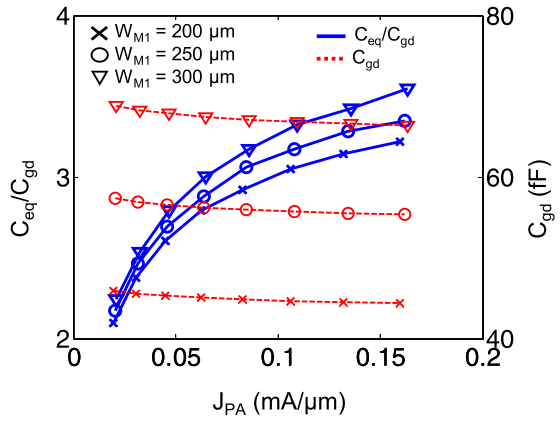


Fig. 4. Relations between current density, J_{PA}, C_{eq}/C_{gd} and C_{gd} for three different widths (W_{M1}) of transistor at 30 GHz using 65-nm CMOS.

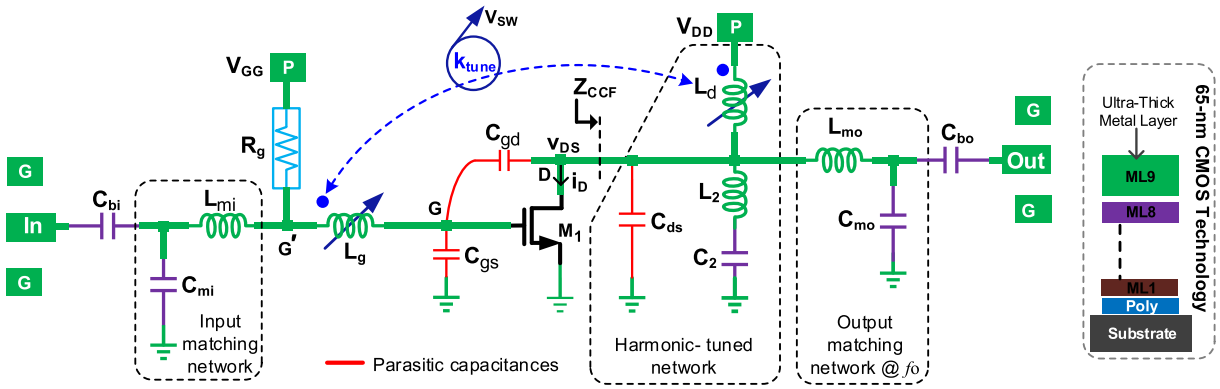
and load resistance (R_L) of the PA are also shown. To analyze the loading effect of C_{gd} on harmonic-tuned network, the net admittance looking into (i.e., left side) the drain terminal (D) is determined as,

$$Y_{eq} = \frac{\omega^2 R_{in}^2 g_m C_{gs} C_{gd}}{1+\omega^2 R_{in}^2 C_{gs}^2} + j\omega C_{gd}\left[1 + \frac{g_m R_{in}}{1+\omega^2 R_{in}^2 C_{gs}^2}\right]. \quad (5)$$

To simplify (5), the term $\omega^2 R_{in}^2 C_{gs}^2$ can be ignored, since $\omega^2 R_{in}^2 C_{gs}^2 \ll 1$ at mmW frequency. For example, at 30 GHz for $C_{gs} = 180$ fF and $R_{in} = 9.8\ \Omega$ (extracted from a 250 μm width of M_1 with a current density of 0.13 mA/μm), $\omega^2 R_{in}^2 C_{gs}^2$ becomes ~0.1. Thus, the equivalent capacitance looking into the drain terminal can be simplified as,

$$C_{eq} \approx C_{gd}[1+g_m R_{in}]. \quad (6)$$

Notice that, C_{eq} can be several times larger than C_{gd} in a practical PA design. To examine the practical range of C_{eq} in a 65-nm CMOS technology with a drain supply (V_{DD}) of 1.1 V, a study is performed using typical NMOS device widths (W_{M1}) of 200, 250 and 300 μm for mmW power-devices [7]–[10]. Each device is divided into 4 multipliers while each multiplier consists of 25 fingers. The selected gate width varies between 2 to 3 μm with a step of 0.5 μm. The g_m, C_{gd} and drain currents (I_D) are extracted from dc simulation. In addition, S-parameter simulation is performed at 30 GHz to extract R_{in}. Fig. 4 shows the current density (J_{PA}) versus ratio between C_{eq} and C_{gd} (i.e., C_{eq}/C_{gd}). As shown in this plot, for J_{PA} of 0.1-0.15 mA/μm,



Parameter	W_{M1} (μm)	L_{mi} (pH)	C_{mi} (fF)	L_g (pH)	L_d (pH)	L_2 (pH)	C_2 (fF)	L_{mo} (pH)	C_{mo} (fF)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	V_{DD} (V)	V_{sw} (V)	V_{GG} (V)	k_{tune}
Value	281.6	120	135	102	73	110	65	145	103	230	80	145	1.1	0.33	0.45	0.24

Fig. 5. Complete circuit diagram of the proposed CCF PA with net device parasitic capacitances (C_{gs}, $C_{gd}$and C_{ds}) in red color, and explicitly showing the used metal layers for components and interconnects in 65-nm bulk CMOS technology.

C_{eq}/C_{gd} varies between 3 to 3.5. Thus, the loading effect of C_{gd} at drain terminal is large. Note that, in the final PA prototype, J_{PA} of 0.13 mA/μm is used to achieve P_{out} of 14.8dBm while maximizing PAE.

This phenomenon can be viewed as an alternative representation of Miller-effect at drain terminal [34]. Due to this effect, the resonance frequency of tuned-load experiences a downward shift (i.e., at intrinsic current generation plane in Fig. 3) and creates a substantial mismatch in the output tuned-load network. This C_{gd} effect at drain terminal is substantially intensified in a deep-submicron CMOS technology due to the inability to predict it accurately. Because, the net C_{gd} (intrinsic and extrinsic) can vary significantly depending on device interconnect routings, PVT variation, and is not always readily captured by EM-simulation due to complexity and computational overheads. In the context of mmW CCF harmonic-tuned load network, this variation in C_{gd} can create large deviation of Z_{CCF} (in Fig. 3) from its desired value resulting compromised power-efficiency across the design range of γ.

B. Range of γ and Limited Quality Factor of Load Network

As shown in Fig. 2, with the increases of γ from 0 in either direction (+1 or −1), the drain voltage increases by a maximum factor of ∼1.7 compared to a standard class-F PA's drain voltage (i.e., $\gamma = 0$). Recently, reported state-of-the-art CCF PAs are designed using GaN-HEMT technology [23]–[27] which has a relatively large breakdown voltage (typically, 3-4 times of drain supply) and thereby GaN device does not experience reliability issue. In contrast, the deep-submicron CMOS devices pose long-term reliability concerns due to oxide-degradation and breakdown under large-signal operation. Therefore, for robust long-term operation of a PA in deep-submicron CMOS technology, maximum tolerable stress across oxide of a device should be considered in the initial design goals. In this work, we used 65-nm CMOS technology and the maximum tolerable dc stress across gate-drain (oxide) to ensure less than 0.01% failure over 10 years at 125°C is approximately 1.35 times of supply voltage (V_{DD}). This is determined using time-dependent dielectric breakdown (TDDB) and hot carrier injection (HCI) analysis as performed in [35]. Under this constraint, a reduced range of γ (i.e., $|\gamma| \leq 0.4$) is considered to realize the CCF PA. This range translates into an achievable fractional bandwidth of 40% (i.e., $0.8/2 = 0.4$) which is sufficient for 5G mobile communications [4], [6].

The low-quality factor (Q) of on-chip passive components at mmW frequencies poses another limiting factor to fulfill the low resistive (theoretically zero) load condition at $2f_o$ band as stated in (3). Although, in practice, loss is unavoidable in the output load-network, but it can be reduced to a tolerable level by judicially designing the harmonic-tuned network. For example, the device and interconnect parasitic components can be modeled as a main building parts of the harmonic-tuned load. This can simplify the CCF PA's load design and reduce the total number of external passive components, as a result, overall high-Q, and subsequently high power-efficiency in the output-load network can be achieved.

III. Proposed CCF PA

Fig. 5 shows the complete circuit diagram of the proposed CCF PA. Device parasitic capacitances (C_{gs}, C_{gd} and C_{ds}) and the used metal layers in 65-nm CMOS technology are shown in the schematic. The output load consists of a harmonic-tuned network for $2f_o$ and $3f_o$ bands, and a LC matching network for f_o band. A transformer with a tunable coupling-coefficient is integrated between drain and gate terminal to neutralize the adverse effects of C_{gd}. The input matching network consists of a LC matching circuit and the gate is biased through a resistor (R_g).

A. Series-Parallel Harmonic-Tuned Load Network

A series-parallel resonance network at the drain terminal of the power device (M_1) is realized using C_{ds}, L_d, L_2 and C_2,

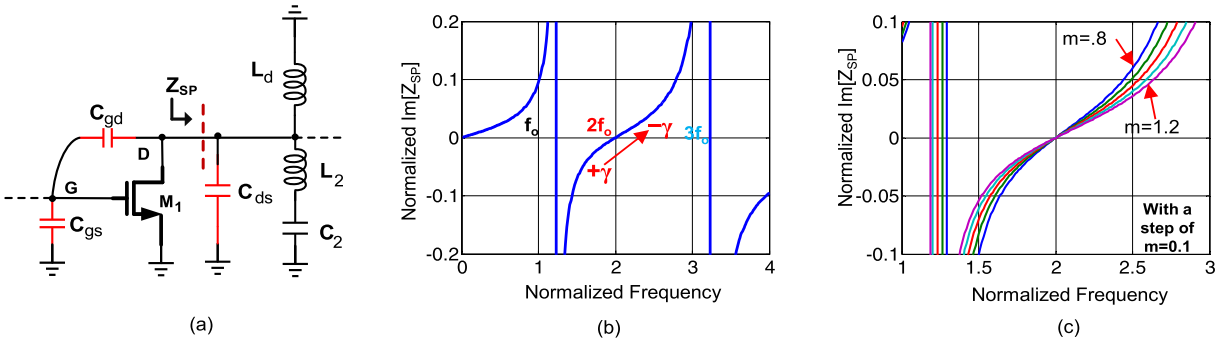


Fig. 6. (a) Simplified schematic of the series-parallel harmonic-tuned load network, (b) normalized Im[Z_{SP}] across normalized frequency, (c) relationship between m and Im[Z_{SP}].

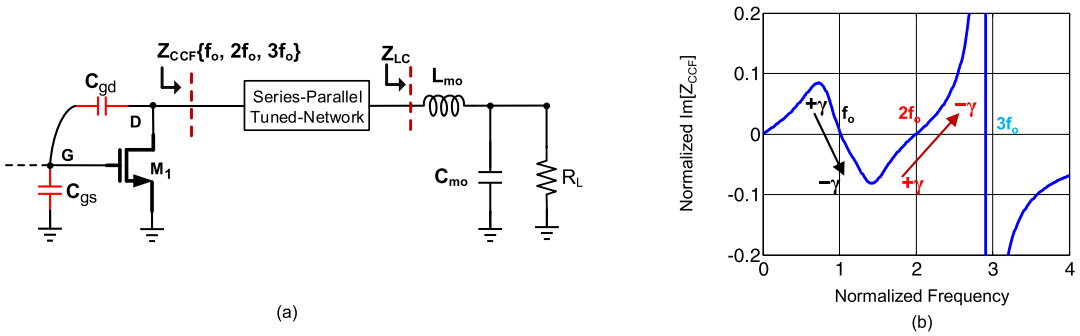


Fig. 7. (a) Simplified circuit diagram of the output load network including LC matching circuit, (b) Normalized Im[Z_{CCF}] across frequency to show the achieved phase relationship in reactive components as required by (2) and (3).

as shown in Fig. 6(a). A series resonance at $2f_o$ is created from L_2 and C_2 while simultaneously a parallel-resonance is obtained using L_d and C_{ds} at $2f_o$. Looking right to the drain terminal (node D), the combination of these two resonance networks (Z_{SP}) provides an inductive impedance with moderate magnitude at f_o, a low impedance at $2f_o$, and a high impedance at $3f_o$ bands as summarized in Fig. 6(b). In the context of load network of a CCF PA, realizing such a network has two-fold advantages. First, it allows to achieve the proper phase variation of Im[Z_{CCF}] at $2f_o$ band with γ (positive to negative) by changing it from a capacitive to an inductive load. Second, a high impedance condition at $3f_o$ band is obtained. A closed-form for Z_{SP} using C_{ds}, L_d, L_2 and C_2 is derived as,

$$Z_{SP} = \frac{j\omega L_d(\omega^2 L_2 C_2 - 1)}{\left[(\omega^2 L_2 C_2 - 1)(1 - \omega^2 L_d C_{ds}) + \omega^2 L_d C_2\right]}. \quad (7)$$

Here, L_d, L_2 and C_2 are defined as,

$$L_d = \frac{1}{4\omega_o^2 C_{ds}} \quad (8)$$

$$L_2 = \frac{1}{4\omega_o^2 C_2} \quad (9)$$

$$C_2 = mC_{ds} \quad (10)$$

where, ω_o is the center frequency and m is a multiplication factor which is used as a tool to control the slope of the Im[$Z_{SP,2fo}$], and so Im[$Z_{CCF,2fo}$]. Fig. 6(c) shows the variations of Im[$Z_{SP,2fo}$] for a range of $m = 0.8$ to $m = 1.2$ with a step of $m = 0.1$. Notice that, the values of L_d, L_2 and C_2 are derived from C_{ds}. Therefore, the harmonic-tuned load network can be realized very close to the intrinsic current generation plane (in Fig. 3). This significantly reduces mismatch concerns associated with impedance shift from the intrinsic current generation plane [23], [25].

A single-stage LC matching circuit after the series-parallel tuned network is considered to match the fundamental impedance while creating minimal influence on 2nd and 3nd harmonic load. Fig. 7(a) shows the simplified circuit diagram of the output load network including LC matching circuit for f_o band. The equivalent Z_{LC} can be derived as,

$$Z_{LC} = \frac{R_L}{1+R_L^2\omega^2 C_{mo}^2} + j\frac{\omega\left[L_{mo} - R_L^2 C_{mo} + \omega^2 C_{mo}^2 R_L^2 L_{mo}\right]}{1 + R_L^2\omega^2 C_{mo}^2}. \quad (11)$$

As shown in (7), the real part of the Z_{SP} is zero while it produces relatively small reactive component at f_o. Therefore, for the purpose of simplicity we can consider (2) and (11) are roughly equal at f_o. By equating real and imaginary parts of (2) and (11), closed-form equations for C_{mo} and L_{mo} are evaluated for f_o band as,

$$C_{mo} \approx \frac{1}{\omega R_L}\sqrt{\frac{\sqrt{3}R_L}{2R_{CCF}} - 1} \quad (12)$$

$$L_{mo} \approx \frac{R_{CCF}}{\gamma\,\omega} + \frac{2R_{CCF}}{\sqrt{3}\omega}\sqrt{\frac{\sqrt{3}R_L}{2R_{CCF}} - 1}. \quad (13)$$

The net Z_{CCF} in Fig. 7(a) can be determined by summing (7) and (11) as Z_{SP} and Z_{LC} are connected in series. In the final PA design, load-pull simulation is performed to

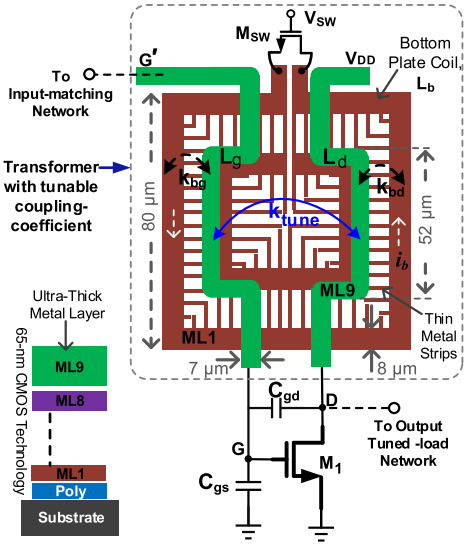


Fig. 8. Simplified circuit diagram of the tunable C_{gd} neutralization network using transformer feedback gate-drain neutralization with the layout details of the tunable transformer in 65-nm CMOS technology [32] [drawn not to scale].

determine Re[$Z_{CCF,fo}$]. This provides the value of R_{CCF} and using (12) and (13), the design value of L_{mo} and C_{mo} can be determined for a practical load value of $R_L = 50\Omega$.

Fig. 7(b) shows the normalized Im[Z_{CCF}] across normalized frequency. At f_o band, with the change in γ (positive to negative), Im[$Z_{CCF,fo}$] moves from inductive to capacitive load. In contrast, at $2f_o$ band, as γ changes (positive to negative), Im[$Z_{CCF,2fo}$] propagates from capacitive to inductive load. Therefore, the necessary phase conditions of reactive components in (2) and (3) to realize a CCF load network are achieved. On the other hand, the appropriate selection of L_{mo}, C_{mo}, m, and C_{ds} values play role to maintain the required ratios of real and reactive parts of $Z_{CCF,fo}$ and $Z_{CCF,2fo}$ in (2) and (3) (i.e., Im[$Z_{CCF,fo}$]/ Re[$Z_{CCF,fo}$] and Im[$Z_{CCF,2fo}$]/ Re[$Z_{CCF,fo}$]).

B. Tunable-Neutralization Network

A gate-drain transformer feedback neutralization technique is adopted using L_d and L_g as shown in Fig. 8. This transformer creates an additional path from output to input which has the same magnitude response, but opposite phase response compared to the existing feedback path [36]. Hence, the net result creates the neutralization of C_{gd} effect. Since L_d is already a part of the output load network, no extra area is required, while L_g can appropriately be modeled as part of an input matching network. To alleviate the modeling inaccuracies of C_{gd} at mmW frequencies, a transformer with a tunable coupling coefficient (k_{tune}) is adopted [36]. The prior work [36] is focused on frequency reconfigurable class-AB PA while this work is solely based on high-efficiency CCF PA. The integration of the tunable transformer in high-efficiency CCF PAs is not covered by prior state-of-the-arts. This transformer-based neutralization can significantly reduce the detrimental effect of C_{gd} on harmonic-tuned load thus facilitating minimal frequency shift of output resonance network. Further, the tunability in transformer can help to reduce the effect of any undesirable change in total C_{gd} due to inaccurate EM modeling or PVT variations by adjusting the value of k_{tune} during measurement. This tunability is realized through the tunable operation of L_d and L_g. The complete layout of the transformer in a 65-nm CMOS technology is shown in Fig. 8. An ultra-thick top metal layer (ML9) is used to design L_d and L_g for a higher quality factor, while the switched substrate-shield bottom plate coil is realized using a lower-most metal layer (ML1). To neutralize the effect of C_{gd} perfectly in a single-ended CMOS PA, the tunable coupling-coefficient can be written from small-signal model of circuit in Fig. 8 as [36],

$$k_{tune} = \frac{C_{gd}}{C_{gs} + C_{gd}} \sqrt{\frac{L_{d,os}}{L_{g,os}}} \tag{14}$$

where, subscript "os" is defined as various operating states of L_d and L_g with respect to control voltage, V_{SW}.

The switched substrate-shield layout technique is used to tune the inductance of L_g and L_d [37]. The induced magnetic current (i_b) flow created from L_d and L_g in bottom plate coil (L_b) is controlled by V_{SW}, which modifies the total magnetic flux in the system resulting a net change in L_d and L_g. Since ($L_{d,os}$, $L_{g,os}$) = $f(V_{SW})$ and k_{tune} = $f(L_{d,os}, L_{g,os})$, hence, k_{tune} = $f(V_{SW})$. Therefore, by controlling V_{SW} a range of coupling-coefficient can be generated from the transformer.

The operation of the transformer can be separated into two distinct modes depending on the states of the MOSFET switch connected in the bottom plate coil. When M_{SW} is tuned-on (i.e., V_{SW} = 1V), the bottom plate coil forms a closed loop through the switch, thus decreasing the equivalent inductance in L_d and L_g. As a result, a net increase in coupling coefficient is obtained. The coupling-coefficient during on-state is defined as,

$$k_{tune,on} = \frac{M_{tune,on}}{\sqrt{L_{d,on} L_{g,on}}} \tag{15}$$

where, $M_{tune,on}$ is the mutual inductance between L_d and L_g during on-state.

In contrast, during M_{SW} is turned-off (i.e., V_{SW} = 0V), the bottom plate coil is open, and the transformer acts akin to a conventional transformer with substrate-shielding. Therefore there is no change in $L_{d,off}$, $L_{g,off}$, and $k_{tune,off}$. Closed form design equations for the transformer are summarized from [36] in Table I for both on and off-state of M_{SW}. Here, k_{bg} and k_{bd} are the coupling-coefficient between (L_g, L_b) and (L_d, L_b) respectively. The M_{SW} is modeled as an equivalent resistance of $R_{sw,on}$ during on-state while off-state is modeled as an equivalent capacitance of $C_{sw,off}$. The loss elements of the L_g, L_d and L_b are modeled as r_g, r_d and r_b. In simulation, the values of $R_{sw,on}$, $C_{sw,off}$ and r_b are roughly 2.2Ω, 170fF and 0.6Ω respectively. The design methodology and equivalent circuits of the transformer in both on and off-states of M_{SW} can be found in [36].

However, the operation of transformer is not exclusively limited to these two modes (on and off). More accurately, it can be operated in a continuous way between completely on and off modes based on the V_{SW} of the control switch. As a result, a continuous set of coupling-coefficient values can be

TABLE I
DESIGN EQUATIONS OF THE TUNABLE-K TRANSFORMER

	M_{SW} = ON V_{SW} = 1 V	M_{SW} = OFF V_{SW} = 0 V
L_d	$L_d\left[1-\frac{k_{bd}^2}{1+\left(\frac{R_{sw,on}+r_b}{\omega L_b}\right)^2}\right]$	$\approx L_d$
L_g	$L_g\left[1-\frac{k_{bg}^2}{1+\left(\frac{R_{sw,on}+r_b}{\omega L_b}\right)^2}\right]$	$\approx L_g$
r_d	$r_d+\left(\frac{k_{bd}^2(R_{sw,on}+r_b)\left(\frac{L_d}{L_b}\right)}{1+\left(\frac{R_{sw,on}+r_b}{\omega L_b}\right)^2}\right)$	$\approx r_d$
r_g	$r_g+\left(\frac{k_{bg}^2(R_{sw,on}+r_b)\left(\frac{L_g}{L_b}\right)}{1+\left(\frac{R_{sw,on}+r_b}{\omega L_b}\right)^2}\right)$	$\approx r_g$
M_{tune}	$M_{tune}+\left(\frac{\lvert k_{bg}k_{bd}\rvert\sqrt{L_gL_d}}{1+\left(\frac{R_{sw,on}+r_b}{\omega L_b}\right)^2}\right)$	$\approx M_{tune}$

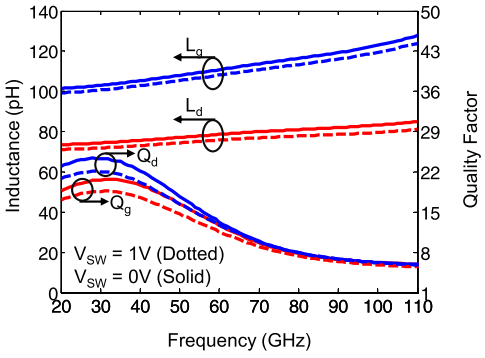


Fig. 9. EM simulation results of L_d, L_g, Q_d, Q_g across frequency for M_{SW} is turned-on and off.

obtained between the extremes of $k_{tune,on}$ and $k_{tune,off}$. This provides a great flexibility to designers, since a wide set of k_{tune} values can be selected based on specific performance requirements during on-chip PA measurements.

The EM simulation results of the transformer using ADS Momentum tool are depicted in Fig. 9 and 10. At 30 GHz, the off-state (V_{sw} = 0 V), $L_{d,off}$ = 76 pH, $L_{g,off}$ = 105 pH and $M_{tune,off}$ = 18.1pH produces $k_{tune,off}$ = 0.202 while at on-state (V_{sw} = 1 V), $L_{d,on}$ = 71 pH, $L_{g,on}$ = 100 pH

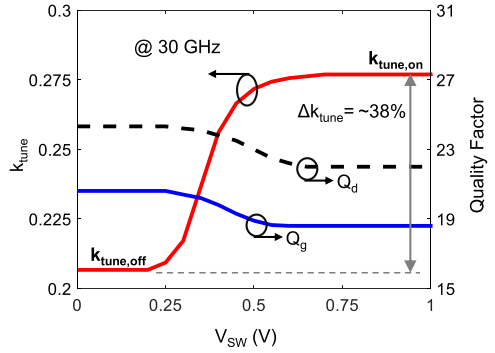


Fig. 10. EM simulation results of k_{tune}, Q_d and Q_g across V_{SW} at 30 GHz.

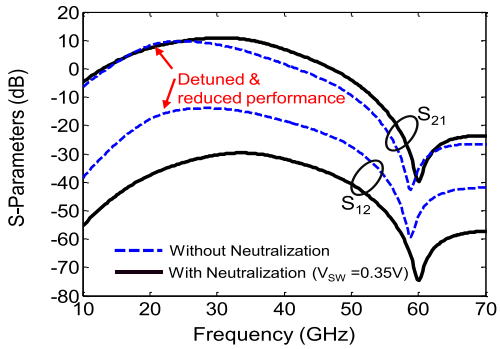


Fig. 11. Simulation results of S-parameter with and without neutralization.

and $M_{tune,on}$ = 23.6 produces $k_{tune,on}$ = 0.28. This provides a 38% change in the coupling-coefficient (Δk_{tune}) as shown in Fig. 10. To neutralize the effect of C_{gd} properly during measurement, the appropriate k_{tune} value can be selected from the above-mentioned range.

IV. IMPLEMENTATION OF CCF PA

A 65-nm CMOS technology is used to implement the proposed PA. Modeling of active devices, especially in a PA where the device size is typically large, plays a key role in ensuring overall achievable performance. To meet power requirements effectively, a large device is generally divided into several unit cells, and finger size is restricted to a certain width to minimize the parasitic gate capacitance and resistance. A device width of W_{tot} = 281.6 μm is selected for M_1 and divided into four power cell units to reduce parasitic capacitances while maximizing f_{max} [12]. Each cell unit consists of 32 fingers with a finger width of 2.2 μm each. A drain supply of V_{DD} = 1.1 V is used. To apply this proposed single-ended PA in mmW transceiver designs, the effects of the non-ideal AC ground need to be incorporated in the PA design. To make a solid AC ground, thick and wider stack of metals can be used. Further, the non-ideal AC ground effects need to be carefully characterized using 2.5D/3D EM simulation tools. In simulation, this device supports a 1-dB compression output power of greater than $P_{o,1dB}$ = 14 dBm, while providing a gain of more than 11 dB in the design frequency band (25-35 GHz). The unit cell's extrinsic interconnect parasitic components (resistances,

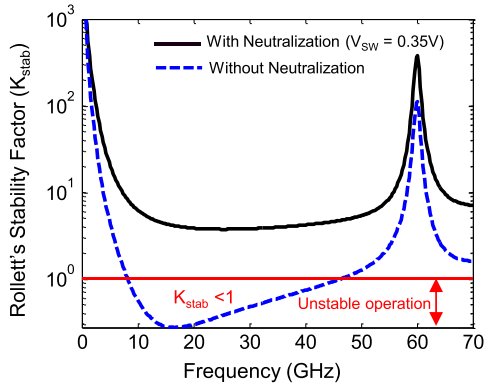


Fig. 12. Simulation results of Rollett's stability factor with and without neutralization.

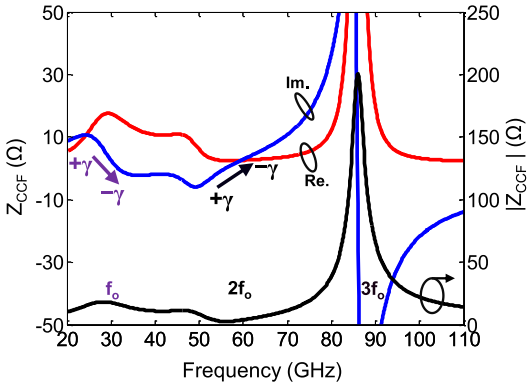


Fig. 13. EM simulation results of the complete output tuned load network of CCF PA (circuit in Fig. 5) [32].

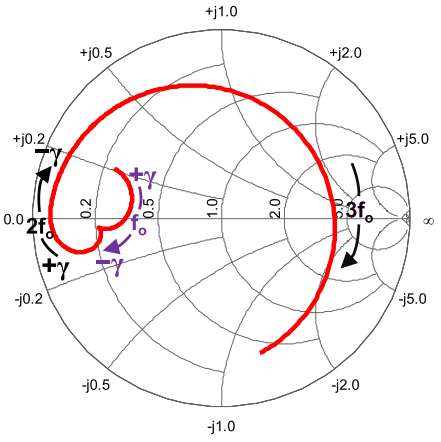


Fig. 14. Smith chart plot (normalized to 50Ω) of the EM simulation results of Z_{CCF} (circuit in Fig. 5).

capacitances, inductances) are also captured using the ADS Momentum EM simulation tool. The resulting model consists of extrinsic parasitic capacitances {C_{gs}, C_{gd}, C_{ds}, C_{gb}, C_{db}}; gate, drain and source terminal resistances {r_g, r_d, r_s}, and interconnect inductances in bottom metal layers of ML1, ML2, ML3 and ML4. Moreover, this EM simulation is extended to the input-output matching and source ground plane in UTM

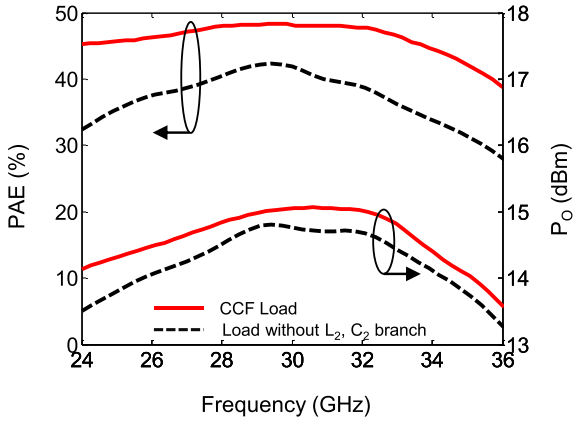


Fig. 15. Comparison of simulated PAE and P_o with a CCF load and a load without L_2 and C_2.

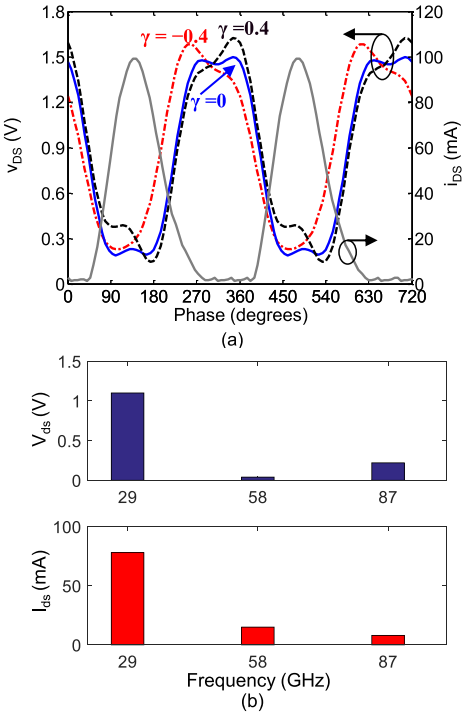


Fig. 16. Simulated (a) drain voltage (v_{DS}) and current (i_D) waveforms at node D (circuit in Fig. 5) for input power, Pin = 7 dBm [32] and (b) drain voltage and current harmonic contents at 29, 58 and 87GHz.

layer (ML9) to account for via parasitic. The simulated net parasitic capacitates are, C_{gs} = 230 fF, C_{gd} = 80 fF, and C_{ds} = 145 fF. This provides an initial value of k_{tune} = 0.22.

A fundamental real load of 14.9 Ω at 30 GHz is determined using load-pull simulation from 54.8% PAE and 14.9 dBm P_o contours [33]. Recently reported silicon PAs for 28 GHz 5G mobile communications present peak P_o of 14-15 dBm for each PA based on 8/16-element phased-arrays [7]–[9]. As a result, the design goal of P_o for this work is well-suited for 5G mobile communications. We also note that the output power level of the CCF PA can be further increased by adopting a differential configuration with the tunable neutralization transformer. This may also help to improve the PAE because

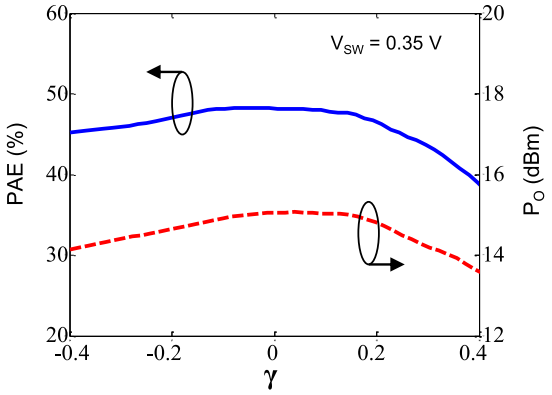


Fig. 17. Simulated PAE and P_o at input power, Pin = 7 dBm.

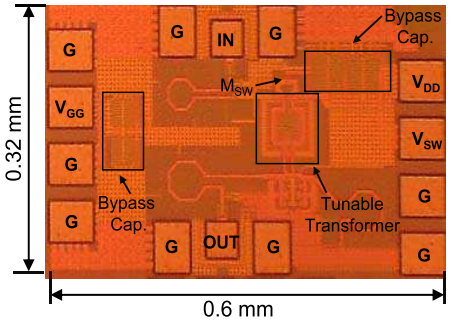


Fig. 18. Die microphotograph of the CCF PA in 65-nm CMOS.

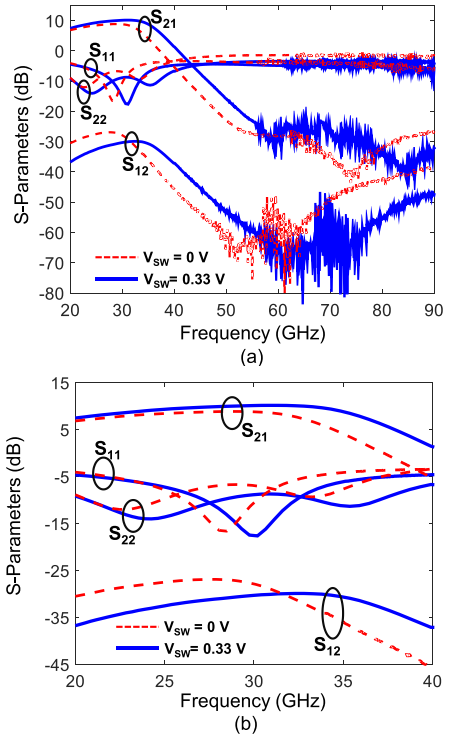


Fig. 19. Measured S-parameters for two different setting of V_{SW}, (a) 20-90GHz, (b) zoom-in plot for in band frequencies.

differential configuration supports higher harmonic tuned load-line thus producing reduced loss from load-line. Further to increase the gain a driver stage can be included.

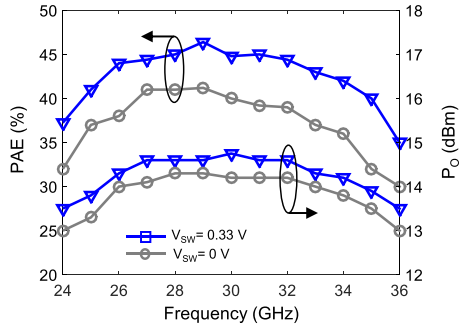


Fig. 20. Measured large-signal results across frequency [32].

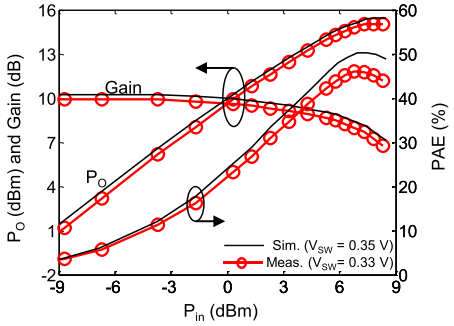


Fig. 21. Large-signal results across input power at 29 GHz [32].

The simulated total output load-line loss is ∼0.85dB at 30GHz and the major contribution of this loss comes from the output LC impedance transformation network which is ∼0.48dB. The mapping of $Z_{CCF,fo}$ and $Z_{CCF,2fo}$ for the design range of γ (−0.4 to 0.4) are calculated from (2) and (3), and the corresponding L_2, C_2, L_{mo} and C_{mo} are evaluated using (9)-(10) and (12)-(13). Fig. 11 and 12 show the simulation results of reverse isolation (S_{12}), forward gain (S_{21}) and Rollett's stability factor (K_{stab}) [38] with and without neutralization versus frequency. Without neutralization, S_{21} and S_{12} show detuned matching and reduced performance. In addition, K_{stab} is less than one (i.e., $K_{stab} < 1$) in the design range of the CCF PA (i.e., 25-35 GHz). Therefore, for this specific setup, the PA is unstable and cannot be practically used. On the other hand, with neutralization, the PA is unconditionally stable for all frequency while showing about 3 dB (maximum) improvement in S_{21} and about 10-15 dB improvement in S_{12} at 25-35 GHz. In the band of interest K_{stab} is about 4 with neutralization. Therefore, a robust operation with improved performance of CCF PA can be obtained using the proposed design technique.

The EM simulated frequency response of Z_{CCF} is depicted in Fig. 13 across 20-110 GHz. With the change of Im[$Z_{CCF,fo}$], the Im[$Z_{CCF,2fo}$] satisfies the required phase change condition as given by (2) and (3). The Smith-chart representation of the Z_{CCF} is also shown in Fig. 14, while specifying f_o, $2f_o$ and $3f_o$ bands. Fig. 15 shows the simulation results of PAE and P_o between a CCF harmonic tuned load and a non-harmonic tuned load. For the non-harmonic tuned load, we removed L_2 and C_2, and re-tuned the load-line. As shown in Fig. 15, the PAE of CCF with harmonic tuned

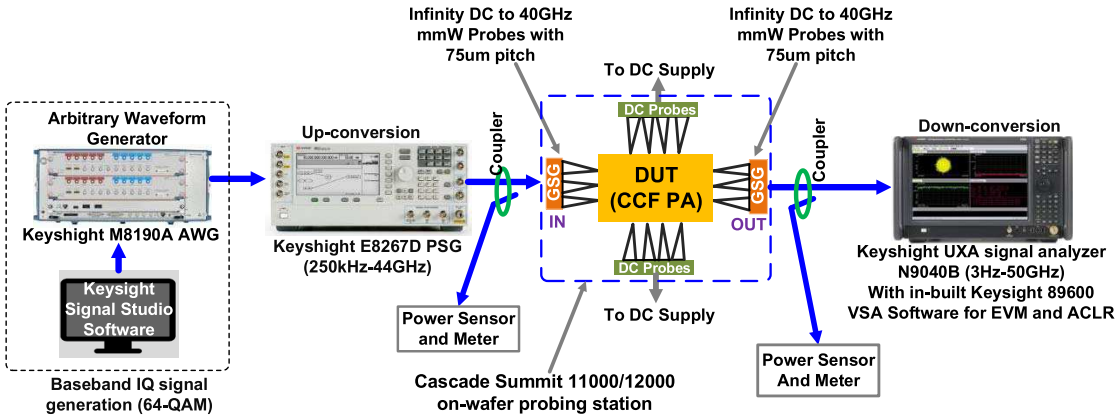


Fig. 22. Modulated-signal (64-QAM, 250 MHz of bandwidth, i.e., 1.5 Gb/s) measurement setup.

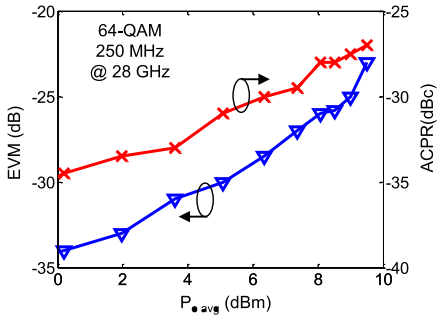


Fig. 23. Measured EVM and ACPR at 28 GHz across average output power for 64-QAM, 250 MHz BW signal.

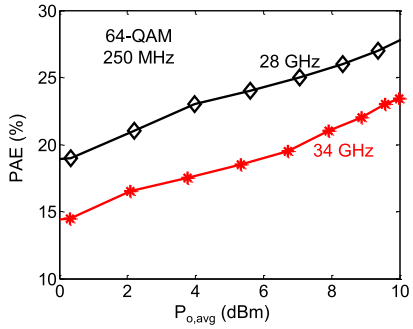


Fig. 24. Measured modulated PAE at 28 and 34 GHz across average output power for 64-QAM, 250 MHz BW (1.5 Gb/s) signal.

load is 6-10% higher across 24-36GHz compared to that of CCF with non-harmonic tuned load.

The drain voltage and current waveforms from post-layout simulation results are plotted in Fig. 16(a), where the voltage waveforms are shown for $\gamma = -0.4$, 0 and 0.4. Also, the simulated drain voltage and current harmonic contents at 29, 58 and 87GHz are shown in Fig. 16(b). Fig. 17 shows the simulation results of the PAE and P_o across γ (-0.4 to 0.4). These results are presented using $V_{SW} = 0.35$ V, the same condition used in Fig. 11 and 12 to shows the S-parameters and K_{stab} results. As it is seen that, PAE is high across γ, showing 39-47.8% of PAE while maintaining 13.8-15 dBm of P_o.

TABLE II
SUMMARY OF MEASUREMENT RESULTS FOR 64-QAM SIGNAL WITH 250 MHz OF CHANNEL BANDWIDTH (1.5Gb/s)

Parameters @ -25 dB EVM	f_c = 28 GHz	f_c = 32 GHz	f_c = 34 GHz
$P_{o,avg}$ (dBm)	9.2	8.8	8.6
Modulated PAE (%)	26	24	21.4
ACLR (dBc)	-27	-28	-27.8

V. EXPERIMENTAL RESULTS

The die microphotograph of the proposed CCF PA in a 65-nm CMOS is shown in Fig. 18, and the chip occupies an active area of 0.12 mm^2 only (total area with pads is 0.32 mm × 0.6 mm). A Cascade Summit 11000/12000 on-wafer probing station with Keysight PNA-X N5247A and E8257 are used to characterize the PA's small-signal. The measured S-parameters are shown in Fig. 19 for two different setups of V_{SW} (i.e., k_{tune}). Here, Fig. 19(a) depicts the measured S-parameter results up to 90 GHz while Fig. 19(b) represent the zoom-in results for in-band frequencies (20-40 GHz). In first setup ($V_{SW} = 0$V) the PA shows a downward frequency shift (i.e., about 6 GHz) in matchings while producing reduced S_{21} and S_{12}. While in second setup ($V_{SW} = 0.33$ V) the PA results an improved performance with near-flat S_{21} and better than -30 dB of S_{12} across 25-35 GHz. This later setup is used to characterize the PA's large-signal performances. Also, in the initial circuit (simulation) design V_{SW} was 0.35V for optimum performance which is slightly higher than the actual measurement setup.

Fig. 20 depicts the measured large-signal performances across 24-36 GHz. The measured PAEs and P_os are shown for both $V_{SW} = 0$ and 0.33 V. More than 40% measured PAE is achieved from 25-35 GHz while attaining 46.4% peak PAE at 29 GHz. On the contrary, the measured PAE for $V_{SW} = 0$ V shows about 5-8% degradation while delivering 0.4-0.6dB

TABLE III
PERFORMANCE COMPARISON WITH RECENTLY REPORTED STATE-OF-THE-ART MMW SILICON PAS

References		Tech. (nm)	Freq. (GHz)	PAE_{sat} (%)	>40% PAE_{sat} BW (GHz)	Gain (dB)	$P_{o,1dB}$ (dBm)	$P_{o,sat}$ (dBm)	V_{DD} (V)	Active Area (mm^2)	Architecture
This Work		**65**	**29**	**46.4**	**10 (25 −35GHz)**	**10**	**13.2**	**14.75**	**1.1**	**0.12**	**1-stage Continuous Class-F**
TMTT'14 [18]	CMOS	45 SOI	47	34.6	-	13	-	17.6	2.4	0.12	1-stage Class-E
RFIC'14 [19]	CMOS	45 SOI	18	43.7	-	12	11.3	15	1.8	0.62**	1-stage, Diff. 2-Stack, Class-E
JSSC'16 [9]	CMOS	28	30	35.5	-	15.7	13.2	14	1.0	0.16	2-Stage Differential
TMTT'16 [7]	CMOS	28	28	43.3	-	10	14	14.8	1.1	0.28	1-stage Differential
TMTT'18 [36]	CMOS	65	28	40.1	-	8.9	13.6	14.4	1.1	0.11	1-Stage Class-AB
RFIC'11 [40]	CMOS	65	19	25.6	-	22	-	23.8	2.4	0.96	2-Stage 1-Stack
MWCL'15 [43]	CMOS	65	23.5	19.3	-	10.2	23.9	26.1	2.4	0.64	1-Stage 1-Stack
RFIC'12 [15]	CMOS	45	42.5	34	-	9.5	-	18.5	2.7	0.3	1-Stage 2-Stack
RFIC'12 [20]	CMOS	32	60	30	-	10	-	12.5	0.9	0.61**	1-Stage Class-E
JSSC'13 [42]	CMOS	40	60	30.3	-	17	13.8	17	1.0	0.074	3-Stage Differential
RFIC'12 [41]	CMOS	65	24	29	-	-	-	18	1.2	0.91	2-Stage Differential
RFIC'17 [10]	CMOS	28	43	24.2	-	20.8	13.4	16.6	0.9	0.16	2-Stage Differential
MWCL'17 [45]	SiGe	55	66	12.5	-	23.8	20	23.4	3	0.17	2-stage Cascode Four-way
ISSCC'17 [46]	SiGe	55	80	23	-	21	18	19	2.3/1.8	0.24**	2-Stage Differential
JSSC'16 [21]	SiGe	130	24	50	4.5	21	16	18	2.3	0.6**	2-stage Class-F^{-1}
TMTT'17 [11]	SiGe	130	28	35.5	-	15.3	15.5	18.6	3.6	0.45**	1-stage Class-AB
JSSC'14 [39]	SiGe	130	41	36	-	21.2	-	18.1	2.4	0.49**	1-stage Class-E
BCTM'11 [44]	SiGe	120	45	30.8	-	7.8	-	14.75	2.4	0.27**	1-stage Class-B
CICC'15 [22]	SiGe	130	28	42	1.5	21.2	15	16.5	2.4	0.52	2-stage Class-F^{-1}
ISSCC'17 [13]	SiGe	130	28	20.3	-	18.2	15.2	16.8	1.5	1.76**	2-Stage Doherty
ISSCC'17 [13]	SiGe	130	37	22.6	-	17.1	15.5	17.1	1.5	1.76**	2-Stage Doherty

**Total area (including pads)

lower P_o. This is due to the non-optimal neutralization of C_{gd}. This also confirms the benefits of the accurate neutralization using the proposed tunable neutralization. In addition, output power (P_o) of >14 dBm from 25-35 GHz is measured. A saturated peak output power of 14.8 dBm is measured at 30 GHz. Fig. 21 depicts the measured and simulated PAE,

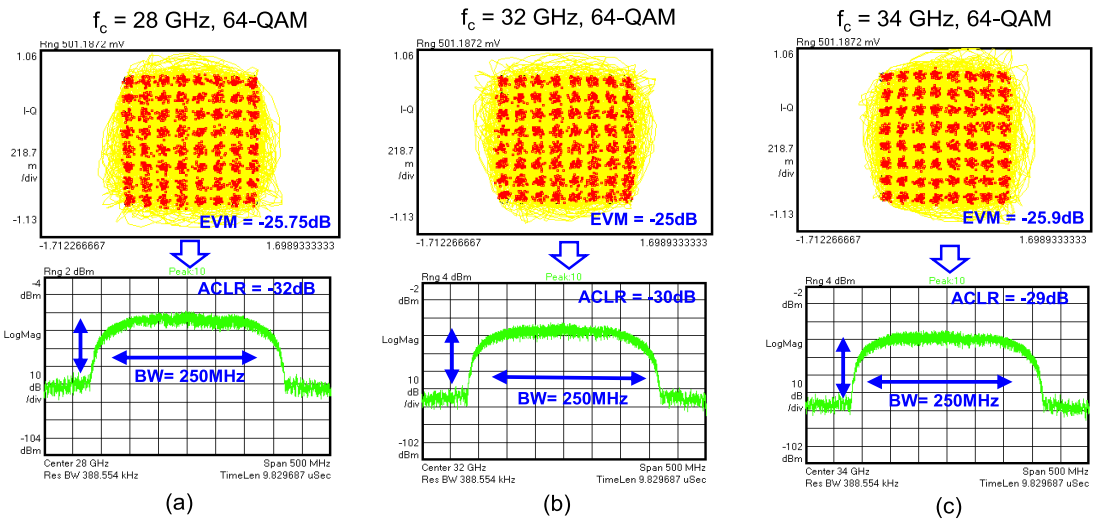


Fig. 25. Measured EVM and ACLR waveforms at center frequencies (f_c) of (a) 28, (b) 32 and (c) 34 GHz for 64-QAM, 250 MHz BW signals.

P_o and gain at 29 GHz to demonstrate its performances with input power (P_{in}).

To evaluate the large-signal performances of the PA with modulated signal, the prototype is tested under 64-QAM, 250 MHz (i.e., data-rate of 1.5Gb/s) signal at 28, 32 and 34 GHz. The measurement setup is shown in Fig. 22. The baseband modulated signal is generated using Keyshight M8190A arbitrary waveform generator (AWG) and Keysight Signal Studio software while the baseband signal is up-converted with the help of Keysight E8267D PSG vector signal generator. The amplified modulated signals are demodulated using Keysight UXA N9040B signal analyzer and Keysight 89600 vector signal analyzer (VSA) software. Fig. 23 shows the measured error-vector-magnitude (EVM) and adjacent channel leakage ratio (ACLR) results at 28 GHz across average output power ($P_{o,avg}$). Further, the PAE results are shown in Fig. 24 at 28 and 34 GHz for a 64-QAM with 250 MHz of BW. At 28 GHz, the PA shows about 26% PAE with 9.2 dBm of $P_{o,avg}$. This result corresponds to -25 dB of EVM and -27 dBc of ACLR.

The measured waveforms of EVM and ACLR at 28, 32 and 34 GHz are shown in Fig. 25. All the waveforms are captured for 64-QAM signal with 250 MHz of BW. The measured large-signal results for modulated-signal at 28, 32 and 34 GHz are summarized in Table II.

The performance comparison with state-of-the-art tuned mmW PAs in silicon technologies is summarized in Table III. The reported PA shows highest reported PAE of 46.4% among CMOS technology at 29 GHz to date. Also, this is the first demonstration of $>40\%$ PAE over a bandwidth of at least 10 GHz among mmW CMOS and SiGe PAs. To fairly evaluate the area effetiveness in comparison to differenial stucture with cross-copupled neutralization, we compare the proposed single stage power amplifier with [7] that has the same operation frequency and $P_{o,sat}$. Since the transformer with small inductance value is compact while reused for RF choke and input matching network, the CCF PA can demonstrate a small active area of 0.12 mm^2, resulting a 2.3X smaller than the active area of [7]. As the same time, the PA can deliver $>3\%$ peak PAE at center frequency. Further, this design is capable to deliver $>40\%$ PAE_{sat} over 10GHz of BW due to the CCF harmonic-tuned load.

VI. Conclusion

This paper presents an integrated high-efficiency continuous class-F (CCF) CMOS PA at mmW frequencies for 5G mobile communications. We identified the practical design challenges associated with mmW CCF PA and demonstrated respective solutions. A harmonic-tuned load with a tunable C_{gd} neutralization network using a transformer is adopted. The harmonic-tuned network creates a favorable impedance characteristic to support the required loads at f_o, $2f_o$, and $3f_o$, while the transformer with a tunable coupling-coefficient desentisizes the influence of C_{gd} on output tuned-load network. These techniques lead to a PAE of 40-46.4% across 25-35 GHz, which is one of the highest reported PAEs in the integrated CMOS and SiGe PAs. Moreover, we presented measurement results using 64-QAM signal with 1.5Gb/s data-rate at 28, 32 and 34 GHz, achieving excellent large-signal performance while meeting good EVMs and ACLRs. This is possible due to the near-flat high-efficiency nature of the CCF PA leveraged by our proposed neutralized tuned-load network over several GHz of BW. The proposed CCF PA in CMOS technology presents an attractive solution for low-cost area-constrained mmW high-speed 5G mobile communications.

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