Analysis of Systematic Losses in Hybrid Envelope Tracking Modulators

Luke Renaud, *Student Member, IEEE*, Joseph Baylon, Srinivasan Gopal, *Student Member, IEEE*, Md Aminul Hoque, and Deukhyoun Heo, *Senior Member, IEEE*

***Abstract*— This paper presents a comprehensive analysis of the intrinsic losses in hybrid envelope tracking power supply modulators used in envelope tracking power amplifier systems. The losses are computed entirely symbolically in terms of system parameters and a single design parameter. Resulting formulations are used to provide design insight into optimum biasing to minimize losses in a hybrid configuration, and establish the theoretical upper bound of achievable efficiency. To illustrate the value of this analysis, a Rayleigh distributed waveform is used to evaluate the performance of the hybrid modulator to describe OFDM and other complex modulation schemes. This paper demonstrates that the common convention of biasing the linear converter's output stage to have zero average current is generally suboptimal from a loss perspective, and establishes how efficiency can be improved without modifying the underlying circuit topology. These findings are validated with a series of simulations modeling a hybrid modulator implemented in a 180-nm CMOS process. This paper derives for the first time, the intrinsic theoretical losses in the hybrid envelope modulator configuration.**

***Index Terms*— Circuit optimization, digital modulation, OFDM, power conversion, probability distribution.**

I. Introduction

FUTURE, high data-rate, wireless systems will require the widespread implementation of high complexity communication signals. Current generation cellular and consumer wireless standards (such as the 802.11 family) already rely heavily upon the use of OFDM and variant OFDM waveforms to enable high data rate communication. The coming wireless standards for 802.11ax and proposed 5G standards do not depart from these complex waveforms. While these standards support high data rate communication, they pose a problem of key interest to mobile wireless nodes (i.e. user handsets, laptops, etc.) in that they exhibit a high Peak-to-Average Power Ratio (PAPR). High PAPR waveforms tend to cause poor power efficiency in transmitter systems as the highest power elements in the transmit amplifier chain operate in back-off most of the time where they exhibit dramatically reduced efficiency.

One possible solution that has been explored to improve the efficiency of a power amplifier (PA) is the use of envelope tracking (ET). In envelope tracking, a dynamic power supply (DPS) is designed to provide a time varying supply voltage to a load PA. The DPS converts a fixed supply to this varying voltage based upon the transmission signal's envelope waveform with sufficient headroom to ensure proper PA operation. Provided the dynamic supply voltage is not set particularly low, the PA may be modeled as an equivalent load resistance [1]. The lower output voltage limit is dictated by requirements for the PA in ensuring linear operation and modeling as a resistive load. The dynamic reduction in supply voltage allows for loss reductions brought about proportional to the difference of the squares of the fixed supply and envelope voltage.

While a theoretically perfect DPS could eliminate all loss associated with supply voltage overhead, real supplies do not converge upon this ideal. In this work we claim further that for more common envelope tracking DPS architectures, not only is the real implementation unable to reach perfect efficiency, but the architectural structure produces an intrinsic loss term that even in an otherwise lossless system will always be present. Using this insight, loss associated with this behavior is derived for both a sine wave and a generalized Rayleigh distributed waveform, and the upper bound of a otherwise lossless supply modulator is derived. To enable designers to rapidly evaluate systems, we formulate this derivation in terms of normalized waveforms and show how the single designer controlled parameter in this system may be optimized to minimize intrinsic losses. We further demonstrate how known loss terms may be incorporated into this formulation to optimize full systems.

The paper is organized as follows. An overview of the existing designs and design understanding, and the basic mathematics required to describe the efficiency of a hybrid regulator is outlined in Section II. The analytical description of losses unique to the hybrid regulator and their relation to both a sinusoidal and to Rayleigh distributed waveforms are described in Section III. More involved mathematics for this analysis is presented in Appendix A and Appendix B. An example system evaluation including the conduction losses

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The authors are with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99164 USA (e-mail: lrenaud@wsu.edu; joseph_baylon@wsu.edu; srinivasan.gopal@wsu.edu; mdaminul.hoque@wsu.edu; dheo@eecs.wsu.edu).

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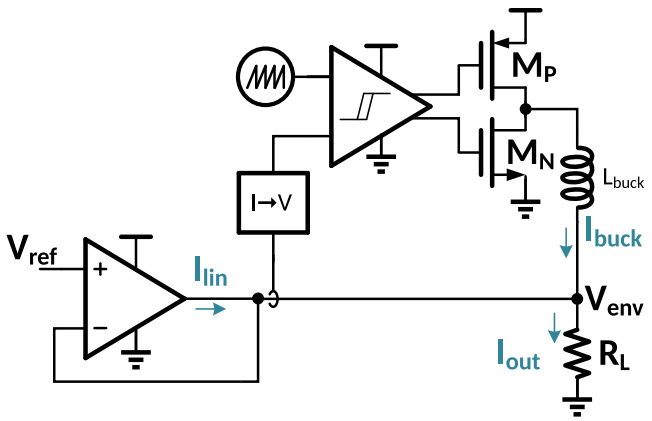

Fig. 1. Schematic of an typical hybrid regulator.

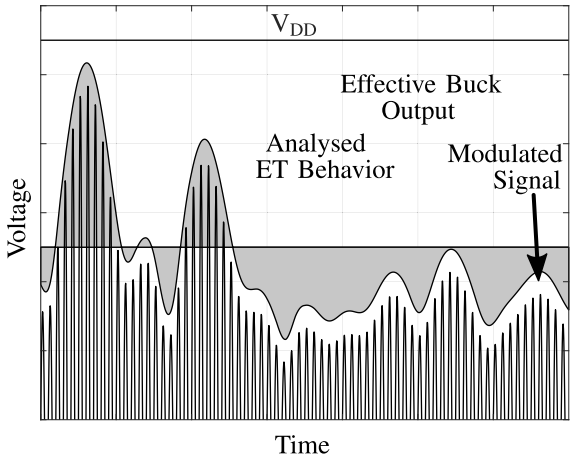

Fig. 2. Losses intrinsic to a hybrid ET system. The shaded region shows the deviation in supply produced by the actions of the linear output stage from the comparatively slow buck converter output. Scale exaggerated for visual clarity.

in a typical buck converter is performed in subsection III-C. The theoretical equations are evaluated to gain insight into their character in section IV, along with the results of a series of circuit simulations used to validate the loss mechanism described is presented in subsection IV-D. Finally, Section V concludes the paper.

II. System Description

In a conventional "hysteretic" hybrid envelope modulator, two parallel power converters are used to convert a fixed input supply voltage to a time-varying output waveform, acting as a PA supply voltage. In such architectures, a switching buck converter is placed in parallel with a low- or unity-gain linear regulator such as in Fig. 1 ([2]–[7]). The inherent trade-off of this strategy is replacing amplitude dependent losses from the supply rail to the envelope signal, with new losses associated with sinking and sourcing supplementary current around an operating point visually identified in Fig. 2. The losses in the hybrid system should, by conceptual arguments [3], be smaller than those of a fixed supply system. Existing works however, do not formalize this argument. The buck converter is usually controlled by using a sensing block to drive the system into a control state as such to minimize the average power delivered by the linear regulator (I_{lin}). Waveform precision is ensured by the very presence of a high-bandwidth linear output stage. To improve efficiency relative to that of an isolated linear stage, designs attempt to maximize power provided by the comparatively high efficiency switching stage. The natural low-pass response of the buck converter [8], tends to drive the buck converter's output current towards the mean of the waveform being produced. Results to date have shown system efficiencies upwards of 80% for some waveforms [9], but neglect to describe or consider the optimal control case for efficiency in their designs [4], [5], [10]. Frequency based arguments considering the low-pass response of the buck converter versus the broadband response of the linear stage were used as motivation in [11]. While such arguments aid in developing an intuitive understanding of design objectives, they leave questions of performance limitations and optimal design unanswered. This paper performs a detailed analysis of losses specific to the hybrid architectural approach, to aid in understanding how the two regulators behave jointly to achieve high efficiency.

Existing works such as [3] and [11] neglect to describe the expected losses of their system. Even in works that attempt to consider losses, as in [10], predictions are not developed analytically. As the published linear stages make use of highly sensitive output stages (such as the super-source-follower stages used in [3] and [11]), chip-to-chip performance can vary dramatically prior to tuning, increasing the value of understanding if a design result has been optimized appropriately.

The comparison problem becomes more convolved when comparing standard ET designs to reduced bandwidth envelope ET systems [12] or discrete multi-level converters [13], where the apparent efficiency appears higher than comparable ET designs. While these modified topologies exhibit improved *DPS* efficiency, the failure to track the envelope waveform simply moves power losses that would otherwise exist in the supply to the load PA. The associated losses described in this paper will thus still be present in such systems, but the losses will be attributed to the PA rather than to the DPS stage. Reduced bandwidth envelope tracking systems will directly offload losses analyzed here to the underlying PA, while multi-level converters will partially remove and partially offload this loss burden.

A. Loss Mechanism

The loss mechanisms in a buck converter include (but are not limited to): inductor conduction losses (instantaneous buck current into the inductor series resistance, $I_{buck}^2 R_{esr}$), voltage drop on switching devices at the switching output node (two terms for sinking and sourcing current times into the respective device voltage drops and load currents, $D \times (V_{drop,up} I_{buck}) + (1 - D) \times V_{drop,dn} I_{buck}$), and controller losses. These mechanisms remain unchanged in a hybrid regulator. Loss mechanisms in the linear stage are designed to be dominated by the voltage drop of the output device ($V_{drop} I_{lin}$, where the voltage drop depends upon the sign of I_{lin}), but DC biasing circuitry will also introduce some static loss. It should

be noted that the losses described thus far are broadly analyzed in existing texts such as [8], and are highly dependent upon implementation and system specifications.

Interestingly, in the hybrid envelope modulator architecture the linear loss term is modulated by the combined behavior of the system in an output dependent manner. It is noted that the output current delivered into a resistive load couples the buck and linear stage's output currents, as well as the output voltage. As the load is resistive in character, any desired change in the output voltage from nominal requires the linear stage to supply or sink the extra or surplus current provided by the buck converter. Thus the voltage at the load (i.e. voltage envelope) is dictated by the sum of currents at the output node, the output voltage is related directly to the output currents as (1).

$$V_{out} = V_{env}(t) = R_L I_{out}(t) = R_L(I_{buck} + I_{lin}) \tag{1}$$

The action of the linear stage to control the output gives rise to a loss term dependent upon I_{buck}, described in relation to the instantaneous current demand, I_{out}. Given the voltage and current descriptions of the desired output envelope in (1), the loss terms are described in equation (2), where I_{out} is the output current of the tracked envelope voltage waveform into a resistive load.

$$P_{lin,loss} = \begin{cases} (V_{DD} - V_{env})|I_{lin}|, & \text{if } I_{out} > I_{buck} \\ V_{env}|I_{lin}|, & \text{if } I_{out} < I_{buck} \end{cases} \tag{2}$$

III. Efficiency Analysis

The general system efficiency of a hybrid envelope modulator is given as equation (3). This expression represents the useful power delivered to the load, and combined losses associated with the buck converter and linear output stage.

$$\eta_{sys} = \frac{P_{load}}{P_{bk,loss} + P_{lin,loss} + P_{load}} \tag{3}$$

The losses of control overhead, and buck switching losses as a sub-element of $P_{bk,loss}$ do not change in hybrid switching regulator architecture. The key term that varies in a hybrid architecture is the linear stage's loss term, $P_{lin,loss}$. As the remaining terms are independent of fundamental ET operation, these loss terms should be minimized independently of the design of the linear stage's loss and are readily incorporated in specific designs by using (3) as necessary. The challenge addressed in this work to understand how various envelope waveforms and specific control restrictions will contribute to loss and thus limit peak efficiency.

For the purposes of this first analysis we will evaluate the performance of an otherwise lossless converter. The buck converter is assumed to have perfect conversion efficiency, and the controller overhead will be neglected. These terms vary wildly based upon implementation specifics. Regardless of design specifics, any associated losses are easily incorporated for individual designs by using (3) without requiring alterations in the following loss analysis. An example incorporating losses from a buck converter is later outlined in subsection III-C. This analysis further relies upon the assumption of a comparatively quickly varying envelope waveform to the natural low-pass response of the buck converter [8]. As signal bandwidths grow even wider than the common 20MHz LTE envelopes in use today, this approximation becomes stronger.

A. Sinusoidal Performance

To demonstrate the analysis consider an envelope signal of an offset sinusoid applied to the system shown earlier in Fig. 1. An average output current will be reached by the buck converter as set by the designer, and deviations from this nominal average (i.e. time varying signal components) will be supplied by the linear stage. Given a sinusoidal amplitude V_0 and DC voltage V_{DC}, the equivalent output voltages and currents into the load resistance are described in equations (4) and (5).

$$V_{env}(t) = V_{DC} + V_0 sin(\omega t) \tag{4}$$

$$I_{env}(t) = \frac{V_{env}(t)}{R_L} \tag{5}$$

Note that in this particular envelope waveform, the DC offset voltage in the waveform should not be confused with the knee voltage used to maintain minimum headroom in the PA. The lowest output voltage of the waveform is given in equation (6).

$$V_{env,min} = V_{DC} - V_0 \tag{6}$$

Normalization of these waveforms will ease analysis and generalization across implementation technologies. Current and voltage waveforms are re-expressed in terms of scaled parameters relative to the amplitude of the output envelope voltage (V_0) and the load resistance (R_L) as in (7) and (8). The difference between nominal buck current (I_{buck}) and the average envelope current is expressed as an offset voltage (V_{offset}) in (9). This is the voltage that would be observed if I_{buck} was applied to the load resistance in isolation. In this sense the offset is a pseudo-voltage, as designers do not directly control it but rather control the nominal buck current through specifics of their buck converter implementation. In implementation, one trivial way to perform this biasing is to inject a bias current into the current-to-voltage conversion block shown in Fig. 1. The other parameters introduced (V_{DC}, V_0, R_L, etc.) are set by the requirements of the load and fixed supply, and thus are not generally under a circuit designer's control. Normalizing in this manner ensures all terms in the analysis exist in the voltage domain.

$$V_{env}(t) = V_0(v_{dc} + sin(\omega t)) \tag{7}$$

$$I_{env}(t) = \frac{V_0}{R_L}(v_{dc} + sin(\omega t)) = I_{lin}(t) + I_{buck} \tag{8}$$

$$V_{offset} = I_{buck} R_L - V_{DC} \tag{9}$$

For visual clarity, the various voltage terms used in this formulation are shown in Fig. 3. The left hand axis shows an example set of system voltages, while the right shows the equivalent normalized axis. This plot shows how a system designer's particular system voltages translate to normalized voltages. Normalized terms are explicitly outlined in (10a-d).

$$v_{dc} = \frac{V_{DC}}{V_0} \tag{10a}$$

$$v_{dd} = \frac{V_{DD}}{V_0} \tag{10b}$$

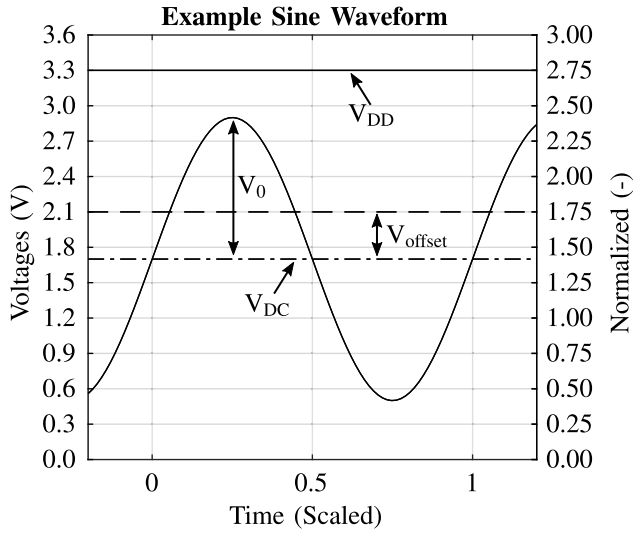

Fig. 3. A representative sine envelope and equivalent amplitude/time normalization. An example set of possible non-normalized voltages are shown on the left axis.

$$v_{off.} = \frac{V_{offset}}{V_0} \tag{10c}$$

$$v_{env}(t) = v_{dc} + sin(\omega t) \tag{10d}$$

Using these conversions, the linear stage's output current is re-expressed from (8) in terms of fixed system parameters given by the envelope waveform, and a single designer controlled parameter describing the control of the buck converter.

$$\begin{aligned} I_{lin}(t) &= \frac{V_{DC} + V_0 sin(\omega t)}{R_L} - I_{buck} \\ &= V_0 \frac{v_{dc}}{R_L} + V_0 \frac{sin(\omega t)}{R_L} - \frac{R_L}{R_L} I_{buck} \\ &= \frac{V_0}{R_L} sin(\omega t) - \frac{1}{R_L}\Big(I_{buck} R_L - V_{DC}\Big) \\ &= \frac{V_0}{R_L} sin(\omega t) - \frac{1}{R_L}\Big(V_{offset}\Big) \\ I_{lin}(t) &= \frac{V_0}{R_L}\Big(sin(\omega t) - v_{off.}\Big) \end{aligned} \tag{11}$$

Using the normalized current and voltage waveforms, the power loss is also re-expressed as (12). Finally, the cycle-average power consumption is then computed by integrating over a single period of the sine wave, and dividing by the period. This yields the total power loss as (13). Details of this formulation are outlined in Appendix A.

$$P_{lin,loss} = \frac{V_0^2}{R_L} \begin{cases} [v_{dd} - v_{dc} - sin(\omega t)] \\ \times (sin(\omega t) - v_{off.}), & \text{if } I_{out} > I_{buck} \\ -[v_{dc} + sin(\omega t)] \\ \times [sin(\omega t) - v_{off.}], & \text{if } I_{out} < I_{buck} \end{cases} \tag{12}$$

$$\begin{aligned} P_{lin,avg,loss} = \frac{V_0^2}{R_L}\Bigg[\frac{v_{dd}}{\pi}\Big(\sqrt{1 - v_{off.}^2} \\ - v_{off.} cos^{-1}(v_{off.})\Big) + \Big(v_{off.} v_{dc} - \frac{1}{2}\Big)\Bigg] \end{aligned} \tag{13}$$

With the knowledge that most of the parameters shown are not within a designers arbitrary control and are dictated by requirements of the envelope tracking system, we seek to optimize the single parameter under designer control, $v_{off.}$. Differentiating with respect to the offset voltage and finding the minima leads to a loss-minimizing normalized offset voltage given by (15), or equivalent buck current given by (16).

$$\frac{\partial P_{lin,avg}}{\partial v_{off.}} = \frac{V_0^2}{R_L}\Bigg[-\frac{v_{dd}}{\pi} cos^{-1}(v_{off.}) + v_{dc} \Bigg] \tag{14}$$

$$v_{off,opt} = cos(\pi \frac{v_{dc}}{v_{dd}}) \tag{15}$$

$$I_{buck,opt} = \frac{V_{DC} + V_0 cos(\pi \frac{V_{DC}}{V_{DD}})}{R_L} \tag{16}$$

Under conventional design wisdom the desired offset voltage should be zero, putting the nominal buck current in the middle of the sinusoid (i.e. at it's mean). *This analysis shows that a 0V offset will only be optimal for specific combinations of envelope offsets and supply voltages.* Specifically, as the supply voltage must be large enough to support the envelope ($V_{DD} \geq V_0 + V_{DC}$) the normalized ratio in (15) requires $v_{dd} \geq 1 + v_{dc}$. If we desire an optimum offset of zero, (16) requires $v_{dd} = 2v_{dc}$. *This indicates designing the buck converter to operate at a sinusoidal envelope's mid-point is only optimum when designs operate with equal headroom and legroom.*

B. Rayleigh Distributions

While a sinusoidal waveform is illustrative of the concept, we seek to understand if similar biasing can bring improvements to far more complex waveforms often used with envelope tracking systems. OFDM is by far the most common waveform, being used in both cellular and 802.11 standards, and exhibits a Rayleigh amplitude distribution. A similar analysis is be performed to determine the optimal reduction of this loss term by considering the expected value of the loss.

Normalization is again used to bring all terms into the same domain rather than mixing current and voltage expressions. The full amplitude range of the envelope signal (V_{FR}) will be used as a scaling term in place of the amplitude as in the sinusoidal example in section III-A. A random variable a is used to describe a Rayleigh distributed waveform, where the distribution parameter (σ_a) is assumed such that the energy beyond 1 is negligibly small. The envelope is thus described using the following terms:

$$V_{FR} = V_{MAX} - V_{MIN} \tag{17}$$

$$v_{max} = \frac{V_{MAX}}{V_{FR}} \tag{18a}$$

$$v_{min} = \frac{V_{MIN}}{V_{FR}} \tag{18b}$$

$$V_{ENV}(t) = V_{FR} \times a + V_{MIN} \tag{19a}$$

$$v_{env}(t) = \frac{V_{ENV}(t)}{V_{FR}} = a + v_{min} \tag{19b}$$

To ease evaluation, a fixed term in the same domain as a, representing the switching converter's output current a_{bk} is introduced in (20) and (21). This behaves similar to the

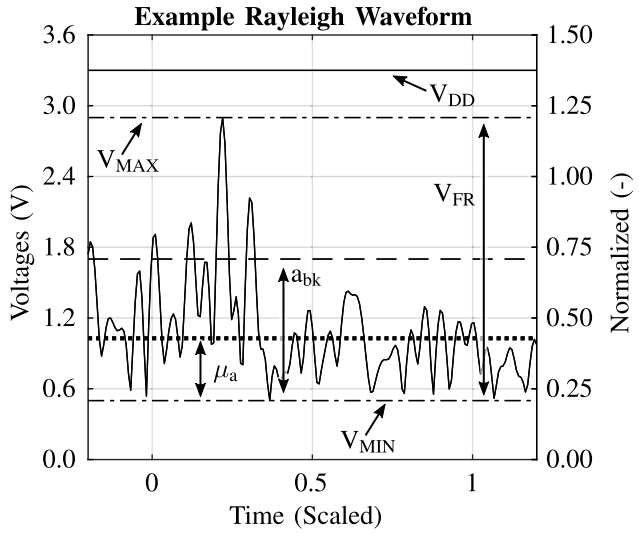

Fig. 4. Representative Rayleigh envelope and associated variables. μ_a is the envelope mean, while a_{bk} represents the effective normalized current, I_{buck}.

V_{offset} term in the sine wave, in that *it describes the buck converter's nominal output current in terms of a normalized pseudo-voltage*. Fig. 4 shows visually how all of the introduced terms relate to a representative waveform. This figure is further annotated with the mean voltage of the waveform.

$$I_{buck} = \frac{a_{bk} \times V_{FR} + V_{MIN}}{R_L} \tag{20}$$

$$a_{bk} = \frac{R_L}{V_{FR}} I_{buck} - v_{min} \tag{21}$$

Rather than performing the integral across a data dependent signal, we can use the expected value operator to compute the expected loss given a fixed buck current as in (22). Using the same scaling method employed for the sine wave, $P_{lin,loss}$ as a function of the random variable is explicitly defined based upon the original definition in (2) and the scaled envelope waveforms to become (23). By expanding terms appropriately the full expected value integral is described as (24).

$$E[P_{lin,loss}] = \int_0^\infty p_a(a) P_{lin,loss}(a) da \tag{22}$$

$$P_{lin,loss}(a) = \frac{V_{FR}^2}{R_L} \begin{cases} [v_{dd} - v_{env}] \\ \quad \times (a - a_{bk}), & \text{if } a > a_{bk} \\ [-v_{env}] \\ \quad \times (a - a_{bk}), & \text{if } a < a_{bk} \end{cases} \tag{23}$$

$$\begin{aligned} E[P_{lin,loss}] = \frac{V_{FR}^2}{R_L} \int_0^\infty p_a(a) \Big[& v_{min} a_{bk} \\ & + a(a_{bk} - v_{min}) - a^2 \Big] da \\ & + \frac{V_{FR}^2}{R_L} \int_{a_{bk}}^\infty p_a(a) \Big[v_{dd}(a - a_{bk}) \Big] da \end{aligned} \tag{24}$$

The computation of this integral pair is readily performed by noting many terms in the first integral are simply scaled terms of the first or second raw moments of the distribution. The second integral's terms are readily computed via scaling, and use of integration tables. Details of this process are outlined in Appendix B. This integral technically includes energy beyond the true amplitude distribution of an envelope waveform, but the energy contained beyond unit amplitude (representing the full waveform range as defined in (17)) is less than 1% if the distribution parameter is less than 0.33.[1] The result of this integral noting this approximation step is given in (25).

$$\begin{aligned} E[P_{lin,loss}] \approx \frac{V_{FR}^2}{R_L} \Bigg[& \mu_a (a_{bk} - v_{min}) + v_{min} a_{bk} \\ & - \frac{4}{\pi} \mu_a^2 + v_{dd} \mu_a erfc\left(\sqrt{\frac{\pi}{4}} \frac{a_{bk}}{\mu_a} \right) \Bigg] \end{aligned} \tag{25}$$

Once again, differentiating relative to the designer controlled parameter (a_{bk}) allows an efficiency optimum to be found. The optimum placement for the buck converter's output current is re-expressed in (27) as a fraction of either the mean of the waveform (μ_a) or the mode (σ_a).

$$\frac{\partial E[P_{lin,loss}]}{\partial a_{bk}} \approx \frac{V_{FR}^2}{R_L} \left[\mu_a + v_{min} - v_{dd} e^{-\frac{\pi}{4}\left(\frac{a_{bk}}{\mu_a}\right)^2} \right] \tag{26}$$

$$\begin{aligned} a_{bk,opt} &= \mu_a \sqrt{\frac{4}{\pi} \ln\left(\frac{v_{dd}}{\mu_a + v_{min}} \right)} \\ &= \sigma_a \sqrt{2 \ln\left(\frac{v_{dd}}{\mu_a + v_{min}} \right)} \end{aligned} \tag{27}$$

In the case of the Rayleigh distributed envelope, observe the optimum is only equal to one of the averages (either mean or mode) if the ratio of the mean, knee voltage, and supply voltage match a very specific ratio. 2.19 ($e^{\pi/4}$) for the mean, or 1.65 ($e^{1/2}$) for the mode.

C. Full System Considerations

To illustrate how we can utilize equations (13) and (25) in a full system evaluation, we can jointly consider the minimization of linear stage systematic losses with the anticipated conduction losses through the switching devices in a buck converter. Assuming ripple in the buck converter's output current is small compared to the steady state output, losses in the switching devices are described by (28) [14], where $R_{on,p}$ and $R_{on,n}$ describe the effective on-state resistances of the high-side (PMOS) and low-side (NMOS) devices respectively. These losses arise due to the finite voltage drop across the switching devices M_P and M_N in Fig. 1.

$$P_{bk,loss} = I_{buck}^2 \times \left(\frac{V_{DC}}{V_{DD}} (R_{on,n} - R_{on,p}) + R_{on,p} \right) \tag{28}$$

Note the new only terms in (28) relative to the analysis performed in Section III are the on-state resistance terms. To optimize the envelope tracking system, this loss is combined with the de-normalized loss described in (13) or (25), and substituted into (3) to describe the system efficiency. As this work principally seeks to describe how the linear stage's nominal current (and offset pseudo-voltage) relates to

[1] By using the cumulative density function, and evaluating energy from 1 to ∞, truncation error is computed as: $\%_{err} = exp(-\frac{1}{2}\sigma_a^{-2})$, $\%_{err} < 0.01 \rightarrow \sigma < 0.3295$. $\%_{err} < 0.001$ (0.1%) $\rightarrow \sigma < 0.269$.

efficiency, differentiation of the sum of the loss terms (i.e. $P_{lin,loss} + P_{bk,loss}$) is used to find a loss minimum and thus efficiency maximum in (29) and (30) for the sine wave and Rayleigh distributed envelopes respectively.

$$\begin{aligned}\frac{\partial P_{loss,sin}}{\partial I_{buck}} &= \frac{\partial P_{bk,loss}}{\partial I_{buck}} + \frac{\partial P_{lin,loss}}{\partial v_{off}} \times \frac{\partial v_{off}}{\partial I_{buck}} \\ &= \frac{\partial P_{bk,loss}}{\partial I_{buck}} + \frac{\partial P_{lin,loss}}{\partial v_{off}} \times \frac{R_L}{V_0} \end{aligned} \tag{29}$$

$$\begin{aligned}\frac{\partial P_{loss,ray}}{\partial I_{buck}} &= \frac{\partial P_{bk,loss}}{\partial I_{buck}} + \frac{\partial E[P_{lin,loss}]}{\partial a_{bk}} \times \frac{\partial a_{bk}}{\partial I_{buck}} \\ &= \frac{\partial P_{bk,loss}}{\partial I_{buck}} + \frac{\partial E[P_{lin,loss}]}{\partial a_{bk}} \times \frac{R_L}{V_{FR}} \end{aligned} \tag{30}$$

The partial derivative of the buck converter's loss is computed as (31). This term may be directly combined with (14) or (26) to find bias terms that will minimize system loss.

$$\frac{\partial P_{bk,loss}}{\partial I_{buck}} = 2I_{buck} \times \left(\frac{V_{DC}}{V_{DD}}(R_{on,n} - R_{on,p}) + R_{on,p}\right) \tag{31}$$

By equating (29) with zero, the bias point where the system will observe minimized loss is expressed by (32a). While this expression does not have a clear analytical solution, numerical solutions are found quite readily with the aid of a computer or plotting the intersection to graphically determine the solution. Similarly, the expression for the optimum bias under a Rayleigh distributed envelope is described by (32b). While each of these individual expressions may appear to be complex, after evaluating fixed system parameters both (32a) and (32b) are specific forms of more general expressions of the form $0 = ax + b - f(x)$ where $f(x) = cos^{-1}(x)$ or $f(x) = e^{kx^2}$ for the two envelopes.

$$\begin{aligned} cos^{-1}(v_{off}) = {} & \frac{v_{off}}{v_{dd}} 2\pi \left(\frac{v_{dc}}{v_{dd}} \frac{R_{on,n} - R_{on,p}}{R_L} + \frac{R_{on,p}}{R_L}\right) \\ & + \frac{v_{dc}}{v_{dd}} 2\pi \left(\frac{v_{dc}}{v_{dd}} \frac{R_{on,n} - R_{on,p}}{R_L} \right. \\ & \left. + \frac{R_{on,p}}{R_L} + \frac{1}{2}\right) \end{aligned} \tag{32a}$$

$$\begin{aligned} e^{-\frac{\pi}{4}\left(\frac{a_{bk}}{\mu_a}\right)^2} = {} & 2\frac{a_{bk}}{v_{dd}} \left(\frac{v_{min} + \mu_a}{v_{dd}} \frac{R_{on,n} - R_{on,p}}{R_L} \right. \\ & \left. + \frac{R_{on,p}}{R_L}\right) + \frac{\mu_a}{v_{dd}} \\ & + 2\frac{v_{min}}{v_{dd}} \left(\frac{v_{min} + \mu_a}{v_{dd}} \frac{R_{on,n} - R_{on,p}}{R_L} \right. \\ & \left. + \frac{R_{on,p}}{R_L} + \frac{1}{2}\right) \end{aligned} \tag{32b}$$

IV. Theoretical Numerical Evaluation

A. Sinusoidal Numerical Evaluation

To perform a numerical evaluation, the normalized voltages used in the analytical development allow for the results to broadly describe various voltage configurations without being bound to the specific voltages employed in an example design. In this evaluation, the the normalized offset voltage ($v_{dc} = V_{DC}/V_0$) is lower bounded by 1 representing the extreme case where the envelope impinges upon 0V. The scaled supply voltage ($v_{dd} = V_{DD}/V_0$) must support this minimum offset, plus the magnitude of the waveform, and thus must be greater than $1+v_{dc}$. The surface shown in Fig. 5 shows the lowest-loss optimum solution for a variety of configurations from (15). Note this surface does not yet include the buck converter loss described in subsection III-C. Supply voltages available to designers are dictated by the environment where the ET system is implemented (e.g. automotive systems near 12V, mobile handsets near 3.7V as dictated by Lithium batteries, etc.). The extreme bounds of the envelope will be set by the modulation standard, with the device limitations used to implement the power converters in the ET modulator, and the PA load. By using the normalization method outlined, a broad set of distinct operating environments are evaluated simultaneously.

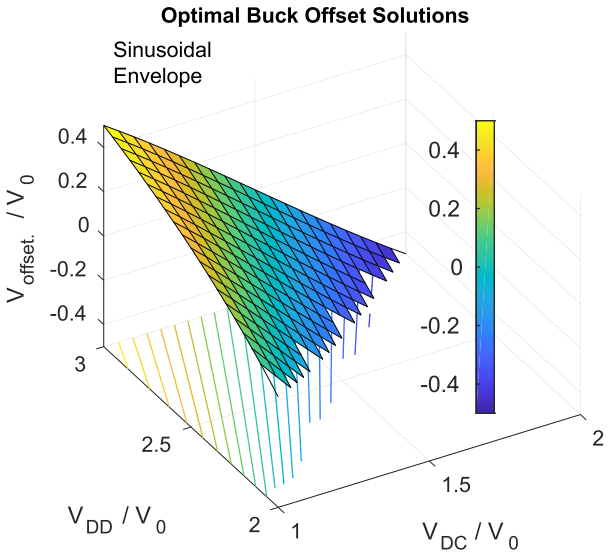

Fig. 5. The optimal buck offset from the sinusoidal envelope mean **neglecting buck converter loss**. Non-physical normalization terms are not plotted.

Solutions in the left side of the plotted surfaces correspond to design environments requiring larger headroom for the envelope tracking system and larger minimum acceptable voltages for the load, while points closer to the right hand edge of the surface correspond to envelope waveforms impinging upon the supply rails. The relative change in the loss term given this biasing change versus mean biasing is plotted in Fig. 6. The precise impact of this change on the system performance is dependent upon how large the linear stage's loss term is compared with any other loss terms in the system.

Finally, considering an example buck converter with a 2.8Ω low-side switch resistance, and a 7.5Ω high-side resistance driving a 50Ω load in a 3.3V design, the full system optimum and efficiency is evaluated. These resistances are given based upon device sizing used in subsection IV-D. The full system efficiency is computed numerically using equation (32a) and plotted in Fig. 8. The bias points required to produce the 8 are shown in 7. Finally, the absolute change in system efficiency compared with the conventional mean biasing is shown in Fig. 9. This represents the precise improvement a designer would observe under the proposed change. Observe that in all configurations, the proposed biasing change improves or at

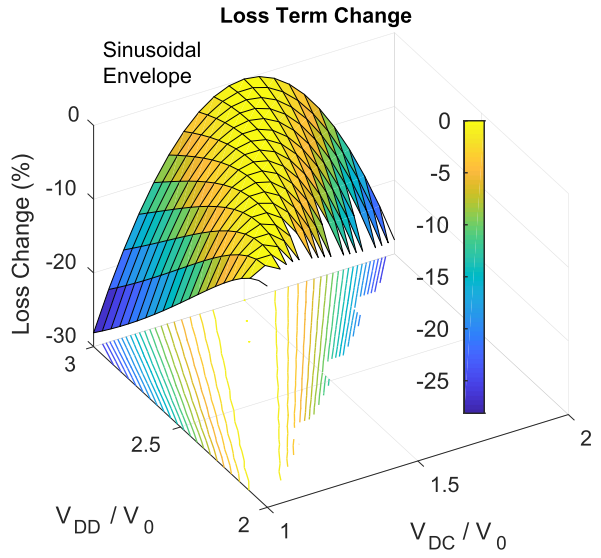

Fig. 6. Relative change in the intrinsic loss term when using optimum relative to mean biasing. Non-physical normalization values are not plotted.

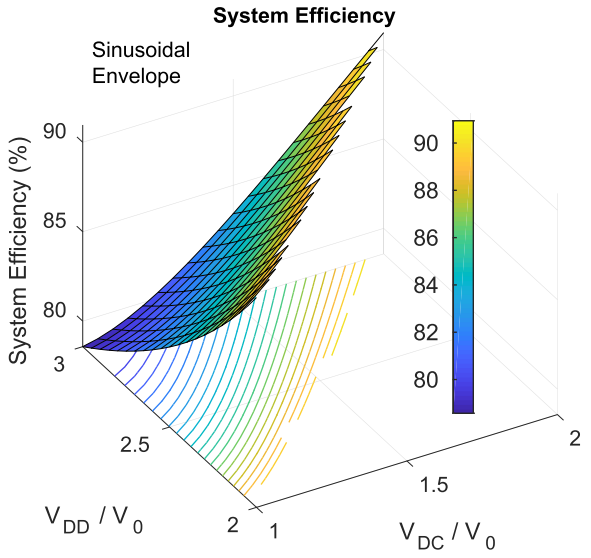

Fig. 8. System efficiency for an example system in various voltages configurations **including buck converter loss**. Non-physical normalization points are not plotted.

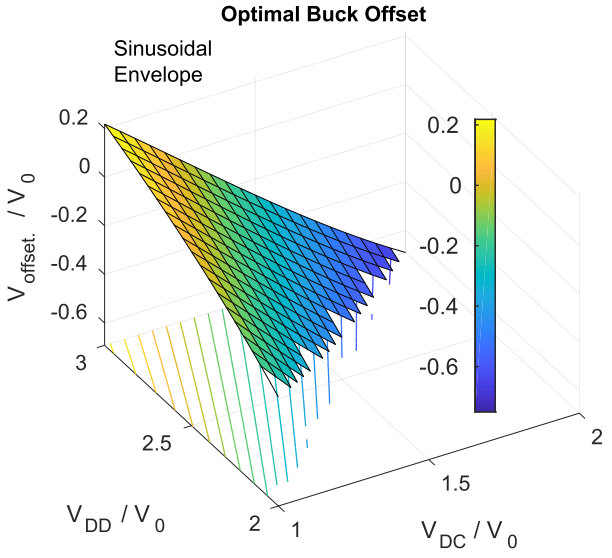

Fig. 7. The optimal buck offset from the sinusoidal envelope mean **including buck converter loss**. Non-physical normalization points are not plotted.

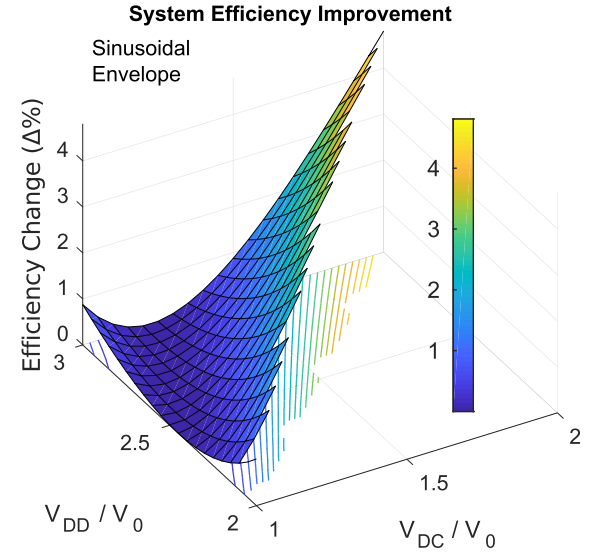

Fig. 9. Change in system efficiency for an example system in various voltages configurations **including buck converter loss** as compared with mean value biasing.

worst matches performance of mean biasing without introducing any changes to the topology.

B. Rayleigh Numerical Evaluation

Numerical evaluation of the optimum biasing for a Rayleigh distribution first requires the distribution behavior to be defined. For initial evaluation a mean value $\mu_a = 0.25$ is assumed. This corresponds to a PAPR[2] of -11dB, and a corresponding mode $\sigma_a = 0.199$, satisfying the error constraint ($\sigma_a < 0.33$) used in the formulation. Numerically this introduces an error term of less than 0.001%[3] into the final term of (25). The optimal set-point for the buck converter to produce theoretically minimized system loss as given in (27) is evaluated across a range of configurations and shown in Fig. 10.

Fig. 11 shows the evaluated system efficiency considering only this systematic loss term. This evaluation is of critical importance as *it demonstrates the theoretical limit of achievable efficiency given the hybrid buck-linear architecture.* The only loss term considered is systematic and essential to the operation of the circuit even in an ideal system. If a designer

[2]PAPR defined as ratio of peak to RMS signal amplitude. The RMS signal amplitude of a Rayleigh distribution is $\sigma_a\sqrt{2}$. Thus, PAPR $= -20log_{10}(\sigma_a\sqrt{2})$.

[3]$\sigma_a = 0.199 \rightarrow \%_{err} = exp(-\frac{1}{2}\sigma_a^{-2}) = 3.5 \times 10^{-6}$ (0.00035%).

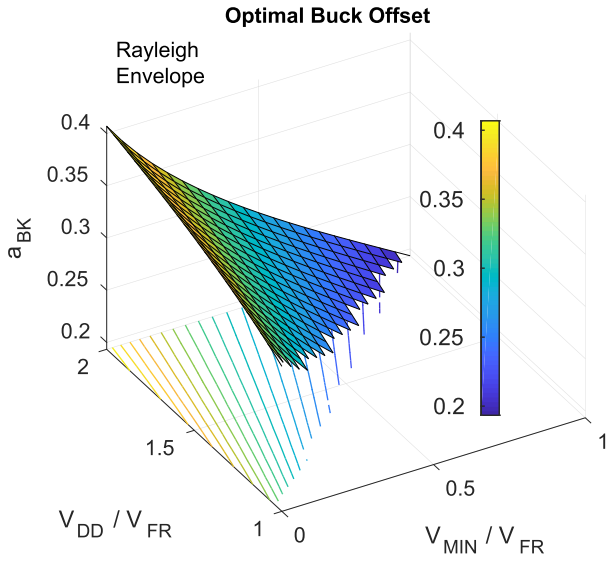

Fig. 10. The optimal buck offset for a Rayleigh envelope with an assumed $\mu_a = 0.25$ for various normalized minimum and envelope swing.

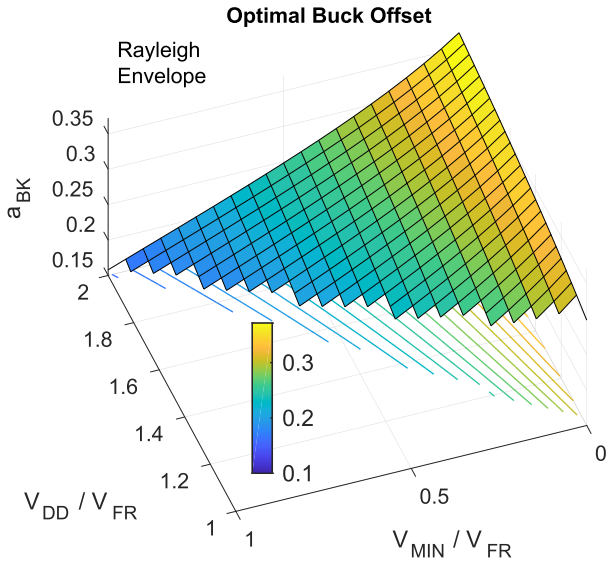

Fig. 12. The optimal buck offset for a Rayleigh envelope with an assumed $\mu_a = 0.25$ for various normalized minimum and envelope swing, **including losses of an example buck converter**.

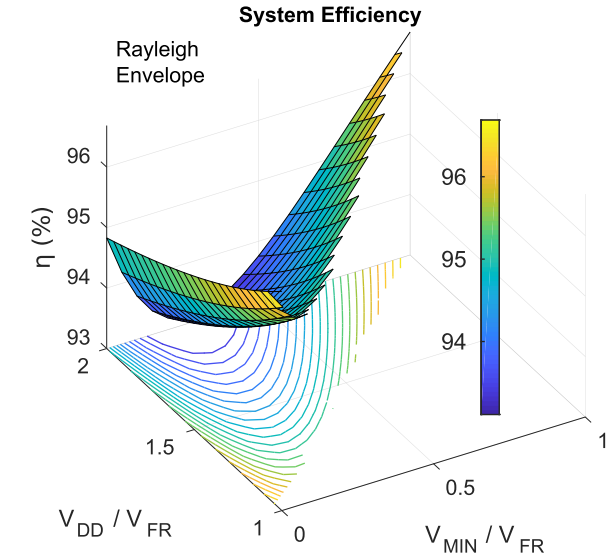

Fig. 11. Evaluated system efficiency of the system under a Rayleigh envelope in an otherwise lossless system when $\mu_a = 0.25$.

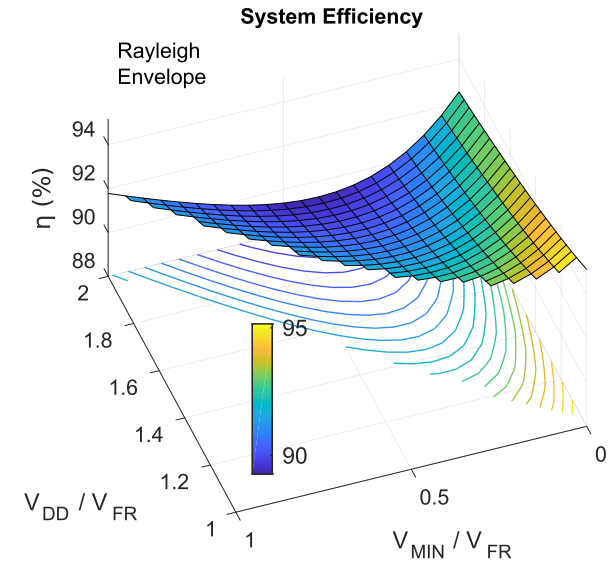

Fig. 13. Evaluated system efficiency of the system under a Rayleigh envelope in an otherwise lossless system when $\mu_a = 0.25$, **including losses of an example buck converter**.

opted to reduce the envelope bandwidth, or only track rising edges accurately, the power loss described in this paper would necessarily be dissipated as either by the linear stage, or by the load device.

As with the sinusoidal envelope evaluation, this process is repeated considering a system including losses of an example buck converter. The full system optimum bias is shown in Fig. 12, with corresponding full system efficiency shown in Fig. 13. To illustrate the significance of this biasing scheme to produce this change, the change in system efficiency as compared with mean waveform biasing is shown in Fig. 14. Authors wish to stress that as this improvement may be brought about simply by modifying the buck converter's nominal output current, and is thus an improvement available without major topology changes.

C. Performance vs PAPR

Of further interest is how the loss may vary under various PAPR constraints. The proposed biasing method exhibits more dramatic improvement over fixed biasing schemes as PAPR rises (i.e. becomes more extreme). Under the transformation used, a reduction in the normalized μ_a term versus the fixed maximum of 1 corresponds to increased PAPR. The system efficiency for the optimal bias versus two fixed bias schemes are shown in Fig. 15. In this sample evaluation $V_{DD} = 3.3$V,

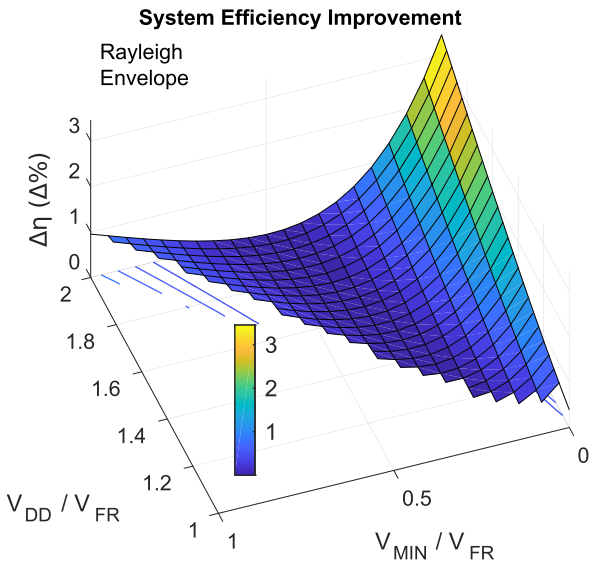

Fig. 14. Absolute change in system η with optimal versus mean (μ_a) biasing for a Rayleigh distributed envelope, **including losses of an example buck converter**.

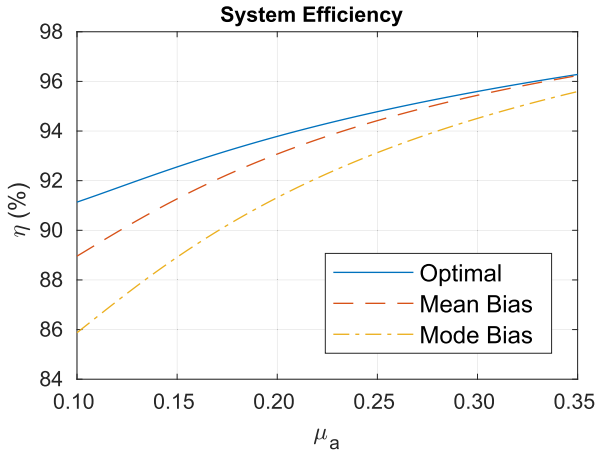

Fig. 15. Theoretical upper limit to system efficiency neglecting buck losses for various biasing schemes given various distribution means (μ_a) representing higher PAPR.

V_{MIN} = 0.5V, and V_{FR} = 2.4V is assumed, and buck converter losses are neglected.

D. Simulation Validation

To validate the described concept a simulated envelope tracking modulator was implemented in a 3.3V/1.8V 180nm CMOS process. The simulations were performed using the Spectre simulator through Cadence Virtuoso. A schematic of the modulator is shown in Fig. 16. The primary buck converter switching devices $M_{bk,p}$ and $M_{bk,n}$) have combined device widths of 1280μm and 192μm respectively, providing on-state resistances of 7.5Ω and 2.8Ω. These devices were driven by a non-overlapping driver to minimize shut current. All devices shown were implemented as thick-oxide devices to utilize a 3.3V fixed supply input. The buck converter inductor (L_{buck}) was implemented as a 100μH inductor with a 100mΩ equivalent-series-resistance (ESR). Furthermore, the results were found to be insensitive to variations in load resistance,

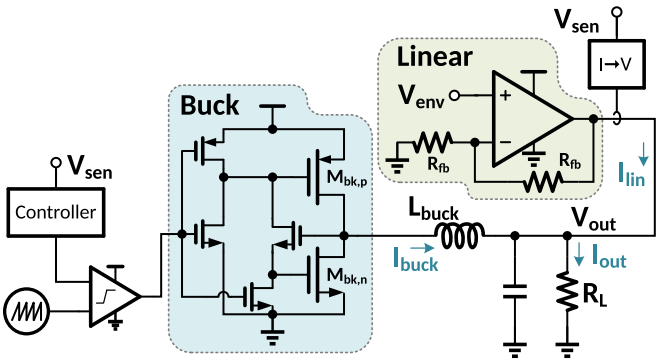

Fig. 16. A schematic of the simulated system.

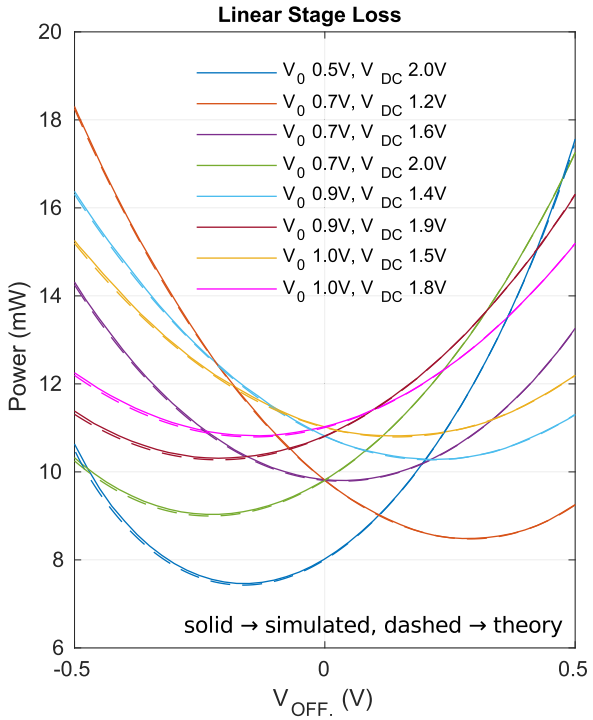

Fig. 17. A comparison of simulated and theoretical losses of the linear stage in the simulated envelope tracking modulator across various sinusoidal test cases.

and equivalent matching was observed using a 600mΩ ESR. The buck converter was driven with a 1MHz ramp signal while the system tracked a 5MHz sinusoidal envelope.

To minimize complexities associated with implementing an extreme bandwidth linear regulator, a behaviorally modeled linear regulator was used in the simulations. The amplifier used to implement the regulator was modeled with 60dB low frequency gain and a unity gain frequency of 100MHz. The regulator was configured in a low-gain configuration using matched feedback resistances as shown in Fig. 16. The simulations were performed for a sinusoidal envelope with various combinations of amplitude (V_0), and DC offset voltage (V_{DC}). Each combination was then simulated across offset voltages (V_{offset}) and the resulting power loss in the linear stage was measured and compared with the theoretical losses as described in equation (13). This comparison is shown in Fig. 17, and shows excellent agreement in the offset required

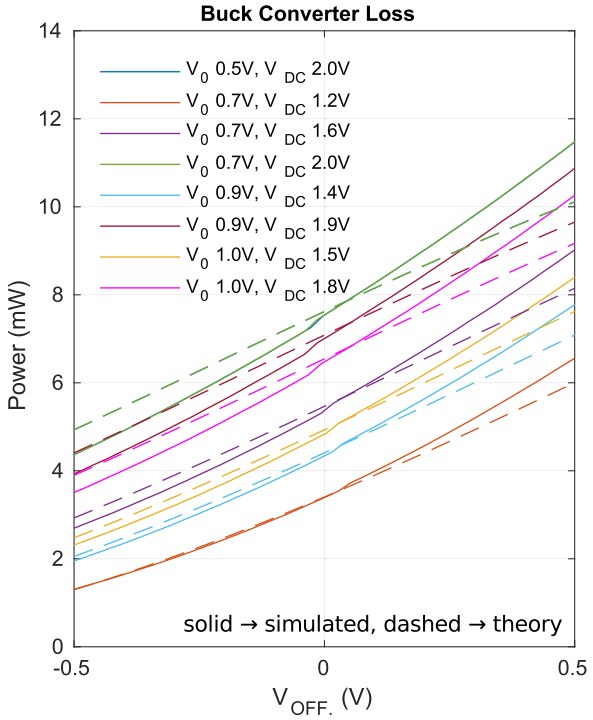

Fig. 18. A comparison of simulated and theoretical conduction losses of the buck converter stage in the simulated envelope tracking modulator across various sinusoidal test cases.

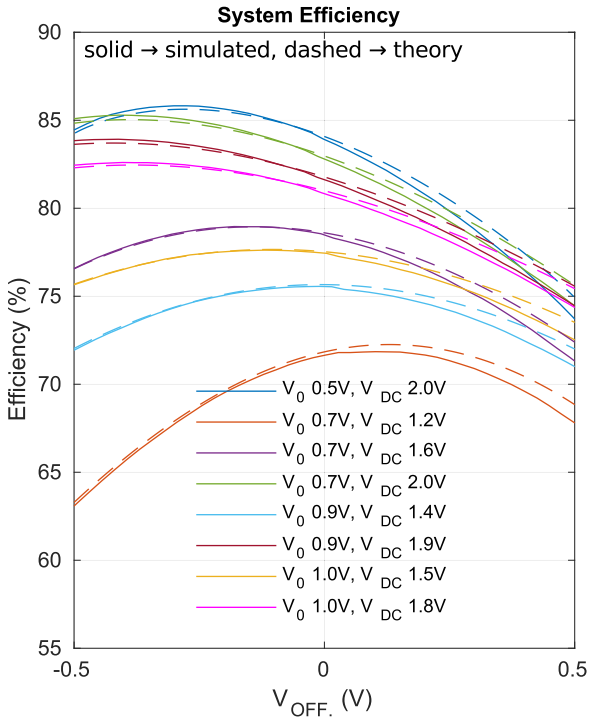

Fig. 19. A comparison of simulated and theoretical losses system efficiency across various sinusoidal test cases.

to produce minimized linear stage losses, as well as exact predicted power loss in the linear stage.

The full system efficiency was compared with the theoretically computed efficiency including buck converter losses described by (28). The theoretical and simulated buck converter conduction loss is shown in Fig. 18, with full system efficiency compared in Fig. 19. For positive values of V_{offset}, modeling of the buck converter limits the agreement between the system efficiency simulation and theory. In spite of this, the bias required to produce an efficiency maxima shows good agreement between simulation and theory, and generally shows the zero offset point to be sub-optimal with varying degrees of severity. For other switching converter topologies more sophisticated loss descriptions may be valuable to designers, but they do not affect the efficiency of the linear stage as shown in Fig. 17.

V. Conclusion

This work shows for envelope waveforms commonly used in envelope tracking systems, the design implementation chosen to asymmetrically favor zero linear-stage current unnecessarily burns extra power even in an ideal converter. Selection of a bias that nominally sinks or sources some small current on average may be used to minimize long term expected losses without requiring designers to change topology. To authors knowledge, this work shows for the first time, the upper bounds of achievable efficiency in the hybrid envelope modulator configuration.

Appendix A
Formulation of Sinusoidal Expected Losses

The integration of the cycle averaged power loss is given as (33) from the definition given in (12).

$$P_{lin,loss,avg} = \frac{1}{T}\int_T P_{lin,loss}(t)dt \tag{33}$$

As the loss is well described in two distinct regions, this integral is split over a period from t_1 to t_2 where I_{out} exceeds I_{buck}, and another region from t_2 to $t_1 + T$ where $I_{out} < I_{buck}$. The crossing points defining t_1 and t_2 are given when $I_{lin}(t) = 0$, or equivalently $sin(\omega t) = v_{off.}$. By nothing the symmetric relation of t_2 to t_1 about the maxima in I_{lin}, the intercept times are given as (34a-b).

$$t_1 = \frac{1}{\omega}sin^{-1}(v_{off.}) \tag{34a}$$

$$t_2 = \frac{T}{2} - \frac{1}{\omega}sin^{-1}(v_{off.})$$

$$t_2 = \frac{1}{\omega}\left(\pi - sin^{-1}(v_{off.})\right) \tag{34b}$$

As it will become valuable when performing this integral, we also note that the difference of these two points can be described as in (35).

$$\begin{aligned} t_2 - t_1 &= \frac{1}{\omega}\left(\pi - sin^{-1}(v_{off.})\right) - \frac{1}{\omega}sin^{-1}(v_{off.}) \\ &= \frac{2}{\omega}\left(\frac{\pi}{2} - sin^{-1}(v_{off.})\right) \\ &= \frac{2}{\omega}cos^{-1}(v_{off.}) \end{aligned} \tag{35}$$

For succinctness, the following steps will replace the scaling term $\frac{V_0^2}{R_L}$ as P. Rewriting (33) as it's constituent components produces (36).

$$P_{lin,loss,avg} = \frac{P}{T}\int_{t_1}^{t_2}[v_{dd} - v_{dc} - sin(\omega t)]$$

$$\times (sin(\omega t) - v_{off.})dt + \frac{P}{T}\int_{t_2}^{t_1+T}[-v_{dc} - sin(\omega t)] \times (sin(\omega t) - v_{off.})dt \quad (36)$$

Noting that all the terms in the second integral are present in the first, we can alternatively rewrite (36) as (37).

$$P_{lin,loss,avg} = \frac{P}{T}\int_{t_1}^{t_2} v_{dd} \times (sin(\omega t) - v_{off.})dt + \frac{P}{T}\int_{T} v_{dc}v_{off.} - sin(\omega t)(v_{dc} - v_{off.}) - \frac{1}{2}\big(1 - sin(2\omega t)\big)dt \quad (37)$$

The integral terms over entire periods of sine, become zero, producing a series of integrals over constants, and a single integration term over part of a sinusoid. The final computation prior to evaluating limits is given as (38).

$$P_{lin,loss,avg} = \frac{P}{T}\Big(\frac{-v_{dd}}{\omega}cos(\omega t)\Big|_{t_1}^{t_2} - v_{dd}v_{off.}(t_2 - t_1)\Big) + \frac{P}{T}\big(Tv_{dc}v_{off.} - \frac{T}{2}\big) \quad (38)$$

From here we can use simple geometric relations to redefine the cosine term in terms of our original definition of $v_{off.}$, and substitute the known expression for $t_2 - t_1$ to arrive at (39).

$$P_{lin,loss,avg} = P\left[\frac{v_{dd}}{\pi}\Big(\sqrt{1 - v_{off.}^2} - v_{off.}cos^{-1}(v_{off.})\Big) + \Big(v_{off.}v_{dc} - \frac{1}{2}\Big)\right] \quad (39)$$

Converting the substation term P back to $\frac{V_0^2}{R_L}$ results in (13).

Appendix B
Formulation of Rayleigh Expected Losses

Starting from (24) defined in section IV-B, we can rapidly solve the bulk of the integral by splitting it into various moments of the random variable, and moving scaling factors outside of the body of the integral. For compactness the leading scaling term ($\frac{V_{FR}^2}{R_L}$) will be succinctly renamed P, and the two integrals are independently renamed as I_1 and I_2 as shown in (40).

$$E[-] = P\int_0^{\infty} p_a(a)\Big[v_{min}a_{bk} + a(a_{bk} - v_{min}) - a^2\Big]da + P\int_{a_{bk}}^{\infty} p_a(a)\Big[v_{dd}(a - a_{bk})\Big]da$$
$$E[-] = PI_1 + PI_2 \quad (40)$$

The first integral I_1 is equivalent to (41), which is readily identifiable as a sum of various raw moments of the probability distribution. For the case of the Rayleigh distribution used here, the three moments (0th, 1st, and 2nd) are 1, $\sigma_a\sqrt{\frac{\pi}{2}}$, and $2\sigma_a^2$ respectively where σ_a is not the variance, but is the Rayleigh distribution parameter. As the 1st raw moment is also the distribution mean, these three terms are re-expressible as 1, μ_a, and $\frac{4}{\pi}\mu_a^2$. This produces a the compact form of I_1 shown in (42). Note that in this step the approximation mentioned in section III-B and IV-B takes place. The integral I_1 captures energy for extremely low probability symbols (those with high amplitude) in this integration step, even though these symbols do not exist in a true OFDM waveform.

$$I_1 = \big(v_{min}a_{bk}\big)\int_0^{\infty} p_a(a)da + \big(a_{bk} - v_{min}\big)\int_0^{\infty} a\,p_a(a)da + \big(-1\big)\int_0^{\infty} a^2 p_a(a)da. \quad (41)$$

$$I_1 = \big(v_{min}a_{bk}\big) + \big(a_{bk} - v_{min}\big)\mu_a - \frac{4}{\pi}\mu_a^2. \quad (42)$$

The precise impact of this approximation is determined first by computing a distribution parameter that will ensure an arbitrarily small error. By using the cumulative density function, and evaluating energy from 1 to ∞, truncation error is computed as: $\%_{err} = exp(-\frac{1}{2}\sigma_a^{-2})$. For $\%_{err} < 0.01$ (1%) this necessitates $\sigma_a < 0.3295$. For $\%_{err} < 0.001$ (0.1%) we instead require $\sigma_a < 0.269$. In the evaluation presented in subsection IV-B a distribution parameter of $\sigma_a = 0.199$ was used, introducing an error term in the integration step of roughly 3.5×10^{-6} or 0.00035%.

The second integral is less convenient as it does not contain the entire distribution domain, but it's structure still allows for a tractable solution. By splitting the terms a plain integral of the distribution can be re-expressed as the complementary integral to the distribution's cumulative distribution function (i.e. the integral from the left hand side to a point, rather than from the right hand side). The other term is a well known integral of a squared exponential of the form $x^2e^{-\frac{1}{2}x^2}$. This is found using integration by parts with the terms x and $xe^{-\frac{1}{2}x^2}$. The result is re-expressed in terms of the distribution parameter σ_a as shown in (43).

$$I_2 = v_{dd}\int_{a_{bk}}^{\infty} ap_a(a)da - a_{bk}v_{dd}\int_{a_{bk}}^{\infty} p_a(a)da$$
$$I_2 = v_{dd}\int_{a_{bk}}^{\infty}\Big(\frac{a}{\sigma_a}\Big)^2 e^{-\frac{1}{2}(\frac{a}{\sigma_a})^2}da - a_{bk}v_{dd}\Big(1 - CDF_a(a_{bk})\Big)$$
$$I_2 = v_{dd}\int_{a_{bk}}^{\infty}\Big(\frac{a}{\sigma_a}\Big)^2 e^{-\frac{1}{2}(\frac{a}{\sigma_a})^2}da - a_{bk}v_{dd}\Big(e^{-\frac{1}{2}(\frac{a_{bk}}{\sigma_a})^2}\Big) \quad (43)$$

By using integration by parts, I_2 becomes the following expression, where $erfc(x)$ is the complementary error function $\frac{2}{\sqrt{\pi}}\int_x^{\infty} e^{-y^2}dy$.

$$I_2 = v_{dd}\Big(a_{bk}e^{-\frac{1}{2}(\frac{a_{bk}}{\sigma_a})^2} + \mu_a erfc\big(\frac{a_{bk}}{\sigma_a}\big)\Big) - a_{bk}v_{dd}\Big(e^{-\frac{1}{2}(\frac{a_{bk}}{\sigma_a})^2}\Big)$$
$$I_2 = v_{dd}\mu_a erfc\big(\frac{1}{\sqrt{2}}\frac{a_{bk}}{\sigma_a}\big) \quad (44)$$

Finally, by re-substituting the terms found here back into (40), and re-expressing the distribution parameter σ_a in

terms of the distribution mean μ_a, the we arrive at (25) as presented earlier.

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Luke Renaud (S'13) received the B.S. degree *(summa cum laude)* in electrical engineering from Washington State University, Pullman, WA, USA, in 2013, where he is currently pursuing the Ph.D. degree in RF microelectronics.

In 2015 and 2016, he was an intern with EM Microelectronic-US, Colorado Springs, CO, USA, where he conducted research on low-power sensing methods for human interface devices. In 2018, he began work at Blue Origin, Kent, WA, USA. His current research work includes the development of new envelope tracking systems, and RF blocks for use in millimeter-wave systems.

Joseph Baylon received the B.Eng. degree from The Cooper Union, New York, NY, USA, in 2012. He is currently pursuing the Ph.D. in electrical engineering with Washington State University.

His research focuses on low-power, wideband mm-wave wireless transceiver design for wireless network-on-chip.

Srinivasan Gopal (S'13) received the B.Tech. and M.Tech. degrees in electrical engineering from IIT Madras, Chennai, India, in 2008, and the Ph.D. degree from the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA, in 2018. From 2008 to 2012, he held analog mixed-signal design engineering positions with Intersil and also with PMC-Sierra, and involved in precision data converter design and optical links.

From 2015 to 2016, he was an Analog Serial I/O Design Intern with Intel, San Jose, CA, USA, where he developed highspeed wireline transceiver designs for field-programmable gate arrays. His current research interests include wireless 3-D interconnect-based high-speed links and time-domain signal processing for neuromorphic computing. He was a recipient of the Harold and Diana Frank Fellowship Award in 2018, and nominations for the Best Paper Awards at the 2018 IEEE-MTTS International Microwave Symposium and the 2017 IEEE/ACM International Symposium on Networks-on-Chip Symposium and Intersil Summit Award in 2011.

Md Aminul Hoque received the B.S. degree in electrical engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2013, and the M.S. degree in electrical engineering from the University of Idaho, Moscow, ID, USA, in 2017. He is currently pursuing the Ph.D. degree in RF microelectronics with Washington State University, Pullman, WA, USA.

His current research interests include the development of RF blocks for use in millimeter wave systems for wireless communications.

Deukhyoun Heo (S'97–M'00–SM'13) received the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2000. In 2000, he joined National Semiconductor Corporation, Santa Clara, CA, USA, where he was a Senior Design Engineer involved in the development of silicon RFICs for cellular applications.

In 2003, he joined the Faculty of Electrical Engineering and Computer Science Department, Washington State University, WA, USA, where he is currently the Frank Brands Analog Distinguished Professor of electrical engineering. He has authored or co-authored approximately 120 publications, including 55 peer-reviewed journal papers and 66 international conference papers. His current research interests include RF/microwave/opto transceiver design based on CMOS, SiGe BiCMOS, and GaAs technologies for wireless and wireline data communications, batteryless wireless sensors and intelligent power management system for sustainable energy sources, adaptive beam formers for phased-array communications, lowpower high data-rate wireless links for biomedical applications, and multilayer module development for system-in-package solutions.

Dr. Heo is a Technical Program Committee Member of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), the IEEE MTT-S International Microwave Symposium (IMS), and the International Symposium of Circuit and Systems. He was a recipient of the 2000 Best Student Paper Award presented at the IEEE MTT-S IMS and the 2009 National Science Foundation CAREER Award. He served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS Part II: Express Briefs from 2007 to 2009 and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.