Analog-Assisted Digital Capacitorless Low-Dropout Regulator Supporting Wide Load Range

Nghia Tang, *Member, IEEE*, Yangyang Tang, *Member, IEEE*, Zhiyuan Zhou, *Student Member, IEEE*, Bai Nguyen, *Student Member, IEEE*, Wookpyo Hong, *Student Member, IEEE*, Philipp Zhang, *Member, IEEE*, Jong-Hoon Kim, and Deukhyoun Heo, *Senior Member, IEEE*

***Abstract*—Capacitorless (CL) low-dropout regulators (LDO) have gained significant research interest for point-of-load voltage regulation without off-chip capacitors. While analog CL-LDOs can deliver superior power supply rejection (PSR), digital CL-LDOs are more scalable and efficient. To achieve the advantages of both types, this paper presents a digital CL-LDO with an analog PSR enhancer, delivering strong PSR without compromising scalability and efficiency. Load regulation is performed by an asynchronous digital feedback controller for fast transient response and scalable load drivability. PSR is achieved by a load-insensitive wide-bandwidth analog controller. A prototype chip of the analog-assisted digital CL-LDO is fabricated in a 130-nm CMOS process with an active area of 0.0645 mm^2, supporting load current up to 50 mA at nominal 1-V input and 0.8-V output. The measured PSR is better than –20 dB for frequencies up to 10 MHz, and the measured current efficiency peaks at 99.3%, with average current efficiency of 96.7% across 50× load range. The measured transient response to a full load step, with two values of load capacitance (100 pF and 10 nF), demonstrates the LDO's stable operation over a wide range of load resistance and capacitance.**

***Index Terms*—Analog control, capacitorless (CL), digital control, low-dropout regulator (LDO), power supply rejection (PSR).**

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N. Tang, Z. Zhou, B. Nguyen, W. Hong, and D. Heo are with the Department of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99164 USA (e-mail: ntang@eecs.wsu.edu; zzhou@eecs.wsu.edu; bnguyen@eecs.wsu.edu; whong@eecs.wsu.edu; dheo@wsu.edu).

Y. Tang is with the Research Department of HiSilicon, Huawei, Shenzhen 518129, China (e-mail: tangyangyang@hisilicon.com).

P. Zhang is with the Research Department of HiSilicon, Huawei, Plano, TX 75024 USA (e-mail: philipp.zhang@huawei.com).

J.-H. Kim is with the Korea Food Research Institute, Sungnam 463-764, South Korea (e-mail: jhkim@kfri.re.kr).

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I. Introduction

LOW-DROPOUT regulators (LDOs) are widely used following switched-mode converters to produce clean supply voltages for noise-sensitive circuits [1]–[5]. Due to system miniaturization, the switching frequency of switched-mode converters has increased beyond 1 MHz to accommodate small inductors and capacitors. Power supply rejection (PSR) in the megahertz range has thus become an important LDO specification. While LDOs with off-chip capacitors typically have robust performance with great PSR [6]–[8], capacitorless (CL) LDOs (without off-chip capacitors) have recently gained popularity for their point-of-load regulation and smaller system size. Yet, without a large off-chip capacitor to filter noise, the PSR of a CL-LDO is compromised at high frequencies.

An LDO can use either an analog control scheme or a digital control scheme to regulate its output voltage $V_{\rm out}$ at a specified load current $I_{\rm load}$. In an analog LDO, see Fig. 1(a), transistor M_0 is operated in the saturation (or triode region under heavy loads) by an analog controller, and $V_{\rm out}$ is regulated by controlling the gate voltage of M_0. On the other hand, a digital LDO, see Fig. 1(b), uses a digital controller to operate transistors M_1–M_N as switches in the triode region, and $V_{\rm out}$ is regulated by controlling the number of turned-ON switches. In Fig. 1, $R_{\rm load}$ and $C_{\rm load}$ are the resistance and capacitance of a load, and $C_{\rm off}$ is an optional off-chip capacitor (not present in a CL-LDO). Compared to the analog counterparts, digital LDOs are known to offer advantages in size, scalability, low-voltage operation, and stability over a wide dynamic range [9]. This is mainly due to the ability to use the entire rail-to-rail supply voltage range to operate the transistors as switches and the flexibility to increase the number of transistors when the load range expands. However, digital LDOs suffer from worse PSR than their analog counterparts because the gate voltages of M_1–M_N cannot be modulated to reject supply noise. An attempt to improve the PSR of digital LDOs is proposed in [10], where supply noise rejection is accomplished by dynamically adjusting the number of turned-ON switches. Although this fully digital technique is capable of low-voltage operation, the PSR is only −16 dB due to the limited speed and resolution of the digital controller. Recently, a hybrid design that uses a digital LDO and an analog LDO in parallel has been presented to combine the advantages

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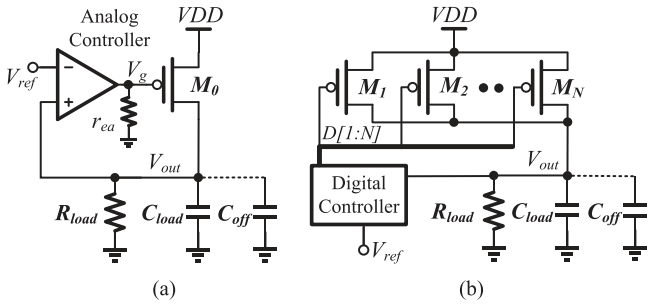

Fig. 1. Basic schematic of (a) analog LDO and (b) digital LDO.

of both topologies [11]. The digital LDO part features fast response to large load disturbances, and it can operate at a supply voltage as low as 0.6 V. The analog LDO part delivers a finetuning current to produce low-noise output voltage when the supply is above 1.1 V. This hybrid design can deliver fast load response, scalability, and low-voltage operation from digital control, together with superior PSR from analog control when the supply voltage is sufficiently high for analog circuits to operate. However, the reported PSR is only about -12 dB despite the help of an analog LDO, which is worse than other analog LDOs operating at similar supply voltages [12], [13]. One reason is that in the hybrid design, the analog LDO part must compensate the supply injected noise of both itself and the digital LDO part. Therefore, it is more challenging to design the analog part in a high-PSR hybrid LDO, compared to a high-PSR standalone analog LDO. Since hybrid designs offer advantages of both digital and analog control schemes, they present interesting opportunities that are worth further investigation and development. In this paper, we propose an analog-assisted digital CL-LDO with better PSR while maintaining the scalable and efficient nature of digital LDOs. This is achieved by improving the performance of the analog part with the help of the digital part. To understand how the digital part complements and improves the analog part, it is worth studying the limitations of analog LDOs.

In an analog LDO, see Fig. 1(a), the feedback loop gain $LG(s)$ is typically a second-order transfer function with an output pole at $V_{\rm out}$ and an internal pole at V_g [13]. One of these two poles should be dominant to make a stable feedback loop. For good PSR over a wide range of frequencies, a feedback loop with large gain-bandwidth (GBW) and a dominant output pole is desirable [13], [14]. If a large off-chip capacitor $C_{\rm off}$ on the order of μF is connected at $V_{\rm out}$, it creates a large output capacitance and accordingly a dominant output pole. Without $C_{\rm off}$ in a CL-LDO, the output capacitance is mostly contributed by $C_{\rm load}$, which is typically on the order of pF [14]. An on-chip capacitor can be added to increase the output capacitance, but it is typically below 1 nF due to silicon area constraint. Therefore, the output pole of a CL-LDO is at a relatively high frequency and close to the internal pole. Since the output pole varies with the load condition, i.e., the values of $R_{\rm load}$ and $C_{\rm load}$, it is difficult to design a feedback loop with large GBW and a dominant output pole. One technique to create a dominant output pole in a CL-LDO is to push the internal pole to a higher frequency by using a buffer [13]. Yet, a limit on the maximum load current $I_{\rm load}$ (or minimum $R_{\rm load}$) must be enforced to prevent the output pole from approaching the internal pole and causing instability. Additionally, the buffer consumes a large bias current to drive a large power transistor at heavy loads, resulting in low current efficiency at light loads. In [14], a capacitance multiplier is used to turn a small on-chip capacitor into a large active output capacitor and thus create a dominant output pole. This technique also degrades current efficiency at light loads because a large bias current is required to achieve a large capacitance multiplication factor. Another PSR-enhancing technique [15] is to use cascaded devices to increase the isolation between $V_{\rm out}$ and the supply voltage VDD, but it is not suitable for LDOs with low-dropout voltage. Ripple feedforward techniques are also effective in improving PSR [12], [16]–[18], but the matching requirements for effective ripple cancellation increase the design complexity, especially at low VDD. More importantly, these CL-LDOs [12], [15]–[18] also have instability issues due to the load-dependent output pole [14].

The load-dependent output pole indeed poses a challenge to the design of a stable large-GBW analog feedback controller. This is also a factor that limits the PSR performance of the hybrid LDO in [11]. To address the load-dependent output pole, Kwok and Mok [19] propose a pole-zero-tracking compensating technique. However, this technique requires prior knowledge of the output capacitance, which is not necessarily predetermined in CL-LDOs [14]. A replica compensated structure is proposed in [20] to make the loop gain independent of the output capacitance. This technique is very effective in improving the stability, bandwidth, and PSR, but it can only be used to support a limited load range because the replica loop makes the regulator unresponsive to load changes. Nevertheless, it is noticed that this replica compensated structure can work in harmony with a digital controller to build a high-PSR analog-assisted digital CL-LDO supporting a wide load range. We propose to design a wide-bandwidth analog PSR enhancer, based on the replica compensated structure with robust stability for a wide range of load capacitance, and use a digital regulator to regulate the output voltage across a scalable, wide range of load current. Section II will describe the proposed analog-assisted digital CL-LDO in detail, and Section III will present the experimental results of a prototype chip.

II. Analog-Assisted Digital CL-LDO

A system-level schematic of the proposed analog-assisted digital CL-LDO is illustrated in Fig. 2. The power stage contains N power switches, each composed of P-channel MOSFET (PMOS) transistors $M_1[i]$, $M_2[i]$, and $M_3[i]$ for $i \in [1:N]$. The load current $I_{\rm load}$ is contributed by the current I_1 from the array $M_1[1:N]$ and the current I_2 from the array $M_2[1:N]$. Load regulation is performed by a digital regulator that produces a digital signal $\overline{D[1:N]}$ to control the transistors in the arrays $M_2[1:N]$ and $M_3[1:N]$. $M_2[i]$ and $M_3[i]$ are operated as switches, which are either turned ON in the triode region (i.e., gate terminals pulled to GND) or turned OFF (i.e., gate terminals pulled to VDD). Transistors in the array $M_1[1:N]$ are controlled in the saturation region by an analog PSR enhancer, and their drain cur-

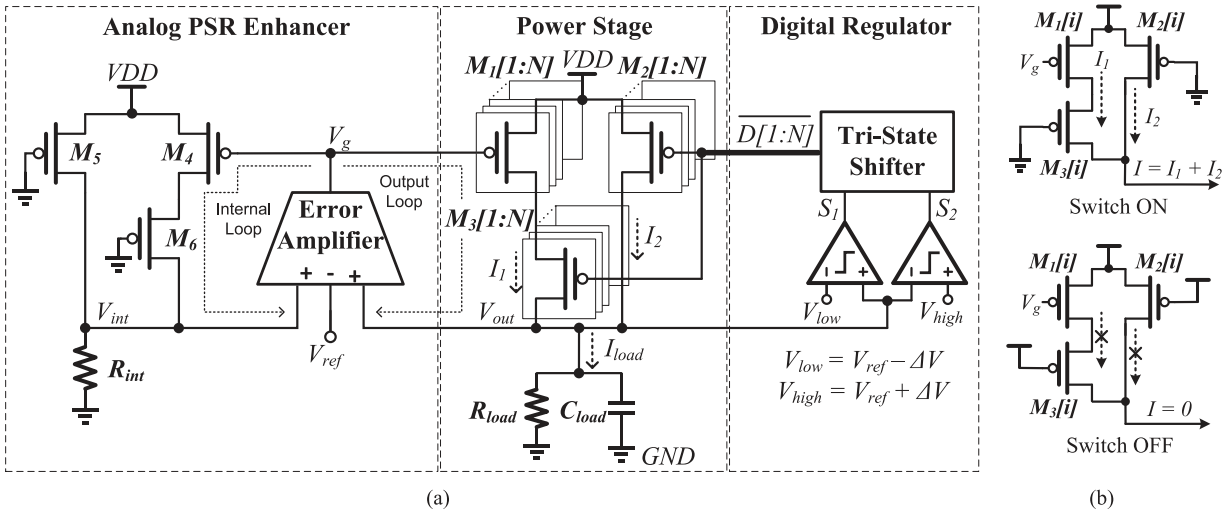

Fig. 2. (a) Proposed analog-assisted digital CL-LDO. (b) Operation of a power switch in the power stage.

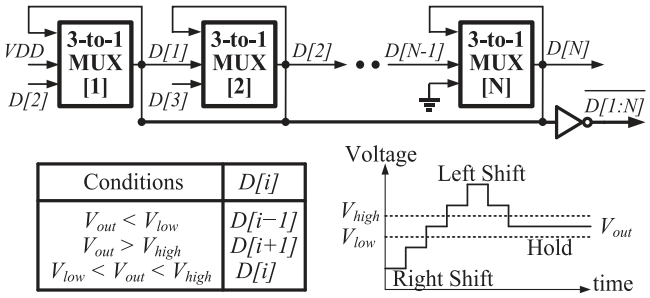

Fig. 3. Schematic and operation of the tri-state shifter.

rents are gated by $M_3[1:N]$. When I_{load} increases, the digital regulator turns ON more transistors in the arrays $M_2[1:N]$ and $M_3[1:N]$, which effectively increases the currents I_1 and I_2. It is worth noting that the ratio I_1/I_2 is constant, and $I_1 \ll I_2$. Under the operation of the digital regulator, V_{out} is regulated into a voltage window bounded by V_{low} and V_{high}, which are respectively ΔV smaller and larger than a reference voltage V_{ref}. The PSR enhancer uses an analog feedback loop to modulate I_1 to reject supply noise from VDD. Essentially, the digital regulator regulates V_{out} against load disturbances, while the analog PSR enhancer suppresses voltage ripple injected from VDD.

A. Digital Regulator

The digital regulator in Fig. 2 mainly consists of a tristate shifter that shifts $\overline{D[1:N]}$ depending on the value of V_{out} relative to V_{low} and V_{high}. The tristate shifter shown in Fig. 3 is simply a chain of N cascaded 3-to-1 multiplexers (MUX).

If $V_{\text{out}} < V_{\text{low}}$, $D[i-1]$ is right shifted to $D[i]$. If $V_{\text{out}} > V_{\text{high}}$, $D[i+1]$ is left shifted to $D[i]$. If $V_{\text{low}} < V_{\text{out}} < V_{\text{high}}$, $D[i]$ is hold and unchanged, and the digital regulator reaches a steady state. MUX$[1]$ does not have a preceding stage, and VDD is used as the preceding value. MUX$[N]$ does not have a succeeding stage, and GND is used as the succeeding value. $D[1:N]$ is then inverted to drive the PMOS transistors in the arrays $M_2[1:N]$ and $M_3[1:N]$. The operation is asynchronous without a reference clock signal and totally based on combinational logics of VDD, GND, and $D[1:N]$. The asynchronous controller in [10] also operates without a reference clock, but it uses a bidirectional shifter with only *left* and *right* shifts while the *hold* state is asserted by a *freeze* command sent from a top-level system. The shifter in [11] has a similar behavior to the tristate shifter, i.e., it automatically stops shifting when $V_{\text{low}} < V_{\text{out}} < V_{\text{high}}$, but the operation is synchronous, requiring a reference clock. Asynchronous and synchronous modes have their own advantages and disadvantages. The tristate shifter is designed with an asynchronous mode to achieve fast shifting, only limited by the delay of combinational logic circuits [10], which is however quite sensitive to process–temperature–voltage variations. The switching threshold ΔV should be set properly to ensure a stable operation. A tight threshold delivers accurate dc setting of V_{out}, which requires the power switches to be sized with fine resolution and the comparators to have high speed and high sensitivity.

B. Analog PSR Enhancer

In Fig. 2, the analog PSR enhancer includes M_4, M_5, and M_6 being scaled replicas of $M_1[i]$, $M_2[i]$, and $M_3[i]$, respectively. M_5 and M_6 are always turned ON (i.e., gate terminals tied to GND). M_4 is controlled by V_g, the same signal that controls $M_1[i]$. The currents from M_4 and M_5 flow into an internal resistor R_{int} and produce an internal voltage V_{int}. To analyze the PSR enhancer, let us assume that the LDO has reached the steady state, i.e., $V_{\text{low}} < V_{\text{out}} < V_{\text{high}}$, and k power switches are turned ON to provide I_{load}. This means that the gate terminals of $M_2[1:k]$ and $M_3[1:k]$ are pulled to GND while those of $M_2[(k+1):N]$ and $M_3[(k+1):N]$ are pulled to VDD. Therefore, $M_1[1:k]$ and $M_2[1:k]$ are providing the load current. In term of small-signal behavior, $M_2[1:k]$ and $M_3[1:k]$ in the triode region can be modeled by on-resistance r_{ds2} and r_{ds3}; whereas, $M_1[1:k]$ in the saturation region can be modeled by transconductance g_{m1} and output impedance r_{ds1}.

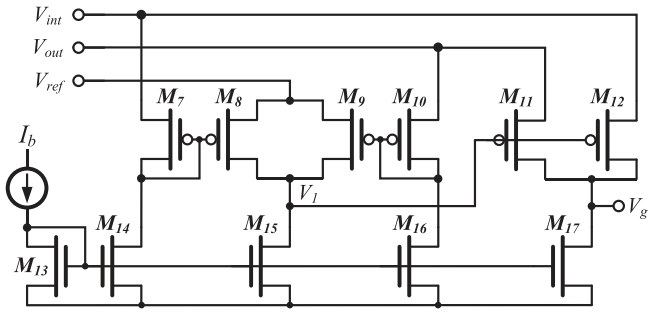

Fig. 4. Schematic of the error amplifier in the analog PSR enhancer.

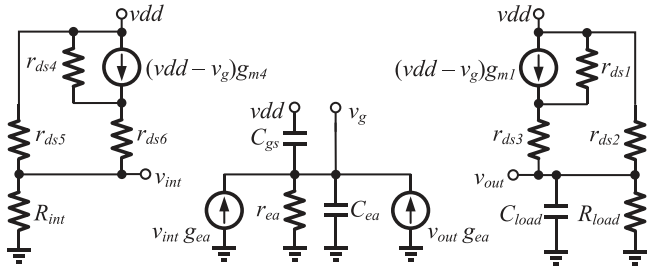

Fig. 5. Small-signal model of the analog PSR enhancer.

The turned-OFF transistors contribute parasitic capacitance to the system. Similarly, the small-signal effects of M_4 are modeled by r_{ds4} and g_{m4}, and M_5 and M_6 are modeled by r_{ds5} and r_{ds6}, respectively.

A schematic of the error amplifier is shown in Fig. 4. Transistors $M_7 - M_{10}$ are matched, and transistors $M_{11} - M_{12}$ are matched. Transistors $M_{14} - M_{16}$ are sized such that their drain currents are related by $2I_{d14} = I_{d15} = 2I_{d16}$. The relationship between small signals $v_{\rm int}$, $v_{\rm out}$, $v_{\rm ref}$, and v_g can be obtained

$$v_g = (v_{\rm int} + v_{\rm out})\,(1 + 2g_{m7}r_{o1})\,g_{m11}r_{ea} - 4v_{\rm ref}g_{m7}r_{o1}g_{m11}r_{ea} \tag{1}$$

where g_{m7} is the transconductance of $M_7 - M_{10}$, g_{m11} is the transconductance of $M_{11} - M_{12}$, r_{o1} is the output impedance at node V_1, and r_{ea} is the output impedance at node V_g. By defining $g_{ea} = (1 + 2g_{m7}r_{o1})g_{m11}$ and $v_{\rm ref} = 0$ (constant $V_{\rm ref}$), (1) can be simplified as follows:

$$v_g = (v_{\rm int} + v_{\rm out})\,g_{ea}r_{ea}. \tag{2}$$

A small-signal model of the analog PSR enhancer is shown in Fig. 5. The error amplifier is modeled by g_{ea} and r_{ea}, the effective capacitance between V_g and GND is modeled by C_{ea}, and the capacitance between V_g and VDD is modeled by C_{gs}. The loading effect of the error amplifier, which pulls microamps of current from $V_{\rm int}$ and $V_{\rm out}$, is small relative to those of $R_{\rm int}$ and $R_{\rm load}$, and thus can be ignored. By using Kirchhoff's current law, the following equations can be derived:

$$\frac{v_{\rm out}}{R_{\rm load}}(1 + sR_{\rm load}C_{\rm load}) = \frac{(vdd - v_g)\,g_{m1}r_{ds1}}{r_{ds1} + r_{ds3}} + \frac{vdd - v_{\rm out}}{r_{ds1} + r_{ds3}} + \frac{vdd - v_{\rm out}}{r_{ds2}} \tag{3}$$

$$\frac{v_{\rm int}}{R_{\rm int}} = \frac{(vdd - v_g)\,g_{m4}r_{ds4}}{r_{ds4} + r_{ds6}} + \frac{vdd - v_{\rm int}}{r_{ds4} + r_{ds6}} + \frac{vdd - v_{\rm int}}{r_{ds5}} \tag{4}$$

$$\frac{v_g}{r_{ea}}(1 + sC_{ea}r_{ea}) = (v_{\rm out} + v_{\rm int})\,g_{ea} + (vdd - v_g)\,sC_{gs}. \tag{5}$$

Since $M_1[1:k]$ are in the saturation region, while $M_2[1:k]$ and $M_3[1:k]$ are in the triode region, r_{ds1} is much larger than r_{ds2} and r_{ds3}. Similarly, r_{ds4} is much larger than r_{ds5} and r_{ds6}. Equations (3)–(5) can be further simplified by arranging the terms as follows:

$$v_{\rm out}\left(\frac{1 + s/\omega_{p1}}{r_{\rm out}}\right) = vdd\left(g_{m1} + \frac{1}{r_{ds2}}\right) - v_g g_{m1} \tag{6}$$

$$\frac{v_{\rm int}}{r_{\rm int}} = vdd\left(g_{m4} + \frac{1}{r_{ds5}}\right) - v_g g_{m4} \tag{7}$$

$$v_g\left(\frac{1 + s/\omega_{p2}}{r_{ea}}\right) = (v_{\rm out} + v_{\rm int})\,g_{ea} + sC_{gs}vdd \tag{8}$$

where $r_{\rm out} = \frac{R_{\rm load}r_{ds2}}{R_{\rm load}+r_{ds2}}$, $r_{\rm int} = \frac{R_{\rm int}r_{ds5}}{R_{\rm int}+r_{ds5}}$, $\omega_{p1} = \frac{1}{r_{\rm out}C_{\rm load}}$, and $\omega_{p2} = \frac{1}{r_{ea}(C_{ea}+C_{gs})}$. Notice that ω_{p1} is the output pole, which varies with the load condition, i.e., $R_{\rm load}$ and $C_{\rm load}$.

By breaking the feedback loop at v_g and setting $vdd = 0$, the system loop gain can be derived as follows:

$$LG(s) = \frac{LG_{\rm int}}{1 + s/\omega_{p2}} + \frac{LG_{\rm out}}{(1 + s/\omega_{p1})\,(1 + s/\omega_{p2})} = \frac{(LG_{\rm int} + LG_{\rm out})}{(1 + s/\omega_{p1})\,(1 + s/\omega_{p2})} \times \left(1 + \frac{s}{(1 + LG_{\rm out}/LG_{\rm int})\,\omega_{p1}}\right) \tag{9}$$

where $LG_{\rm int} = g_{m4}r_{\rm int}g_{ea}r_{ea}$ is the dc gain of the internal loop, and $LG_{\rm out} = g_{m1}r_{\rm out}g_{ea}r_{ea}$ is the dc gain of the output loop. In steady state, $V_{\rm out} = V_{\rm int} = V_{\rm ref}$, and the following relationship can be achieved:

$$\frac{g_{m1}}{g_{m4}} \cong \frac{r_{ds5}}{r_{ds2}} \cong \frac{R_{\rm int}}{R_{\rm load}} \cong \frac{r_{\rm int}}{r_{\rm out}}. \tag{10}$$

Thus, $LG_{\rm int} \cong LG_{\rm out} \cong LG_0$, and (11) can be simplified as follows:

$$LG(s) \cong \frac{2LG_0\,(1 + s/2\omega_{p1})}{(1 + s/\omega_{p1})\,(1 + s/\omega_{p2})}. \tag{11}$$

In comparison with the loop gain equation of a conventional analog LDO, (11) has an additional factor of $2(1 + s/2\omega_{p1})$ in the numerator. Effectively, the internal loop adds an additional gain of two and a zero ω_{z1} that tracks the output pole ω_{p1} at twice the frequency, i.e., $\omega_{z1} = 2\omega_{p1}$. The tracking zero ω_{z1} is

a result of the internal loop trying to prevent the output loop from reacting to load disturbances. Due to this tracking zero, the analog PSR enhancer with a dominant pole ω_{p2} can be stable across a wide range of load conditions. For example, when $R_{\rm load}$ or $C_{\rm load}$ increases, ω_{p1} moves to lower frequencies and approaches ω_{p2}. The effect of ω_{p1} alone would add $-90°$ phase lag within the frequency span from $0.1\omega_{p1}$ to $10\omega_{p1}$ and degrade the phase margin. Given $\omega_{z1} = 2\omega_{p1}$, the phase lag would only have a slight dip of $-18.4°$ at ω_{p1} and almost completely recover at $10\omega_{p1}$. Mismatch between $LG_{\rm int}$ and $LG_{\rm out}$ affects the zero frequency. For example, if there is 20% mismatch between $LG_{\rm INT}$ and $LG_{\rm OUT}$, the zero frequency can be either 1.8 or 2.2 times the output pole frequency. Since the zero still tracks the output pole within half a frequency decade, pole-zero cancellation is still effective to maintain stability. Careful design and layout are needed to limit the variation less than 20%. It is also noteworthy that the pole at V_1 has been neglected to simplify the analysis. In practice, this pole should be much higher than the dominant pole ω_{p2} at V_g to maintain good phase margin. Such condition is easily achievable since the loading capacitance at V_g due to $M_1[1:N]$ is much larger than that at V_1.

The PSR of the proposed LDO can also be derived by solving for $v_{\rm out}/vdd$ from (8)–(10)

$$\text{PSR} = \frac{1}{1+LG(s)}\left(g_{m1}+\frac{1}{r_{ds2}}-\frac{sC_{gs}g_{m1}r_{ea}}{1+s/\omega_{p2}}\right) \times\left(\frac{r_{\rm out}}{1+s/\omega_{p1}}\right). \tag{12}$$

It is worth noting that (12) looks like the PSR equation of a conventional analog LDO [17]. One difference is that r_{ds2} would be replaced with r_{ds1} for a conventional analog LDO. The second difference is in $LG(s)$, which has an extra gain of two and a tracking zero to help improve the PSR at low and high frequencies. For example, $LG(s)$ increases at frequencies beyond $\omega_{z1} = 2\omega_{p1}$, which improves PSR.

C. Effect of Nonlinear Loads

If the load is a current source, it can have a small dc resistance, $R_{\rm load}$, and a large ac resistance, $r_{\rm load}$. The third equality in (10) may not be satisfied because the output impedance becomes $r_{\rm out} = \frac{r_{\rm load}r_{ds2}}{r_{\rm load}+r_{ds2}}$. Larger $r_{\rm out}$ increases $LG_{\rm OUT}$ and pushes the tracking zero away from the output pole ω_{p1}. However, the effect is not significant since $r_{ds2} < R_{\rm load} < r_{\rm load}$. For example, if the LDO produces 0.8-V output from 1-V input, $R_{\rm load}$ would be $4r_{ds2}$. Even if $r_{\rm load}$ is infinite, $r_{\rm out}$ and $LG_{\rm OUT}$ would be increased by only 25%, and the tracking zero would be at 2.25 times the frequency of ω_{p1}.

D. Implementation and Simulation

The proposed analog-assisted digital CL-LDO is designed in a 130-nm CMOS process. The nominal operating voltage is 1 V, and the dropout voltage is 0.2 V. The switching threshold ΔV is set at 20 mV; thus, $V_{\rm ref}$= 800 mV, $V_{\rm low}$= 780 mV, and $V_{\rm high}$= 820 mV. The target range of load current is from 1to 50 mA, provided by 28 power switches, i.e., $N = 28$ in Fig. 2. The power switches are implemented by PMOS transistors with minimum channel length and divided into four groups, driven by four analog PSR enhancer modules. A PSR enhancer module is activated when its associated power switches are turned ON by the digital regulator. If the range of load current is extended, more power switches together with PSR enhancers can be added. By scaling the number of PSR enhancers with the number of power switches, we can keep ω_{p2} at a high frequency to maintain large gain-bandwidth product. Moreover, by activating the PSR enhancers accordingly to the load current, high current efficiency can be maintained at light loads. The static current consumption of the proposed LDO changes from 160 μA at the lightest load to 350 μA at the heaviest load. Fig. 6 shows the frequency response of the internal loop when the output loop is disabled by tying $V_{\rm out}$ to $V_{\rm ref}$. The internal loop is completely stable with a dominant pole at V_g, which is expected because $V_{\rm int}$ is only loaded by $R_{\rm int}$.

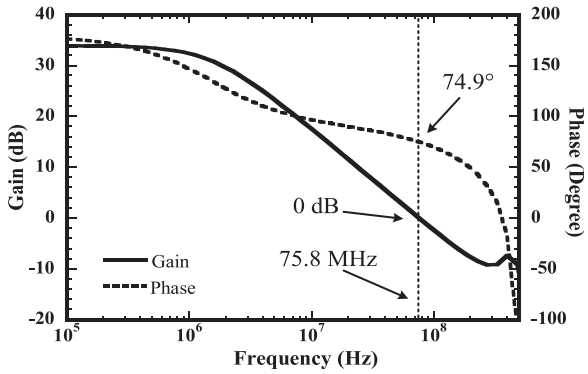

Fig. 6. Frequency response of the internal loop of the analog PSR enhancer when the output loop is disabled.

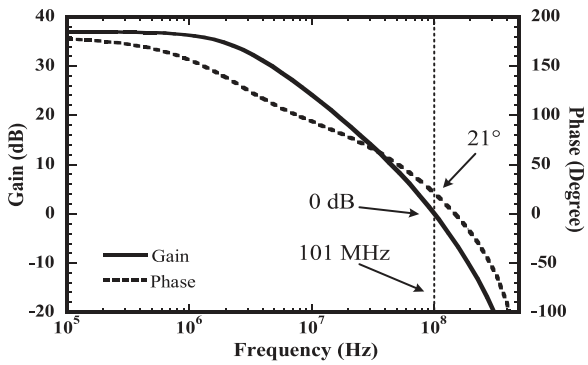

Fig. 7. Frequency response of the output loop of the analog PSR enhancer with $C_{\rm load}$ = 10 pF when the internal loop is disabled.

Figs. 7 and 8 show the frequency response of the output loop when the internal loop is disabled by tying $V_{\rm int}$ to $V_{\rm ref}$. This frequency response is equivalent to that of a conventional analog LDO. Due to the relatively high frequency of ω_{p2}, the phase margin is very small even when $C_{\rm load}$ = 10 pF in Fig. 7, and the output loop is unstable when $C_{\rm load}$ = 100 pF in Fig. 8.

Figs. 9–11 show the frequency response of the analog PSR enhancer with both the internal loop and the output loop enabled, for $C_{\rm load}$ = 10 pF, 100 pF, and 1 nF. The phase margin is higher

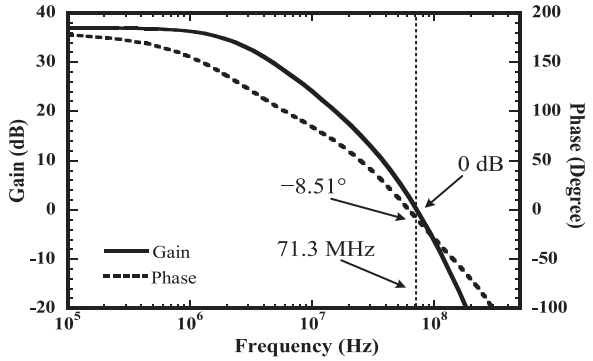

Fig. 8. Frequency response of the output loop of the analog PSR enhancer with $C_{\text{load}} = 100$ pF when the internal loop is disabled.

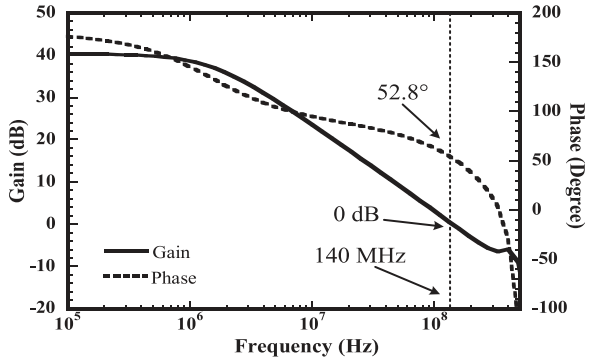

Fig. 9. Frequency response of the analog PSR enhancer with $C_{\text{load}} = 10$ pF when both internal loop and output loop are enabled.

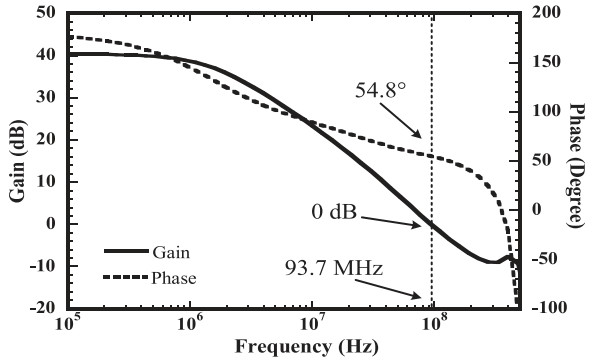

Fig. 10. Frequency response of the analog PSR enhancer with $C_{\text{load}} = 100$ pF when both internal loop and output loop are enabled.

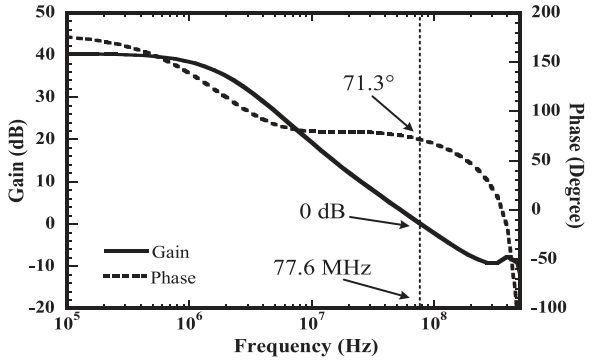

Fig. 11. Frequency response of the analog PSR enhancer with $C_{\text{load}} = 1$ nF when both internal loop and output loop are enabled.

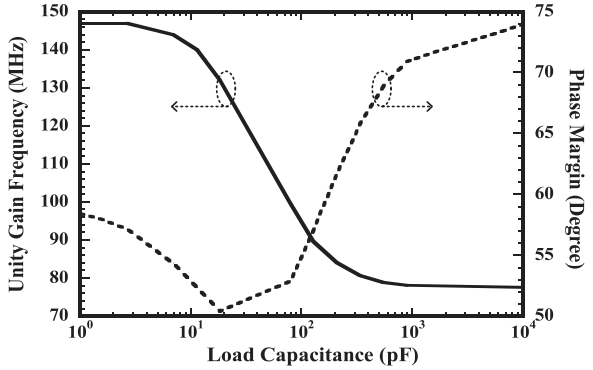

Fig. 12. Unity gain frequency and phase margin of the PSR enhancer when C_{load} varies from 1 pF to 10 nF, which demonstrates the stability of the proposed design across a wide range of capacitive loads.

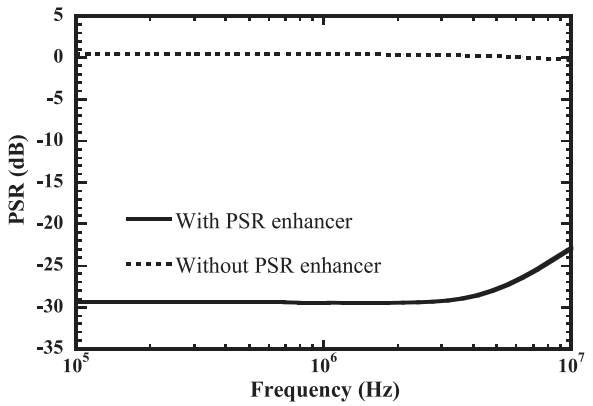

Fig. 13. Simulated PSR of the CL-LDO with and w/o PSR enhancer.

than 50°, which is sufficient to ensure the stability. Fig. 12 shows the simulated unity gain frequency and phase margin of the analog PSR enhancer when C_{load} varies. As C_{load} increases, the output pole ω_{p1} moves to lower frequencies and decreases the unity gain frequency. However, because the tracking zero ω_{z1} neutralizes the phase lag effect of ω_{p1}, the phase margin is maintained above 50°, and the analog PSR enhancer is always stable even when C_{load} varies from 1 pF to 10 nF. Fig. 13 shows the simulated PSR of the LDO. Without the analog PSR enhancer, supply noise is injected to the output through the turned-ON transistors in the array $M_2[1:N]$ without any suppression. The simulated PSR without the analog PSR enhancer is observed to be slightly higher than 0 dB. Transconductance g_{m2} of the turned-ON transistors $M_2[1:k]$ causes supply noise to be amplified slightly at the output. In the analysis above, g_{m2} is ignored since the effect of ON-resistance r_{ds2} is assumed dominant. The simulated PSR with proposed CL-LDO is close to –30 dB at low frequencies and better than –20 dB at 10 MHz.

III. Experimental Results

Fig. 14 shows a micrograph of the prototype chip fabricated in a 130-nm CMOS process, with an area of 0.0645 mm^2 excluding

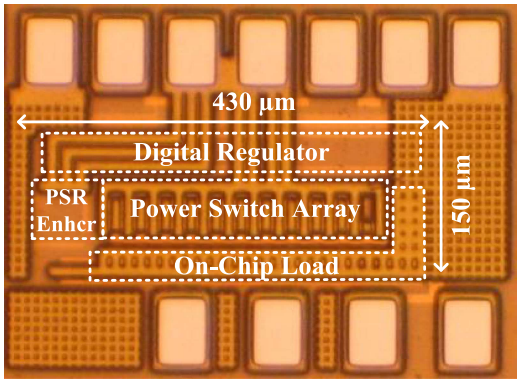

Fig. 14. Micrograph of the proposed CL-LDO prototype chip.

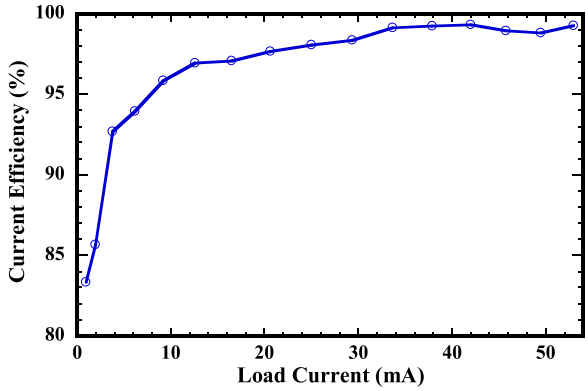

Fig. 15. Measured current efficiency of the CL-LDO prototype chip versus load current at $VDD = 1$ V and $V_{\mathrm{OUT}} = 0.8$ V.

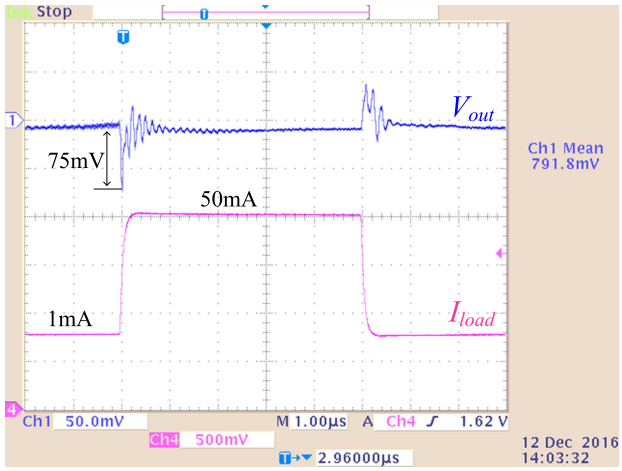

Fig. 16. Measured transient response of the CL-LDO prototype chip to a load step from 1 to 50 mA with $C_{\mathrm{load}} = 100$ pF (on-chip).

pads. On-chip load includes a 100-pF capacitor and a voltage-controlled current source. Fig. 15 shows the measured current efficiency, which is higher than 96% when the load current is above 10 mA and peaks at 99.3%.

Figs. 16 and 17 show the measured load response with $C_{\mathrm{load}} =$ 100 pF (on chip) and with an additional off-chip 10-nF capacitor, respectively, to demonstrate the capability to support a wide

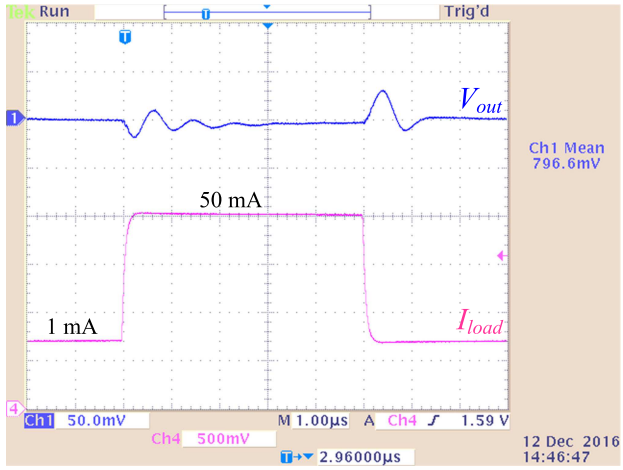

Fig. 17. Measured transient response of the CL-LDO prototype chip to a load step from 1 to 50 mA with $C_{\mathrm{load}} = 10$ nF (off-chip).

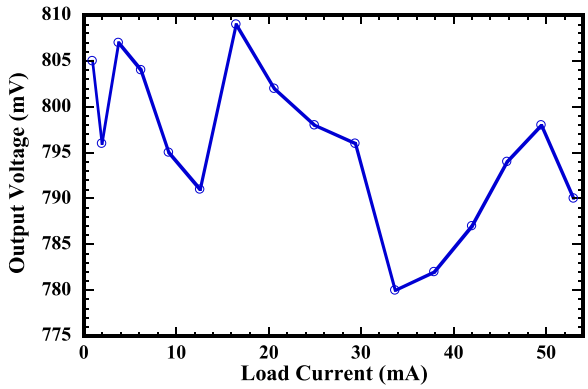

Fig. 18. Measured load regulation of the CL-LDO prototype chip.

range of load capacitance. The load current is stepped between 1 and 50 mA by controlling the on-chip voltage-controlled current source. The scope was set to dc coupling to capture the dc component of the output voltage. The scale was set to 50 mV/div to see the small voltage spikes. The offset of the scope was set to 800 mV so that the waveform could be displayed with the scale of 50 mV/div. The blue arrow with number 1 on the left of the figures indicates where the 800-mV level is for channel Ch1. In Fig. 16, the mean of the blue waveform (Ch1) is displayed as 791.8 mV on the right side. In Fig. 17, it is 796.6 mV. Voltage overshoots are caused by the response of the digital regulator as it tries to regulate V_{out} into the voltage window $[V_{\mathrm{low}}, V_{\mathrm{high}}]$. Fast transient response with low voltage overshoot is observed in both cases, which demonstrates a stable co-operation of the digital regulator and the analog PSR enhancer regardless of the output pole frequency. The transient response time is estimated to be 150 ps, based on the formula presented in [1]. The settling time is measured to be 3 μs. A faster digital regulator such as the one in [11] can be used to achieve much faster settling time, e.g., 60 ns [11]. Large C_{load} increases the setting time, but it reduces the voltage spikes caused by the digital regulator.

The measured load regulation and line regulation are shown in Figs. 18 and 19, respectively. Unlike conventional analog

TABLE I
COMPARISON WITH EXISTING LOW-VOLTAGE CAPACITORLESS LDOS

	TCAS-1 2015 [13]	TCAS-1 2015 [10]	TPE 2015 [21]	ESSCIRC 2016 [11]	ISSCC 2017 [22]	**This Work**
Process (nm)	65	40	130	130	65	**130**
LDO Type	Analog	Digital	Digital	Dig. + Analog	Dig. + Analog	**Dig. + Analog**
Input Voltage (V)	1.2	0.6	0.5 – 1.2	1.1 – 1.2	0.5 – 1	**1**
Output Voltage (V)	1	0.4	0.45 – 1.14	0.8 – 1.1	0.45 – 0.95	**0.8**
Max Load Current, I_{MAX} (mA)	10	200	4.6	12	12	**50**
Controller Current, I_Q (μA)	50 – 90	25.1	~751	163.2	> 3.2	**160 – 350**
Peak Current Efficiency (%)	n/a	99.99	98.3	98.64	n/a	**99.3**
|PSR| (dB) @ 10 MHz	< 20	16	16	12	n/a	**> 20**
ΔV (mV) @ Load Step (mA)	82 @ 10	n/a	40 @ 0.7	240 @ 10.3	105 @ 10	**75 @ 49**
Response Time, T_R (ns)*	1.15	n/a	0.22	18	> 0.862	**0.15**
Settling Time (ns)	> 100	n/a	400 - 1900	32	> 3000	**< 800**
Load Regulation (mV/mA)	1.1	0.07	< 10	< 2.67	n/a	**0.46**
Total On-chip Capacitor (nF)	0.14	None	n/a	0.5	0.1	**0.1**
Min/Max Load Capacitor (nF)	n/a	n/a	n/a	n/a	n/a	**0.001 – 10**
Active Area (mm^2)	0.023	0.0375	0.114	0.0818	0.0338	**0.0645**
FOM1 (%)	n/a	n/a	90.8	n/a	n/a	**96.7**
FOM2 (ps)	5.74	n/a	36**	244.8	0.23	**0.48 – 1.05**

FOM1 (Efficiency Metric) = Average current efficiency across a 50x current dynamic range. [21]
* $T_R = C_{out} \times \Delta V / I_{MAX}$ [1]; FOM2 (Performance Metric) = $T_R \times I_Q / I_{MAX}$ [1]; ** Process normalized value [21].

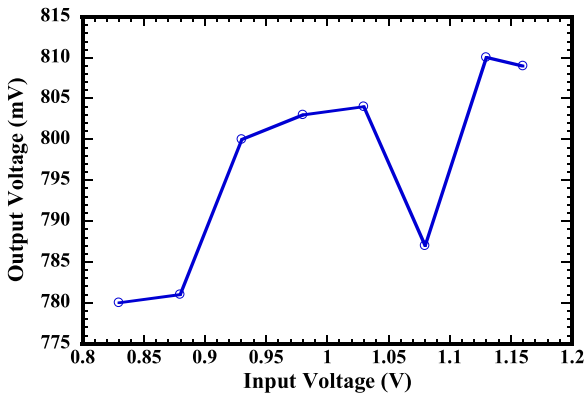

Fig. 19. Measured line regulation of the CL-LDO prototype chip.

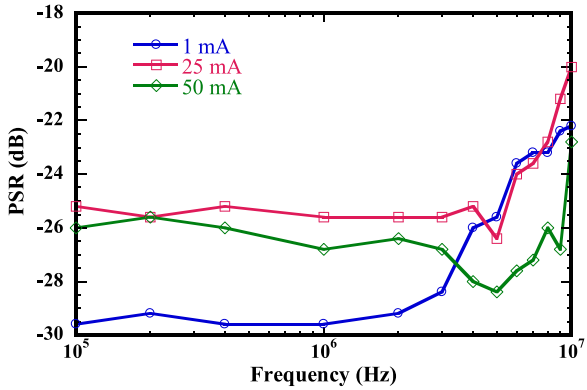

Fig. 20. Measured PSR of the CL-LDO prototype chip at three different load currents with on-chip C_{load} = 100 pF.

LDOs, the proposed design does not exhibit a gradual $V_{\rm out}$ variation when the $R_{\rm load}$ or VDD changes. Under the control of the digital regulator, $V_{\rm out}$ can settle to any values within the voltage window $[V_{\rm low}, V_{\rm high}]$, which is ±20 mV of $V_{\rm ref}$. This explains the random patterns of $V_{\rm out}$ observed in Figs. 18 and 19. We define that $V_{\rm out}$ is correctly regulated when it is between $V_{\rm low}$ and $V_{\rm high}$. The load regulation and line regulation could be improved by using a tighter voltage window $[V_{\rm low}, V_{\rm high}]$, which would require faster comparators with higher sensitivity.

Fig. 20 shows the measured PSR at three different load currents, i.e., 1, 25, and 50 mA, with $C_{\rm load}$ = 100 pF. The PSR is observed to be better than −20 dB for frequencies up to 10 MHz. Table I summarizes the performance of the proposed analog-assisted digital CL-LDO in comparison with existing low-voltage CL-LDOs, including digital type, analog type, and hybrids. The proposed design has the best PSR at 10 MHz among digital LDOs with or without analog assistance, and superior average current efficiency (FOM1) of 96.7% across a 50x load range. Simulation and measurement both demonstrate the ability to support a very wide range (up to four decades) of load capacitance. Theoretically, the range of load capacitance is only limited by the stability of the digital regulator, and according to simulation, the proposed design is still stable at $C_{\rm load}$ = 1 μF, which is beyond any practical load conditions of a CL-LDO. Compared to the hybrid CL-LDO in [11], which uses the same process node, the analog part of the proposed design can operate at a lower supply voltage while delivering much better PSR over a larger frequency range. It is also noteworthy that the proposed design is 5.3 times smaller in area per load current than the design in [9].

IV. CONCLUSION

In this paper, an analog-assisted digital CL-LDO was presented with the capability to operate at low voltage, deliver good PSR for frequencies up to 10 MHz, and maintain robust stability across an extremely large range of load conditions. Such performance is achieved by separating load regulation and PSR

function into digital control and analog control, respectively. The analog control does not respond to load changes, and thus the load-dependent output pole does not cause instability issue. This characteristic enables the design of an analog feedback loop with large GBW to improve PSR at high frequencies. Load regulation is performed by an asynchronous digital feedback controller for fast response to load changes. The combination of digital control and analog control enables good PSR at high frequencies over a wide range of load conditions.

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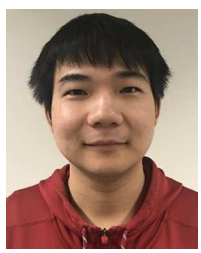
Nghia Tang (S'10–M'18) received the B.S. and Ph.D. degrees in electrical engineering from Washington State University, Pullman, WA, USA, in 2009 and 2016, respectively. His doctoral research primarily focuses on power management integrated circuits.

He has been involved in the design of envelope tracking supply modulators for power amplifiers, fully integrated voltage regulators, and energy harvesting systems. He has served as an IC design Intern at several companies, including Tagore Technology, Silicon Labs, and Texas Instruments.

Yangyang Tang (S'12–M'15) received the M.S. degree in research of I-MARS, and the Ph. D. degree in electronics and information engineering from the Université de Bretagne Sud, Lorient, France, in 2009 and 2013, respectively.

He was a Visiting Scholar from June 2011 to June 2012 with the Low-Energy/Fault-Tolerant Systems Laboratory, Utah State University, Logan, Utah. His previous research interests include error-correction circuit design and fault-tolerant featured hardware architecture for contemporary digital logic or nanoelectronics. In July 2013, he joined the Research Department of HiSilicon, Huawei, as a Senior Research Engineer. He has authored and coauthored more than ten technical papers, has more than ten issued and ten pending patents. His current research interests include low power circuit design, dc–dc converter, LDO, and ultralow power circuit design.

Dr. Tang is the recipient of HiSilicon President's Award in 2015 and the Award of Outstanding Project Manager by 2012-Lab Huawei in 2017.



Zhiyuan Zhou (S'17) received the M.S. degree in electrical engineering from the University of Texas at Dallas, Richardson, TX, USA, in 2013. He is currently working toward the Ph.D. degree in electrical engineering with Washington State University, Pullman, WA, USA.

His research interests include on-chip power management system and energy-harvesting system for Internet of Things devices.

Bai Nguyen (S'15) received the B.S. degree in electronics and telecommunication from Vietnam National University, Hanoi, Vietnam, in 2005, and the M.S. degree in electrical and computer engineering from Chungbuk National University, Cheongju, South Korea, in 2008. Since 2013, he has been working toward the Ph.D. degree in electrical engineering with Washington State University, Pullman, WA, USA.

He was a Research Assistant with the Institute of Material Science, Vietnam Academy of Science and Technology, a Design Engineer with Emerson Network Power, a Hardware Manager with Innova Electronics, and a Senior Researcher with Viettel R&D Institute, Viettel Group. His research interests include analog integrated circuit design for power conversion and management, emphasizing on high-efficiency switching regulator, fully integrated dc–dc converter, wireless power transfer, and energy harvesting.

Wookpyo Hong (S'15) received the B.S. degree in electrical and computer engineering from Chungbuk National University, Cheongju, South Korea, in 2006. He is currently working toward the Ph.D. degree in electrical engineering with Washington State University, Pullman, WA, USA.

His current research interests include power management circuits, emphasizing on fully integrated voltage regulators, single-input multiple-output voltage regulators, energy harvesting systems, and sensor networks.

Philipp Zhang (Chen-Xiong Zhang) (M'86) received the Ph.D. degree in electrical engineering from the University of Karlsruhe (now Karlsruhe Institute of Technology, KIT), Karlsruhe, Germany, in 1990.

In 1983, he joined the Institute for Theoretical Electrical Engineering, University of Karlsruhe, where he was involved in teaching and research activities in VLSI layout and circuit design. From 1991 to 1995, he was with SIEMENS Microelectronic Center, Hamburg, Germany, where he was involved in research and development of ATM broadband networks and ASIC design for telecom application. He was involved in the R&D of Advanced Communication technologies in Europe (RACE) project. In 1995, he transferred to Interphase Corp., Dallas, TX, USA, and was in charge of development of communication chipsets and systems. Since then he has worked in a couple of start-up companies as CEO/CTO in the U.S. and in China in the area wireless and broadband communications. He joined Huawei Technologies as a Chief Scientist in 2005 and is currently in charge of corporate research programs and projects.

Jong-Hoon Kim received the Ph.D. degree in biomechatronics engineering from Sungkyunkwan University, Seoul, South Korea, in 1997.

He is currently a Principle Researcher of smart distribution systems with the Korea Food Research Institute, Sungnam, South Korea.

Deukhyoun Heo (S'97–M'00–SM'13) received the B.S.E.E. degree in electrical engineering from Kyoungpuk National University, Daegu, South Korea, in 1989, the M.S.E.E degree in electrical engineering from Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 1997, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2000.

In 2000, he joined the National Semiconductor Corporation, where he was a Senior Design Engineer involved in the development of silicon RFICs for cellular applications. Since 2015, he has been a Professor with the Department of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA. His primary research interests include RF/microwave/opto transceiver design based on CMOS, SiGe BiCMOS, and GaAs technologies for wireless and wireline data communications, batteryless wireless sensors and intelligent power management systems for sustainable energy sources, adaptive beam former for phased-array communications, low-power high date-rate wireless links for biomedical applications, and multilayer module development for system-in-package solutions.

Dr. Heo has been a member of the Technical Program Committee of IEEE Microwave Theory and Techniques Society (IEEE MTTS-S) International Microwave Symposium (IMS) and the International Symposium of Circuit and Systems (ISCAS). He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS— PART II: EXPRESS BRIEFS (2007–2009) and has served as an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He has been the recipient of the 2009 National Science Foundation CAREER Award.