High-Efficiency Fully Integrated Switched-Capacitor Voltage Regulator for Battery-Connected Applications in Low-Breakdown Process Technologies

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***Abstract*—Conventional implementations of fully integrated, battery-connected, switched-capacitor voltage regulators (SCVRs) require either thick-oxide MOSFETs or stacked thin-oxide MOSFETs as power switches to sustain the voltage stress induced by a nominal 3.7-V Li-ion battery voltage. These approaches, however, exacerbate power loss, thus unable to achieve good power efficiency. Therefore, this paper proposes a solution to overcome the breakdown issue while improving the power efficiency by using only nonstacked, thin-oxide MOSFETs. This is realized by using a three-state, low-voltage-stress SCVR with a cross-phase-switching technique to decrease the output impedance and increase the total equivalent capacitance in a multiphase configuration. A prototype 3:1 SCVR is implemented fully on-chip in a standard 130-nm CMOS process. The chip is capable of delivering a maximum load current of 45 mA with an input voltage range from 3.2 to 4 V. Measurement results show 78–80% efficiency over a range of output power 4–28 mW, and a power density up to 38 mW/nF. The measured output ripple is 30–50 mV over a load range of 11–45 mA, and the measured voltage droop is 69 mV with 200-ns settling time under a 13-mA load step.**

***Index Terms*—Battery connected, cross phase switching (CPS), fully integrated voltage regulator (FIVR), low voltage stress (LVS), switched-capacitor voltage regulator (SCVRs).**

I. Introduction

RECENTLY emerging wearable electronics [1], such as smartwatches, health monitoring straps, wireless earbuds, etc., as well as future low-profile devices, like miniature spy robots or drones [2], have imposed a strict constraint on the available space for electronic circuit hardware. Naturally, the best approach to tackle this issue is to utilize fully integrated solutions and advanced process technologies featuring thin-oxide short-channel-length devices. However, the low-breakdown voltage of thin-oxide devices requires dedicated system design to optimize performance and ensure reliability. For example, Li-ion batteries are the most popular choice for wearable electronics thanks to their superior power density, but their voltage range of 2.9–4.2 V largely exceeds the breakdown voltage of approximately 1 V of thin-oxide devices in modern processors and system on chips (SoCs) [3]. Conventionally, an off-chip dc–dc converter is implemented to step down the battery voltage, but this arrangement is not area efficient for the above-mentioned applications [3]. As a result, the motivations for efficient, fully integrated voltage regulators (FIVRs) directly tied to the battery electrodes have become apparent. Although on-chip linear regulators have been popularly employed as power supply for processor cores, achieving high efficiency requires the use of switching converters when the dropout voltage is large [4]. Compared with inductor-based converters [5]–[11], switched-capacitor voltage regulators (SCVRs) [4], [12], [13] have been widely considered as an attractive choice for fully on-chip implementation because integrated capacitors can achieve low series resistance without additional fabrication steps while standard on-die inductors suffer from high series resistance (hence big conduction loss) [4]. On the other hand, some existing SCVRs report efficiency values above 80% [4], [13], but they support input voltages around 1–2 V only. The design presented in [14] could accept 3.7-V battery voltage, but it only provides a single 2:1 conversion ratio, which is inefficient to provide supply voltages around 1 V or lower for modern processors and SoCs. Likewise, the resonant SCVR presented in [15] is only efficient at 2:1 ratio because its efficiency drops below 73% at conversion ratio of 3.7–1.2 V. To provide a wide range of conversion ratio, an inductor has been used together with switched capacitors operating under a soft-charging mechanism presented in [16]. Although this structure has been designed for battery input voltage by employing stacked MOSFETs, it is implemented with a number of off-chip passive components that occupy large space. In [17], a

Manuscript received April 6, 2017; revised July 30, 2017; accepted September 12, 2017. Date of publication September 28, 2017; date of current version April 20, 2018. This work was supported in part by the U.S. National Science Foundation under Grant CNS-1705026 and Grant CNS-1564014, in part by the Joint Center for Aerospace Technology Innovation, and in part by the NSF Center for Design of Analog–Digital Integrated Circuits. Recommended for publication by Associate Editor J. Stauth. *(Corresponding author: Deukhyoun Heo.)*

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Digital Object Identifier 10.1109/TPEL.2017.2757950

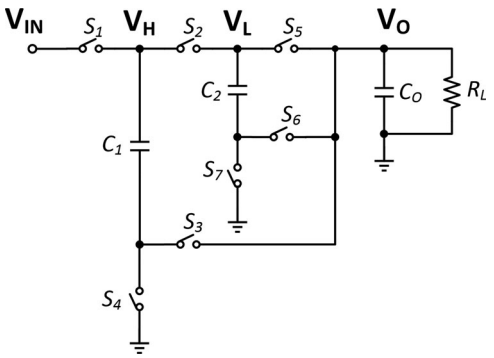


Fig. 1. Core power stage of the proposed LVS SCVR.

high-efficiency integrated multiphase-soft-charging (MSC) converter without any off-chip components has been presented. However, the input voltage of this SCVR is limited at 3.2 V only, significantly below the 3.7-V target. Additionally, the MSC technique requires many switches conducting in series at small duty cycles, thus increasing conduction loss.

If an SCVR produces 1 V from a 3.7-V battery voltage, the drain–source voltage across some turn-off MOSFETs could be as high as $(3.7\,\mathrm{V}\text{ - }1\,\mathrm{V}) = 2.7\,\mathrm{V}$, far beyond the breakdown voltage at around 1 V of modern technologies [18]. Several solutions have been proposed, but they tend to have poor power efficiency [3], [18], [19]. For example, a 4:1 SCVR presented in [19] makes use of thick-oxide MOSFETs in a two-stage cascade SCVR, achieving 70% peak efficiency. The converter proposed in [18] uses an low dropout (LDO) in series with an SCVR and achieves peak efficiency of 60%. The reconfigurable dual-ratio fully integrated SCVR presented in [3] employs stacks of power MOSFETs to withstand high voltages and achieves 73–74.3% efficiency, which could be considered as the state of the art for battery-connected FIVRs. Staking MOSFETs, however, still hinders the effort to further improve efficiency due to the extra power loss from using a larger number of switching devices.

This paper hence presents a structure named the low-voltage-stress (LVS) SCVR to implement a 3:1 fully integrated SCVR that overcomes the drawbacks mentioned above while using only nonstacked thin-oxide MOSFETs. The key ideas of the design are subsequently disclosed in Section II, including the LVS operation to mitigate voltage stresses, a cross-phase-switching (CPS) technique to further improve power density and efficiency. In Section II, practical implementation of the chip fabricated in a standard 130-nm CMOS process is also given in. Measurement results are summarized in Section III, and conclusions are finally discussed in Section IV.

II. Proposed SCVR With LVS Topology and CPS Technique

A. Proposed LVS Topology

A basic structure of the power stage in the proposed LVS SCVR is illustrated in Fig. 1. This cell consists of two flying capacitors C_1 and C_2, seven power switches $S_1 - S_7$, and an output decoupling capacitor C_O. The operation of this

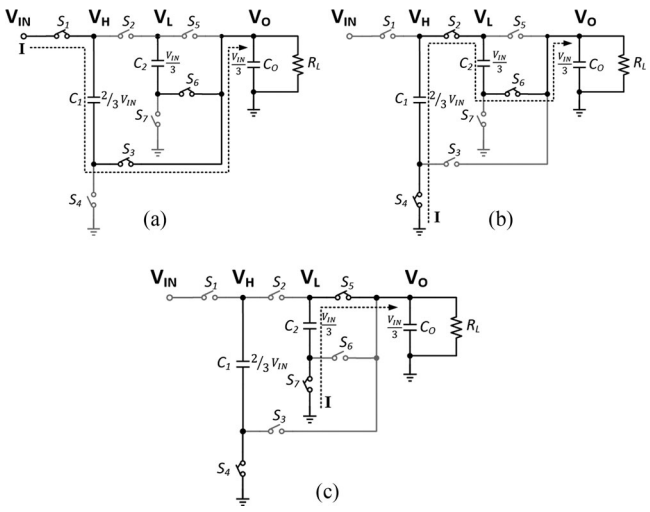


Fig. 2. Operating states of the SCVR with LVS scheme: (a) state 1; (b) state 2; and (c) state 3.

architecture is elaborated through three periodic states 1–3 in Fig. 2 and will be explained in details.

For convenience, the current flow is represented by a dotted arrow at each state, turn-on switches are black, and turn-off switches are grayed out in Fig. 2. At first, let consider a no-load, steady state when all the capacitor voltages remain constant throughout three states. If the voltages of C_1 and C_2 are settled to V_1 and V_2, respectively, the following three equations corresponding to three states need to be met:

$$V_{\mathrm{IN}} = V_1 + V_O \tag{1}$$

$$V_1 = V_2 + V_O \tag{2}$$

$$V_2 = V_O\,. \tag{3}$$

The solution for this set of equations is straightforward, resulting in $V_1 = 2/3V_{\mathrm{IN}}$, $V_2 = V_{\mathrm{IN}}/3$, and $V_O = V_{\mathrm{IN}}/3$. In fact, these voltages alter from state to state by a certain amount of ripple about their dc values in the presence of an output load. Nevertheless, with a proper choice of the capacitor sizes, the ripple voltages could be ignored with respect to their dc levels.

This three-state switching scheme hence always keeps voltage stresses across the switches around $V_{\mathrm{IN}}/3$. Starting with state 1, C_1 is charged through S_1 and S_3 to deliver a current flow to R_L. At the same time, the bottom plate of C_2 is tied to V_O through S_6 while its top plate is floating to set V_L to $2/3V_{\mathrm{IN}}$. This voltage at V_L ensures voltage stress on S_2 and S_5 to be kept at $V_{\mathrm{IN}}/3$. On the other hand, voltage stresses on S_4 and S_7 are also $V_{\mathrm{IN}}/3$. During this state, the current flow charges up C_1 while C_2 just holds any charges it previously stored.

Once the SCVR turns to state 2, C_1 is discharged and C_2 is charged through S_4, S_2, S_6, and $R_L \,//\, C_O$, while the voltage stress across S_1, S_3, S_5, and S_7 equal to $V_{\mathrm{IN}}/3$. Eventually, the SCVR accomplishes a switching period at state 3, in which C_2 is discharged through S_7, S_5, and $R_L \,//\, C_O$ while C_1 holds its charges with the bottom plate grounded and the top plate opened to keep V_H at $2/3V_{\mathrm{IN}}$. Once again, this arrangement simply sets the same voltage stress $V_{\mathrm{IN}}/3$ across turn-off switches S_1, S_2,

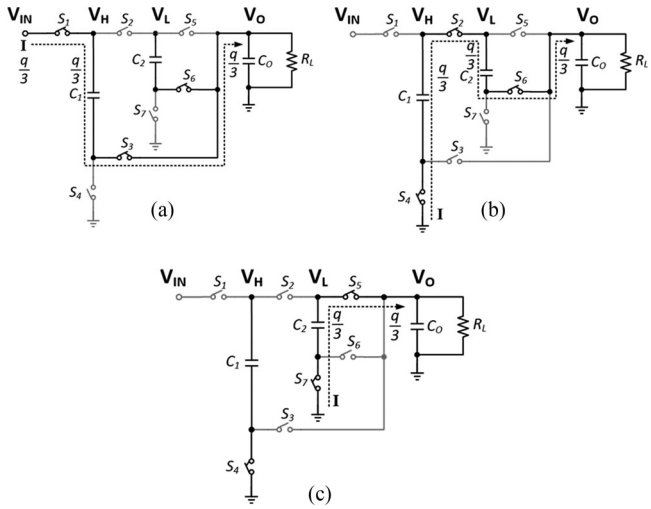


Fig. 3. Normalized charge flows in the LVS structure at different states: (a) state 1; (b) state 2; and (c) state 3.

S_3, and S_6. When working at 3.7 V input voltage, ideally, this SCVR produces 3.7/3 V = 1.23 V output voltage. Likewise, voltage stress across any power switch is also 1.23 V, which is only half of the stress (3.7 − 1.23) V = 2.47 V that would be generated in conventional SCVRs [18]. Although a high voltage is at $2/3V_{\rm IN}$ is seen across C_1, on-chip capacitors with high voltage ratings are widely available in recent fabrication processes. For example, MIM capacitors that are used as flying capacitors in this proposed design feature 6.8-V rating, thus eliminating the concern about voltage stress on C_1. Another benefit of this structure is that it also halves drain–source voltage swings of MOSFETs utilized to implement these switches, thus reducing switching loss.

The above-mentioned voltage stress is under no-load conditions. When a load current is drawn from V_O, this voltage drops under the effect of output impedance, in the same manner as any other SCVR. In this case, $(V_{\rm IN} - 2V_O)$ is seen across S_2 while V_O is seen across all other switches. In order to diminish the influence of load current on V_O, flying capacitances and switching frequency should be large enough to minimize the output impedance, which will be addressed in the following sections.

B. Slow-Switching Limited (SSL) Output Impedance of the LVS Structure

In order to get more insights into the merits of the proposed LVS structure, it is instructive to analyze the output impedance of this SCVR. First, the method using charge multiplier vectors presented in [12] and [20] to calculate the SSL impedance can be adopted with some modifications for three-state operation. Using the KCL constraints and the constraint of steady state dictating that the incoming and outgoing charges through each flying capacitor should be equal in one period, the charge flows through capacitors and voltage sources normalized with respect to the output charge flow can be found in Fig. 3. The charge multiplier vectors are thus determined as

$$a\,(1) = [a_O\,(1)\,a_{C_1}\,(1)\,a_{C2}\,(1)\,a_{\rm IN}\,(1)]^T = [1/3\,1/3\,0\,-1/3]^T \tag{4}$$

$$a\,(2) = [a_O(2)\,a_{C_1}(2)\,a_{C2}(2)\,a_{\rm IN}(2)]^T = [1/3\;-1/3\,1/3\,0]^T \tag{5}$$

$$a\,(3) = [a_O(3)\,a_{C_1}(3)\,a_{C2}(3)\,a_{\rm IN}(3)]^T = [1/3\;0\;-1/3\;0]^T \tag{6}$$

where $a(i)$ is the charge multiplier vector at state i, with $i = 1, 2, 3$. Vector $a(i)$ is partitioned into output, capacitors, and input components: $a_O(i)$, $a_{Cj}(i)$, and $a_{\rm IN}(i)$, respectively. It is noteworthy that charge flows shown in Fig. 3 are found by equations of charge conservative law (equivalent to KCL), thus independent of C_1 and C_2 capacitances [12]. Values of C_1 and C_2 only affects the voltage ripples on these capacitors.

The SSL output impedance is thus obtained by the following equation, as mentioned in [20]:

$$R_{\rm LVS,SSL} = \frac{1}{2f_{\rm SW}} \sum_i \sum_j \frac{a_{Cj}(i)^2}{C_j}. \tag{7}$$

Plugging the values of $a_{Cj}(i)$ from (4)–(6) into (7), the output impedance is determined as

$$R_{\rm LVS,SSL} = \frac{1}{9}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) f_{\rm SW}^{-1}. \tag{8}$$

Given a total flying capacitance budget $C_{F,\,\rm TOT} = (C_1 + C_2)$, the optimum design is achieved when the output impedance is minimized [12], [20]

$$R^*_{\rm LVS,SSL} = \min(R_{\rm LVS,SSL}) = \frac{4}{9}\frac{1}{C_{F,\rm TOT} f_{\rm SW}},$$
$$\text{when } C_1 = C_2 = \frac{C_{F,\rm TOT}}{2}. \tag{9}$$

C. Fast-Switching Limited (FSL) Output Impedance, Total Output Impedance, and Power Loss Analysis

Unlike SSL impedance, which is established for SCVRs with ideal switches [12], FSL output impedance is otherwise used in the case when the *RC* constant of flying capacitance and the switch resistance are very large as compared with the conduction cycle of these switches [12]. In this asymptotic limit, the switch charge flow multiplier vectors [12], [20] are found based on the charge flows shown in Fig. 3

$$a_r\,(1) = [a_{r1}(1)\,a_{r2}(1)\,a_{r3}(1)\,a_{r4}(1)\,a_{r5}(1)\,a_{r6}(1)\,a_{r7}(1)]^T$$
$$= [1/3\;0\;1/3\;0\;0\;0\;0]^T \tag{10}$$

$$a_r\,(2) = [a_{r1}(2)\,a_{r2}(2)\,a_{r3}(2)\,a_{r4}(2)\,a_{r5}(2)\,a_{r6}(2)\,a_{r7}(2)]^T$$
$$= [0\;1/3\;0\;1/3\;0\;1/3\;0]^T \tag{11}$$

$$a_r\,(3) = [a_{r1}(3)\,a_{r2}(3)\,a_{r3}(3)\,a_{r4}(3)\,a_{r5}(3)\,a_{r6}(3)\,a_{r7}(3)]^T$$
$$= [0\;0\;0\;0\;1/3\;0\;1/3]^T \tag{12}$$

where $a_r(i)$ is the switch-resistance charge-multiplier vector at state i, with $i = 1, 2, 3$. Each component of $a_r(i)$, namely

$a_{rj}(i)$, is the normalized charge flow through switch S_j at state i.

As pointed out in [20], the FSL output impedance is determined from these vectors

$$R_{\mathrm{LVS,FSL}} = \sum_i \sum_j \frac{R_{\mathrm{on},j}}{D(i)} a_{rj}^2(i) = \frac{1}{D_{\mathrm{st}}} \sum_j R_{\mathrm{on},j} \sum_i a_{rj}^2(i)$$
$$= \frac{1}{D_{\mathrm{st}}} \sum_j R_{\mathrm{on},j} a_{rj,\mathrm{RSS}}^2 \tag{13}$$

where state duty cycle $D(i)$ is the ratio of the time duration of state i per the switching period. Assume $D(i) = D_{\mathrm{st}}$ is constant for all states ($D_{\mathrm{st}} = 1/3$ in a three-state structure) and $a_{rj,\mathrm{RSS}} = \sqrt{\sum_i a_{rj}^2(i)}$ is the root-sum-squared (RSS) value of the switch charge vector's components corresponding to S_j. According to Seeman and Sanders [12], the optimized FSL impedance is

$$R_{\mathrm{LVS,FSL}}^* = \frac{1}{D_{\mathrm{st}} G_{\mathrm{tot}}} \left(\sum_j a_{rj,\mathrm{RSS}} \right)^2 = \frac{3}{G_{\mathrm{tot}}} \left(\frac{7}{3} \right)^2$$
$$= \frac{49}{3G_{\mathrm{tot}}} = \frac{16.33}{G_{\mathrm{tot}}} \tag{14}$$

where G_{tot} is the total switch conductance. The approximated total output impedance, suggested in [20], is hence

$$R_{\mathrm{LVS,tot}} = \sqrt{{R_{\mathrm{LVS,SSL}}^*}^2 + {R_{\mathrm{LVS,FSL}}^*}^2}. \tag{15}$$

The power loss of the converter, including switching loss, flying capacitors' bottom plate loss, capacitor charge sharing loss, and conduction loss, is calculated by the following equation:

$$P_{\mathrm{LOSS}} = P_{\mathrm{SW}} + P_{\mathrm{BOT}} + R_{\mathrm{LVS,tot}} I_O^2$$
$$= f_{\mathrm{SW}} \sum_{j=1}^{7} C_{\mathrm{GS}j} V_{\mathrm{GS}j}^2 + f_{\mathrm{SW}} \sum_{j=1}^{2} C_{\mathrm{BOT}j} V_{\mathrm{BOT}j}^2$$
$$+ I_O^2 \sqrt{{R_{\mathrm{LVS,SSL}}^*}^2 + {R_{\mathrm{LVS,FSL}}^*}^2} \tag{16}$$

where P_{LOSS}, P_{SW}, and P_{BOT} are total power loss, switching loss, and bottom plate loss, respectively, while conduction loss (proportional to FSL impedance [12], [20]) and capacitor charge sharing loss (proportional to SSL impedance [12], [20]) are combined in $R_{\mathrm{LVS,tot}} I_O^2$; $C_{\mathrm{GS}j}$ and $V_{\mathrm{GS}j}$ are gate capacitance and voltage swing of switch S_j, respectively; and $C_{\mathrm{BOT}j}$ and $V_{\mathrm{BOT}j}$ are parasitic capacitance and voltage swing at bottom plate of flying capacitor C_j, respectively. There is a tradeoff between conduction loss and switching loss because a wider MOSFET helps reduce R_{on} but it increases C_{GS}. Power loss is then minimized at optimum sizes of switches [12], [20].

D. Comparative Study Between the Proposed LVS and Other Topologies

This section compares the proposed LVS structure and other topologies in terms of both output voltage ripple and power loss. In particular, flying-capacitor multilevel (FCML) [21] converter regular Dickson topology [17], [22] will be compared with the proposed LVS in details to understand merits and drawbacks of this structure. This discussion only considers single-phase configuration. Comparison of multiphase implementations will be addressed in the next section.

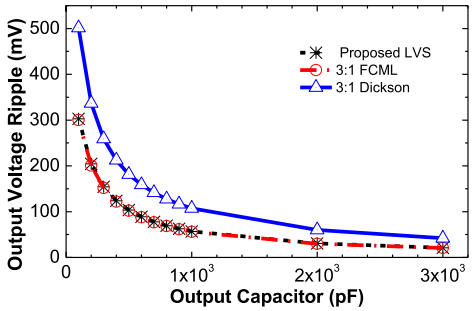


Fig. 4. Comparison of output ripple with $C_1 = C_2 = 360$ pF, $f_{\mathrm{SW}} = 100$ MHz, and $I_O = 30$ mA among different topologies.

At switching state i, the total current delivered by all flying capacitors to V_O, denoted by $I_O(i)$, is defined by

$$I_O(i) = \frac{q_O(i)}{\Delta t(i)} = \frac{a_O(i) q_O}{D_{\mathrm{st}} T_{\mathrm{SW}}} = \frac{a_O(i)}{D_{\mathrm{st}}} \left(\frac{q_O}{T_{\mathrm{SW}}} \right) = \frac{a_O(i)}{D_{\mathrm{st}}} I_{O,\mathrm{MEAN}} \tag{17}$$

where $q_o(i)$ stands for the total charges delivered by flying capacitors to V_O during state i, $\Delta t(i)$ is the time interval of state i, T_{SW} is the switching period, $q_O = \sum q_O(i)$ is the total charge flow to V_O in one period T_{SW}, and $I_{O,\mathrm{MEAN}} = q_O / T_{\mathrm{SW}}$ is the average output load current. Mismatch between $I_O(i)$ and $I_{O,\mathrm{MEAN}}$ results in ripple current that flows through C_O and creates voltage ripple at V_O. Based on this observation, a concept of output ripple current is defined in percentage to represent mismatch among state currents $I_O(i)$

$$\%I_{O,\mathrm{RIPPLE}} = \frac{\max(I_O(i)) - \min(I_O(i))}{I_{O,\mathrm{MEAN}}} \times 100\%$$
$$= \frac{\max(a_O(i)) - \min(a_O(i))}{D_{\mathrm{st}}} \times 100\%. \tag{18}$$

In the proposed LVS and previous FCML structures, $\%I_{O,\mathrm{RIPPLE}} = 0\%$ since $a_O(i) = 1/3$ at any state. In the regular Dickson topology, $\%I_{O,\mathrm{RIPPLE}} = 66.67\%$ as the charge flow to V_O at one state is twice that at the other state. Therefore, the regular Dickson topology has higher output voltage ripple in comparison with the proposed LVS and previous FCML structures. This effect is verified by simulation in Fig. 4, where the output voltage ripple of regular Dickson circuit is from 1.6 to 2 times as high as those of LVS and FCML. Besides the ripple induced by mismatch of $I_O(i)$, there is also ripple of V_O caused by the voltage variation of flying capacitors, the total ripple is hence not zero when $\%I_{O,\mathrm{RIPPLE}} = 0$. However, the ripple of V_O is greatly reduced by eliminating the mismatch between state currents $I_O(i)$.

On the other hand, compared with the proposed LVS, the FCML has worse FSL output impedance since its current needs to flow through more switches, thus producing more conduction loss. A qualitative comparison of FSL impedances among LVS, FCML, regular Dickson, as well as other topologies is

TABLE I
THEORETICAL COMPARISON BETWEEN THE PROPOSED LVD AND OTHER SINGLE-PHASE TOPOLOGIES

	The Proposed 3:1 LVS	3:1 Regular Dickson Topology [17], [22]	3:1 FCML Topology [21]	3:1 Series–Parallel Topology [4]	3:1 Ladder Topology [12]
FSL impedance [a]	$16.33/G_{\rm tot}$	$14.22/G_{\rm tot}$	$17.49/G_{\rm tot}$	$18/G_{\rm tot}$	$18/G_{\rm tot}$
SSL impedance	$\frac{4}{9}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{4}{9}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{4}{9}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{4}{9}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{2}{C_{F,\rm TOT}f_{\rm SW}}$
% Output current ripple	0%	66.67%	0%	66.67%	66.67%
# power MOSFETs [a]	7	8	6	9	6
Stacked MOSFETs	No	Yes [b]	No	Yes	No

[a]Given that any switch seeing $2V_{\rm IN}/3$ voltage stress is implemented with two stacked MOSFETs.
[b]Each pair of interstage switches presented in [17] is a form of stacked MOSFETs.

presented in Table I, by assuming the use of two stacked MOSFETs to withstand $2V_{\rm IN}/3$ stress occurring across a switch. As seen in Table I, regular Dickson converter exhibits the smallest FSL impedance even though it requires more power MOSFETs with the stacking method. This can be explained by (14): $D_{\rm st}$ of regular Dickson is 50% for a two-state switching scheme, larger than $D_{\rm st} = 33.33\%$ of the three-state LVS and FCML, thus resulting in a smaller FSL impedance even though it has a bigger sum of $a_{rj,\rm RSS}$. Therefore, FSL impedance of LVS lies between those of FCML and regular Dickson. Apart from this, all these three structures give the same SSL impedance because of the same charge flow patterns through flying capacitors. In summary, the proposed LVS topology can be considered as a balance design between output voltage ripple and FSL impedance since it has a smaller FSL impedance than that of FCML while offering lower output voltage ripple as compared with regular Dickson.

Parameters of some other topologies are also given in Table I, the ladder topology [12] exhibits both the highest SSL and FSL output impedances, so it is definitely less efficient. Although the series–parallel topology [4] has the same SSL output impedance as the LVS topology does, it needs two pairs of stacked MOSFETs [18] to comply with $2V_{\rm IN}/3$ stress, so that its FSL impedance is higher than that of LVS. Moreover, the output impedance of the LVS structure can be improved by the CPS technique introduced in the following section to reduce power loss.

E. Proposed CPS Technique

Although the LVS scheme helps reduce voltage stresses and voltage swings, each flying capacitor experiences an idle time corresponding to its hold state (C_1 at state 3 or C_2 at state 1), lowering down the total effective capacitance seen at V_O. On the other hand, there is an inherent correlation between this total capacitance and voltage droop at transient load step so that it is worth eliminating the idle times of flying capacitors. The CPS technique is hence introduced to achieve this goal in a multiphase configuration. Interestingly, this technique not only increases the total effective capacitance, but also reduces the output impedance, thus further improving the efficiency.

Fundamentally, multiphase configuration for SCVRs is known as a method to mitigate output voltage ripple. In this approach, the power stage of an SCVR is split into multiple parallel cells switched at symmetrically interleaved phases to give the best ripple cancelation. With a vast number of interleaved phases, an SCVR could produce extremely low output ripple even without C_O. In the design of SCVR with LVS, multiphase operation also offers a chance of eliminating the capacitor idle times by the CPS technique shown in Fig. 5. This architecture consists of three phases $P1$–$P3$ interleaved by $2\pi/3$ phase shifts.

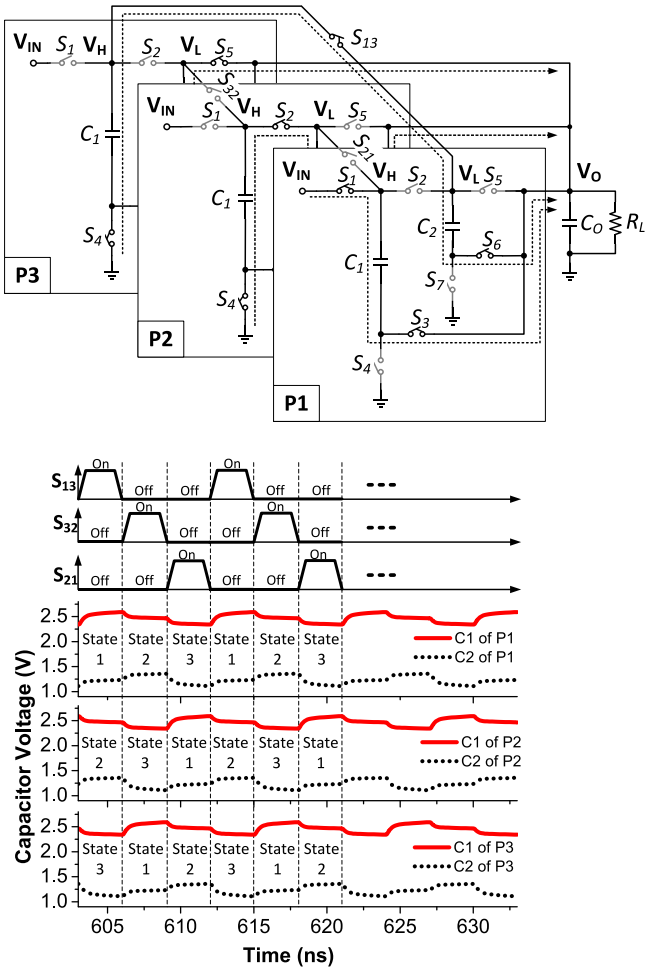


Fig. 5. CPS technique for a three-phase LVS SCVR.

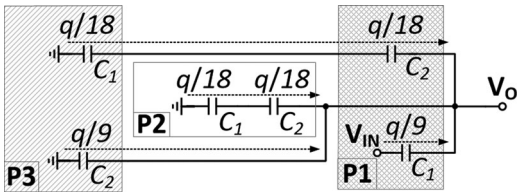


Fig. 6. Normalized charge flows at a state of the CPS topology.

Furthermore, three cross-phase switches S_{13}, S_{32}, and S_{21} are added to bridge from V_L of one phase to V_H of another phase. For example, S_{13} is placed across V_L of $P1$ and V_H of $P3$. These nodes see the same voltage $2/3V_{\rm IN}$ when capacitors C_1 of $P3$ and C_2 of $P1$ are currently in their idle time (state 1 of $P1$ and state 3 of $P3$), S_{13} is then turned ON to connect these capacitors in series and conduct a current to R_L. As a result, the idle times of flying capacitors are avoided. Voltages of flying capacitors during switching states are illustrated in Fig. 5. To understand how this CPS topology also reduces the output impedance, the equivalent circuit of the CPS topology at a typical state is shown in Fig. 6 with normalized charge flows found by KCL and steady-state constraints. The charge multiplier vectors are then determined as

$$a(1) = [1/3\ 1/9\ 1/18\ -1/18\ 1/18\ -1/18\ -1/9\ -1/9]^T \tag{19}$$

$$a(2) = [1/3\ -1/18\ 1/18\ -1/18\ -1/9\ 1/9\ 1/18\ -1/9]^T \tag{20}$$

$$a(3) = [1/3\ -1/18\ -1/9\ 1/9\ 1/18\ -1/18\ 1/18\ -1/9]^T. \tag{21}$$

Plugging values of $a_{Cj}(i)$ from (19)–(21), with $j = 1-6$ and $i = 1-3$, into (7) thus yields the SSL output impedance obtained by CPS

$$R_{\rm CPS,SSL} = \frac{1}{36}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) f_{\rm SW}^{-1} \tag{22}$$

$$R^*_{\rm CPS,SSL} = \min(R_{\rm CPS,SSL}) = \frac{1}{3}\frac{1}{C_{F,\rm TOT} f_{\rm SW}},$$

$$\text{when } C_1 = C_2 = \frac{C_{F,\rm TOT}}{6} \tag{23}$$

where the total flying capacitance $C_{F,\rm TOT} = \sum C_j = 3(C_1 + C_2)$. Comparing (9) and (23), it is obvious that the CPS technique helps reduce the SSL impedance by 25%. In other words, power loss and voltage dropout caused by capacitor charge transfer are lowered down by 25% when CPS is used. Simulations have been done to validate the analytical outcomes. Because the analysis assumes a constant V_O (corresponding to $C_O = \infty$), the simulated output impedances will fit the analytical results if the ripple of V_O is negligible by employing a large C_O, such as $C_O = 6.3$ nF in Fig. 7(a). As expected, a reduction of 25% in the output impedance offered by CPS closely agrees with the simulated results. On the other hand, a big C_O is undesirable, in practice, because of its area overhead. Therefore, a smaller $C_O = 300$ pF is utilized for practical implementation. From the simulations shown in Fig. 7(b), a smaller C_O indeed helps

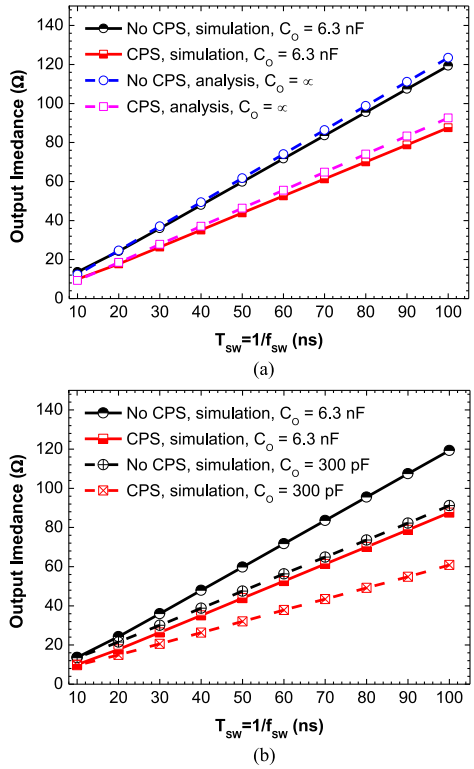


Fig. 7. Simulations of the SSL output impedance for $C_{F,\rm TOT} = 360$ pF: (a) simulations versus analytical outcomes; and (b) impact of output capacitor C_O.

decrease the output impedance even more, thus further improving the efficiency. This is a result of less charge sharing between C_O and flying capacitors, thus lower power loss. However, it comes at the cost of a higher ripple at V_O, which needs to be diminished by employing more interleaved phases. It is noteworthy that increasing the number of interleaved phases and decreasing C_O simultaneously does not change efficiency significantly, because charge sharing between parallel flying capacitors from different phases deteriorates the efficiency saved by the reduction of charge transfer at C_O. The efficiency of the proposed design is improved mainly by CPS while multiphase interleaving reduces voltage ripple without using a bulky C_O. The chip prototype is implemented with six interleaved phases, $C_{F,\rm TOT} = 720$ pF and $C_O = 300$ pF, as described in the next section.

On the other hand, FSL impedance of the CPS topology is evaluated through the switch charge vectors. Because of the symmetry among three phases as well as three cross-phase switches, it is sufficient to find the switch charge vectors of one phase with one cross-phase switch and then triple $\sum a_{rj,\rm RSS}$ of these switches to obtain the total FSL impedance. Switch charge vectors of phase $P1$ with cross-phase switch S_{13} are determined based on charge flows shown in Fig. 6

$$a_{r,P1\&S13}(1) = [1/9\ 0\ 1/9\ 0\ 0\ 1/18\ 0\ 1/18]^T \tag{24}$$

$$a_{r,P1\&S13}(2) = [0\ 1/18\ 0\ 1/18\ 0\ 1/18\ 0\ 0]^T \tag{25}$$

$$a_{r,P1\&S13}(3) = [0\ 0\ 0\ 1/18\ 1/9\ 0\ 1/9\ 0]^T. \tag{26}$$

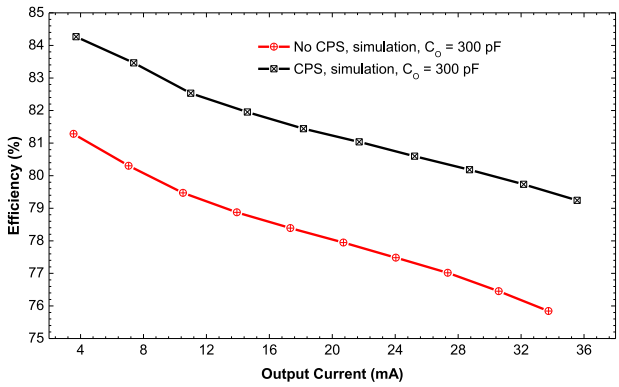


Fig. 8. Simulated efficiency of the LVS power stage with and without CPS, $V_{\rm IN} = 3.7$ V, $V_O \approx 1$ V, and $C_{F,\,\rm TOT} = 720$ pF.

As a consequence, the optimum FSL impedance of CPS is

$$R^*_{\rm CPS,FSL} = \frac{1}{D_{\rm st}G_{\rm tot}}\left(\sum_j a_{rj,\rm RSS}\right)^2 = \frac{1}{D_{\rm st}G_{\rm tot}}\left(3\sum_{j\in P1} a_{rj,\rm RSS} + 3a_{r13,\rm RSS}\right)^2 = \frac{13.71}{G_{\rm tot}}. \quad (27)$$

This result implies a reduction of FSL impedance offered by CPS, thus lowering down conduction loss. This is expected because CPS improves the switch usage when conduction duty cycles of S_4 and S_6 grow from 1/3 to 2/3. Moreover, the efficiency improvement by CPS is verified by simulations shown in Fig. 8 (for power stages only, excluding power consumption of signal processing and controller's circuits). These simulations take into account switching loss of the power stages under the effects of parasitic capacitances obtained by parasitic extraction. All switches are implemented with thin-oxide devices featuring 120-nm channel length. The simulations are conducted for a six-phase configuration, as depicted in the next section. Each phase employs one p-channel MOSFET (PMOS) for S_1, which has a total width of 192 μm, and triple-well n-channel MOSFETs (NMOSs) for all the other switches, each of which has a total width of 84 μm. C_1 and C_2 are implemented with MIM capacitors for low parasitic bottom-plate loss while C_O employs both MIM and MOS capacitors for maximum capacitance density. It is evident that the efficiency of the one with the CPS technique is better by roughly 3% than that without CPS.

Table II brings out a comprehensive comparison between different approaches to realize a 3:1 conversion SCVR. Since output voltage ripple can be diminished by increasing the number of interleaved phases, output ripple is thus not a critical constraint when multiphase interleaving is employed. This table, hence, emphasizes on impedances and efficiency of the studied 3:1 SCVRs.

From Table II, the LVS structure with CPS exhibits the smallest FSL impedance, thus producing the lowest conduction loss of all these topologies. On the other hand, its SSL impedance is the second best, only larger than the MSC converter [17]. Compared with CPS, the MSC technique proposed in [17] can reduce SSL impedance significantly by application of soft charging, but it requires more switches in series as well as smaller conduction duty cycles of switches, thus causing a bigger FSL impedance according to (14). In addition, because of many extra switches and complicated interconnections required in MSC, it will create large parasitic capacitances from metal routing, thereby increasing the switching loss. Depending whether the SCVR is intended to operate in the SSL or FSL mode, efficiency of CPS can be better or worse than MSC. The proposed LVS with CPS should be the best choice for SCVRs that work in the FSL mode.

F. System Architecture

The proposed SCVR is fully integrated on a chip fabricated in a standard 130-nm CMOS process to deliver a nominal output around 1.07 V (the voltage 1.23 V at standard conversion ratio is not used because there must be a voltage drop when the SCVR is loaded) which is regulated by a frequency modulator when the load current varies from 3 to 25 mA. Beyond this current range, the SCVR still works fine if voltage regulation is relaxed, as will be detailed in the measurement results later. To mitigate the output voltage ripple with a relatively small C_O, which is 300 pF in this design, the SCVR is implemented with six interleaved phases using $C_{F,\,\rm TOT} = 720$ pF, as shown in Fig. 9.

These phases are then divided into two groups of three, each group is a three-phase LVS SCVR operating under CPS technique, as described previously. There exists a phase difference of π between these two groups to minimize the output ripple. Phase interleaving is fulfilled by the phase shifter presented in the circuit of a unit phase, which receives three nonoverlapping (NOV) clocks $\rm Clk_1$, $\rm Clk_2$, and $\rm Clk_3$, corresponding to the three states of the LVS scheme from the controller. These NOV clocks are generated by the circuit shown in Fig. 10(a). In the power stages, all power MOSFETs, including PMOS and triple-well NMOSs, are thin-oxide devices with their bulks terminated appropriately to prevent any body-diode conduction. These MOSFETs are switched ON (OFF) by tapping their gates properly to either *GND*, V_O, V_L, V_X, $2/3V_{\rm IN}$, or $V_{\rm IN}$ rails. This is managed by the level shifters adopted from [23], followed by the drivers as illustrated in Fig. 9. Each driver is a tapered inverter chain powered by V_O, V_L, V_X, $2/3V_{\rm IN}$, or $V_{\rm IN}$ rails, respectively. Since V_L and V_X are floating rails, interfacing circuits are used in some drivers as illustrated in Fig. 10(b). A few thick-oxide MOSFETs are used in the level shifters with only a small power overhead since their sizes are much smaller than those of power MOSFETs.

Unlike $V_{\rm IN}$, V_O, V_L, and V_X inherently available in this SCVR structure, the $2/3V_{\rm IN}$ rail is created by an auxiliary $2/3V_{\rm IN}$ generator. Simply, this generator closes the switch $M_{\rm AUX}$ to sample the V_H node of a power stage when this node is at $2/3V_{\rm IN}$ voltage. $C_{\rm AUX}$ then holds the voltage $2/3V_{\rm IN}$ when $M_{\rm AUX}$ turns OFF at the time that V_H jumps up to $V_{\rm IN}$. In this chip implementation, $C_{\rm AUX} = 1.1$ pF, which is negligible in comparison with flying and output capacitances because the $2/3V_{\rm IN}$ auxiliary voltage just needs to deliver a small power for driver circuits.

TABLE II
COMPARISON OF THE PROPOSED LVS WITH CPS, WITHOUT CPS, AND OTHER MULTIPHASE TOPOLOGIES

	The Proposed 3:1 LVS		3:1 MSC Dickson Topology [17]	3:1 FCML Topology [21]	3:1 Series–Parallel Topology [4]	3:1 Ladder Topology [12]
	With CPS	Without CPS				
FSL impedance [a]	$13.71/G_{\rm tot}$	$16.33/G_{\rm tot}$	$18.32/G_{\rm tot}$	$17.49/G_{\rm tot}$	$18/G_{\rm tot}$	$18/G_{\rm tot}$
SSL impedance	$\frac{1}{3}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{4}{9}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{1}{6}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{4}{9}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{4}{9}\frac{1}{C_{F,\rm TOT}f_{\rm SW}}$	$\frac{2}{C_{F,\rm TOT}f_{\rm SW}}$
# power MOSFETs per phase [a]	8	7	10	6	9	6
Stacked MOSFETs	No	No	Yes [b]	No	Yes	No

[a]Given that any switch seeing $2V_{\rm IN}/3$ voltage stress is implemented with a pair of two stacked MOSFETs.
[a]Each pair of interstage switches presented in [17] is actually a form of stacked MOSFETs.

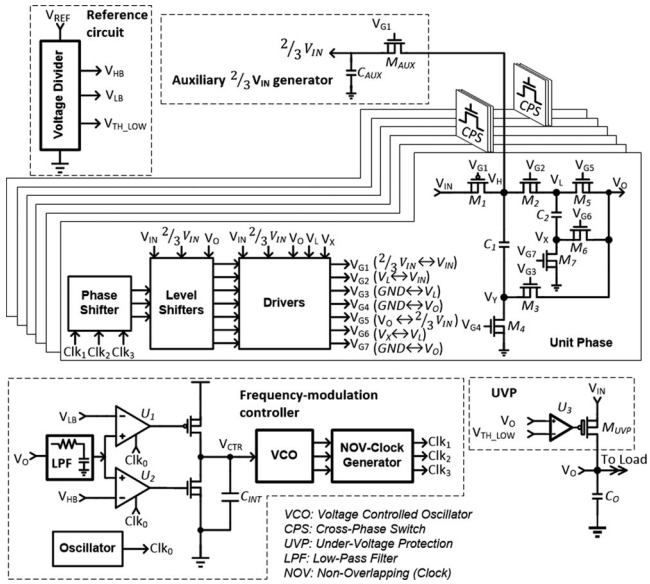


Fig. 9. System architecture of the proposed SCVR. All devices are implemented on-chip, including $C_{\rm AUX}$ and C_O.

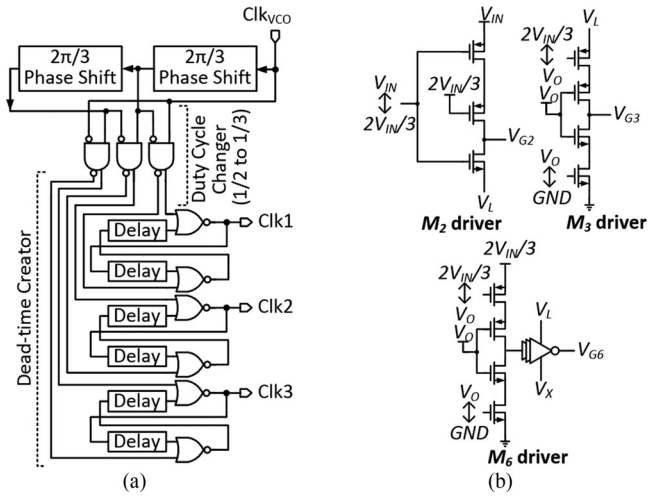


Fig. 10. Dedicated circuits for three NOV clock signals and drivers: (a) three-NOV-clock generator; and (b) drivers' interfacing circuits with floating rails V_L and V_X.

The output voltage is regulated by a frequency-modulation controller, similar to that presented in [3]. However, the main loop is implemented with double bounds (high bound $V_{\rm HB}$ and low bound $V_{\rm LB}$) instead of a single $V_{\rm ref}$ as in [3]. Ripple is removed from V_O feedback signal by a low-pass filter (LPF) before this feedback is compared with $V_{\rm HB}$ and $V_{\rm LB}$. Whenever V_O is lower (higher) than $V_{\rm LB}$ ($V_{\rm HB}$), the charge pump integrator will increase (decrease) $V_{\rm CTR}$, thus incrementing (decrementing) the frequency of the voltage-controlled oscillator (VCO) to pull back V_O to a point between $V_{\rm LB}$ and $V_{\rm HB}$. Unlike the design presented in [3] whose switching frequency is often varied and V_O largely fluctuates around $V_{\rm ref}$, those of the proposed work are less varied once V_O is positioned between $V_{\rm LB}$ an $V_{\rm HB}$. Depending on the required precision of V_O, $V_{\rm HB} - V_{\rm LB}$ could be set to a reasonably small window, which is 52 mV in this design. The selection of this window is based on the design of LPF and the amplitude of output ripple over the desired load range. Since frequency modulation is used as regulation mechanism, output voltage ripple increases at light load. An LPF is designed to attenuate voltage ripple of the feedback signal, thus keeping this ripple within the comparison window at the smallest load current. However, high-attenuation LPF will slow down the dynamic response. Therefore, 52-mV boundary window is a tradeoff between ripple of the feedback signal in the worst case and the load transient response time, which is in the order of hundreds of nanoseconds. In addition, a mechanism of undervoltage protection (UVP) is incorporated to prevent V_O from dropping below a threshold $V_{\rm TH\_LOW}$, which may cause a functional failure in the drivers. Thick-oxide PMOS $M_{\rm UVP}$ is used in the UVP circuit without any efficiency penalty since it remains off in normal condition.

III. MEASUREMENT RESULTS

The proposed fully integrated SCVR is fabricated in a standard 130-nm CMOS process, which features 1.2-V nominal and 1.6-V peak operating voltage for thin-oxide devices, together with 2.5-V and 3.3-V thick-oxide devices. Fig. 11 shows a micrograph of the chip with an area of 750 μm $\times$ 520 μm, excluding pads. The following efficiency measurement has taken into account power consumption of the entire system,

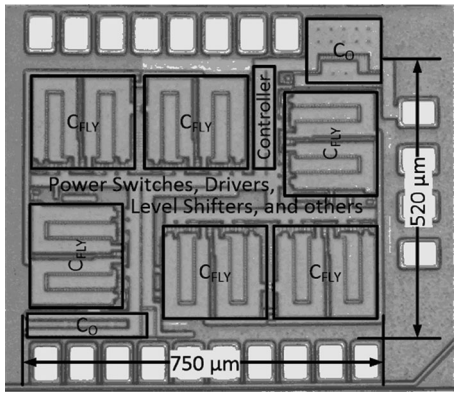


Fig. 11. Micrograph of the chip prototype.

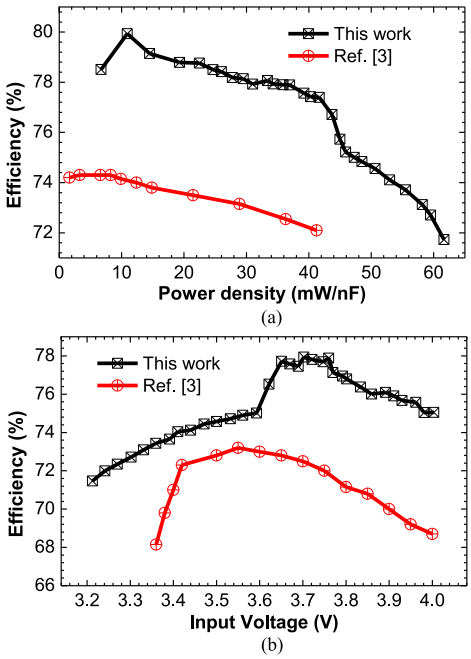


Fig. 12. Efficiency measurement of the proposed SCVR versus that proposed in [3]: (a) efficiency versus power density at $V_{\rm IN} = 3.7$ V; (b) efficiency versus $V_{\rm IN}$ at 36-mW/nF power density.

including the controller, signal interfaces, and the $2V_{\rm IN}/3$ auxiliary voltage generator.

Fig. 12 shows the measured efficiency of the proposed SCVR in comparison with that of the FIVR proposed in [3], which is also designed to work with Li-Ion battery power source at 3:1 conversion ratio. Because the efficiency of an SCVR is inherently dependent on power density that is affected by the technology choice, it is necessary to normalize the power density cross different processes for a fair comparison. It is worth noting that commonly about 80% area of an SCVR is occupied by flying capacitors while the output capacitor could be minimized if not eliminated by a vast number of interleaved phases. Therefore, output power per total flying capacitance is a process-independent measure of power density. As seen in Fig. 12, the proposed SCVR evidently achieves a better efficiency than that proposed in [3] by 5% on average. The efficiency reaches its peak of 80% at 10 mW/nF, then slightly slopes down-

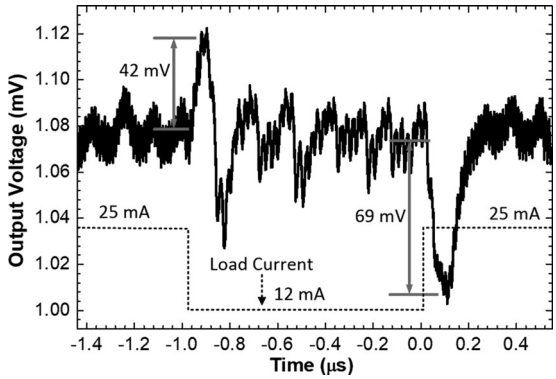


Fig. 13. Load transient response of the proposed SCVR.

ward to 78% at 38 mW/nF. The output dc voltage is kept within 1.07 V $\pm$ 26 mV over the load range from 6.9 to 38 mW/nF by frequency modulation. Above 38 mW/nF, the SCVR is out of its load regulation range, hence its output voltage freely drops while its efficiency rolls off as the switching frequency is no longer adjustable to a proper point. This regulation range is bounded by the VCO of the controller that puts a restriction on the range of switching frequency. Likewise, the efficiency of this SCVR is higher than that proposed in [3] by 5% in its line regulation range from 3.65 to 4 V input while dc voltage of $V_{\rm O}$ is bounded. DC level of V_O and the efficiency both decrease when $V_{\rm IN} < 3.65$ but the measured efficiency is still above than that proposed in [3] for the same 3:1 conversion ratio.

The SCVR's load transient response is shown in Fig. 13. The upper level of the load step is set to 25 mA because the output voltage is out of regulation at current above that level. In contrast, the lower level of 12 mA is employed since the ripple voltage would be dramatically high at lighter load. This is a result of frequency modulation as opposed to self-loading operation (fixed frequency), in which the ripple is reduced at light load but dc level of V_O is unregulated (V_O is freely varied by load current). Regulation range could be improved by a wider tuning-range VCO [3], whereas the ripple at light load could be mitigated without sacrificing dc regulation by a more sophisticated controller [24]. Some low-frequency oscillations are observed in steady state because nonzero step size of $V_{\rm CTR}$ of the charge pump integrator shown in Fig. 9 causes the switching frequency to be slightly different from an exact frequency to deliver a certain load current, hence V_O is slowly varied. Whenever V_O goes beyond the two bounds, the controller will adjust $V_{\rm CTR}$ to pull V_O back to the bounded region, resulting in the low frequency fluctuation seen in the measurement. The voltage droop under a rising load step is 69 mV, equivalent to 6.5%, while the voltage overshoot at the opposite edge of the load step is 42 mV, equivalent to 3.9%. The settling time is approximately 200 ns in both cases.

Table III summarizes the performance of the proposed SCVR in comparison with previous designs of fully integrated SCVRs driven by Li-ion battery compatibility. It is difficult to make a fair comparison of SCVRs designed for different conversion ratios using different processes. However, it can be seen that the proposed SCVR outperforms the other designs at Li-ion battery

TABLE III
COMPARISON WITH PREVIOUS FULLY INTEGRATED SCVRS

	[19]	[14]	[18]	[3]	[17]	This Work
Process (nm)	40	90	180	65	28	130
Capacitor types	MOS	MIM + MOS	NA	MOS	MOM + MOS	MIM + MOS
Area (mm^2)	1.06	3.24	3.2	0.64	0.117	0.39
Input voltage (V)	3.5 – 4	3 – 3.9	2.8	3 – 4	3.2	3.2 – 4
Output voltage (V)	0.8	1.3 – 1.5	0.8	1	0.95	1.07
External high voltage bias	No	No	No	No	8 V	No
Conversion ratio	4:1	2:1	5:2	3:1, 5:2	3:1	3:1
Frequency (MHz)	20 – 160	75	75 – 125	1 – 300	267	10 – 100
Total flying cap. (nF)	2.64	2	NA	3.88	1.5	0.72
Interleaved phases	1	10	1	18	6	6
Max load (mA) [a]	50	100	21	162	135	45
Output ripple (mV)	20 – 60	NA	15	NA	65	30 – 50 [c]
Output voltage droop (%)	7.5	2.1	5	7.6	Unregulated [d]	6.5
Power density (mW/nF) [b]	13	75	NA	42	86	60
Eff. (%) @ 38 mW/nF +	NA	75	NA	72.2	82	78
Peak eff. (%)	70	77	60	74.3	82	80
Li-ion battery compatibility	Yes	Yes	No	Yes	No	Yes

[a] At output voltage drop less than 10% of the nominal level.
[b] Output power per total flying capacitance at output voltage drop less than 10% of the nominal level.
[c] At load current greater than 10 mA.
[d] Output voltage dc level is not maintained at the step-load response waveform presented in [17].

input voltage in term of efficiency even though it uses a less advanced process node. Particularly, compared with the design presented in [3], which is the most appropriate reference for the same 3:1 conversion ratio and similar output voltage, the efficiency of this paper is higher by 5% and the power density is 1.4 times than that proposed in [3]. Breussegem and Steyaert [14] shows a high power density but it delivers only 2:1 conversion ratio and high output voltage (>1.3 V), which tends to cause more power consumption for digital loads, such as processors and SoCs. The designs presented in [18] and [19] provide smaller output voltage, but their efficiencies are only 60–70%, much lower than that of the proposed SCVR. The MSC converter proposed in [17] achieves high efficiency and power density since it is implemented with expensive and advanced baseline 28-nm CMOS, which allows the circuit to switch at much higher frequency (267 MHz) than that of this paper (100 MHz) with minimal switching loss. It is also noteworthy that input voltage of that work is only 3.2 V, substantially below 3.7-V Li-ion battery voltage, because advantages of the 28-nm process come at the cost of lower breakdown voltage. Moreover, that design requires an extremely high external voltage of 8 V for N-type well bias to reduce bottom-plate power loss [17]. Since such high voltage is not inherently available, an extra boost converter is needed. Should this boost converter be fully integrated, it would consume overhead power and increase design complexity, especially to prevent breakdown when generating 8-V bias voltage. The proposed design, in contrast, does not require such high bias voltage.

IV. CONCLUSION

This paper introduces a high-efficiency, fully integrated SCVR that can be directly connected to a Li-ion battery. The LVS topology is proposed to halve the voltage stress across power switches as compared with the conventional series–parallel topology, thus enabling to employ only thin-oxide 1.2-V MOSFETs to reduce power loss when the SCVR is supplied by 3.7-V input voltage. In addition, the presented CPS technique has been proven to produce lower output impedance, thereby decreasing the power loss associated with capacitors' charge transfer by 25% and conduction loss by 16%. These proposed ideas have been verified from analytical theories, simulations, to measurement results. From the measurement results, as expected, the proposed SCVR shows an improvement in efficiency by about 5%, equivalent to approximately 20% reduction in power loss, as compared with conventional figures. It also demonstrates high power density, fast transient response, and reasonable output ripple, which fits well a variety of miniature and fully integrated devices powered by Li-ion batteries.

REFERENCES

[1] S. W. Yoon, B. Petrov, and K. Liu, "Advanced wafer level technology: Enabling innovations in mobile, IoT and wearable electronics," in *Proc. IEEE 17th Electron. Packag. Technol. Conf.*, Singapore, 2015, pp. 1–5.
[2] M. Karpelson, J. P. Whitney, G. Y. Wei, and R. J. Wood, "Energetics of flapping-wing robotic insects: Towards autonomous hovering flight," in *Proc. IEEE/RSJ Int. Conf. Intell. Robots Syst.*, Taipei Taiwan, 2010, pp. 1630–1637.
[3] H. P. Le, J. Crossley, S. R. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19 W/mm2 at 73% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, 2013, pp. 372–373.
[4] H. P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.
[5] N. Tang *et al.*, "Fully integrated buck converter with fourth-order low-pass filter and quasi-V2 controller," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3700–3707, May 2017.

[6] M. Alimadadi, S. Sheikhaei, G. Lemieux, S. Mirabbasi, W. G. Dunford, and P. R. Palmer, "A fully integrated 660 MHz low-swing energy-recycling DC–DC converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1475–1485, Jun. 2009.

[7] M. Wens and M. Steyaert, "A fully-integrated 0.18μm CMOS DC-DC step-down converter, using a bondwire spiral inductor," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2008, pp. 17–20.

[8] P. Hazucha *et al.*, "A 233-MHz 80%–87% efficient four-phase DC-DC converter utilizing air-core inductors on package," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, Apr. 2005.

[9] R. X. Wu and J. K. O. Sin, "High-efficiency silicon-embedded coreless coupled inductors for power supply on chip applications," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4781–4787, Nov. 2012.

[10] N. Sturcken *et al.*, "A 2.5D integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 244–254, Jan. 2013.

[11] C. H. Chia, R. C. H. Chang, P. S. Lei, and H. M. Chen, "A two-phase fully-integrated DC-DC converter with self-adaptive DCM control and GIPD passive components," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3252–3261, Jun. 2015.

[12] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[13] R. Jain *et al.*, "A 0.45–1 V fully-integrated distributed switched capacitor DC-DC converter with high density MIM capacitor in 22 nm tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, Apr. 2014.

[14] T. M. V. Breussegem and M. S. J. Steyaert, "Monolithic capacitive DC-DC converter with single boundary–multiphase control and voltage domain stacking in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1715–1727, Jul. 2011.

[15] C. Schaef and J. T. Stauth, "A 3-phase resonant switched capacitor converter delivering 7.7 W at 85% efficiency using 1.1 nH PCB trace inductors," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2861–2869, Dec. 2015.

[16] W. C. Liu, P. Assem, Y. Lei, P. K. Hanumolu, and R. Pilawa-Podgurski, "10.3 A 94.2%-peak-efficiency 1.53 A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65 nm CMOS," presented at the IEEE International Solid-State Circuits Conf., San Francisco, CA, USA, 2017, pp. 178–179.

[17] N. Butzen and M. Steyaert, "10.1 A 1.1 W/mm2-power-density 82%-efficiency fully integrated 3∶1 switched-capacitor DC-DC converter in baseline 28 nm CMOS using stage outphasing and multiphase soft-charging," presented at the IEEE International Solid-State Circuits Conf., San Francisco, CA, USA, 2017, pp. 182 –183.

[18] Y. Geng and D. Ma, "A 100-MHz breakdown-resilient power converter with fully monolithic implementation on nanoscale CMOS process," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5529–5538, Sep. 2015.

[19] T. Tong, X. Zhang, W. Kim, D. Brooks, and G. Y. Wei, "A fully integrated battery-connected switched-capacitor 4:1 voltage regulator with 70% peak efficiency using bottom-plate charge recycling," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, 2013, pp. 1–4.

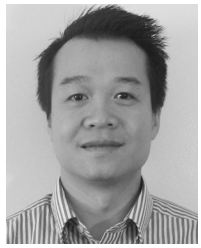
[20] J. Delos, T. Lopez, E. Alarcón, and M. A. M. Hendrix, "On the modeling of switched capacitor converters with multiple outputs," presented at the IEEE Applied Power Electronics Conf. Expo., Fort Worth, TX, USA, 2014, pp. 2796–2803.

[21] A. Stillwell, C. N. Robert, and Pilawa-Podgurski, "A 5-level flying capacitor multi-level converter with integrated auxiliary power supply and start-up," presented at the IEEE Applied Power Electronics Conf. Expo., Tampa, FL, USA, 2017, pp. 2932–2938.

[22] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976.

[23] B. Serneels, M. Steyaert, and W. Dehaene, "A high speed, low voltage to high voltage level shifter in standard 1.2 V 0.13 μm CMOS," in *Proc. IEEE 13th Int. Conf. Electron., Circuits Syst.*, Nice, France, 2006, pp. 668–671.

[24] S. S. Kudva and R. Harjani, "Fully integrated capacitive DC–DC converter with all-digital ripple mitigation technique," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1910–1920, Aug. 2013.



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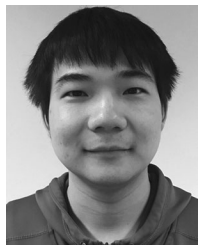

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