Solar Energy Materials and Solar Cells 176 (2018) 9–18

Contents lists available at ScienceDirect

Solar Energy Materials and Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Polycrystalline CdTe photovoltaics with efficiency over 18% through improved absorber passivation and current collection

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ARTICLE INFO

Keywords:
CdTe
Cadmium chloride
Passivation
Photovoltaics
Chalcogenide

ABSTRACT

Sublimated thin-film CdTe photovoltaic devices with conversion efficiencies over 18% and a fill-factor greater than 79% have been repeatedly obtained using high-rate fabrication processes on commercial soda-lime glass substrates used in CdTe modules. Four major improvements to the device have enabled an increase in efficiency from a baseline of approximately 12–18.7%: 1) A sputtered multilayer metal-oxide anti-reflection layer; 2) total replacement of the CdS window layer with a higher bandgap sputtered $Mg_xZn_{1-x}O$ (MZO) window layer; 3) deposition of the CdTe layer at a higher thickness and substrate temperature; and 4) an evaporated tellurium back-contact. This work describes the effect of these changes on the device performance and film microstructural characteristics using various methods. Multiple devices with comparable high efficiency have been fabricated and demonstrated using methods described in this study, yielding very high efficiencies for CdTe polycrystalline thin-film photovoltaics using deposition processes and equipment in a university setting.

1. Introduction

Thin-film CdTe photovoltaics have consistently demonstrated the lowest cost solar electricity generation, particularly for utility scale applications. CdTe is a *p*-type absorber that has a bandgap of 1.5 eV which is nearly optimal for photovoltaic conversion. Approximately 2 μm is sufficient to absorb most of the visible solar spectrum [1,2]. CdTe films are typically deposited on glass substrates using low-cost hardware and high-rate deposition processes [3–5] reducing production costs. Typical crystalline silicon photovoltaics require wafers that are 150–200 μm thick and use a more complex and capital-intensive fabrication process [3].

The low-cost manufacturing of thin-film CdTe PV has enabled agreement for a record low cost power purchase agreement of ¢3.8/kWh for a 100 MW field [6], which is significantly lower than the average cost of electricity in the U.S. of ¢11/kWh [7]. With recent improvements, research-scale small devices have recorded efficiencies of 22.1% [8], while modules with up to 18.6% [9] efficiency have been produced. The leading CdTe PV manufacturer, First Solar Inc., has increased *average production module* efficiency from 13.5% in the first quarter of 2014 [10] to 16.7% in the first quarter of 2017 [11]. Further improving the efficiency without substantial increase in production cost will reduce the levelized cost of energy for CdTe photovoltaics [12,13].

Maintaining the dual requirement of high efficiency and low cost requires the use of film deposition techniques suitable for mass production of millions of solar modules per year. The vapor deposition methods used for this study, including sublimation, evaporation, and sputter deposition, have been used in large scale manufacturing for solar and other industries. Commercially available 3.2-mm soda-lime glass with a fluorine-doped tin-oxide (FTO) transparent conducting layer is a standard substrate for thin-film PV manufacturing, including for CdTe, due to its sufficient strength, reliability, and low cost. Using processes suitable for large scale manufacturing, the authors have explored new materials and process modifications to systematically reduce conversion losses in devices fabricated on low cost glass substrates. This has resulted in an 18.3% efficient device which has been externally certified by Newport Corporation PV Laboratory, Bozeman, Montana, U.S.A. [14]. These independent measurements correspond closely to internal measurements performed at Colorado State University. The performance results have been repeatedly replicated. This is one of the highest efficiency device for which the complete structure has been reported in detail. A detailed materials characterization protocol was used to guide the process optimization. Methods include transmission electron microscopy (TEM) and energy dispersive X-ray

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https://doi.org/10.1016/j.solmat.2017.11.031
Received 12 July 2017; Received in revised form 10 November 2017; Accepted 18 November 2017
Available online 06 December 2017

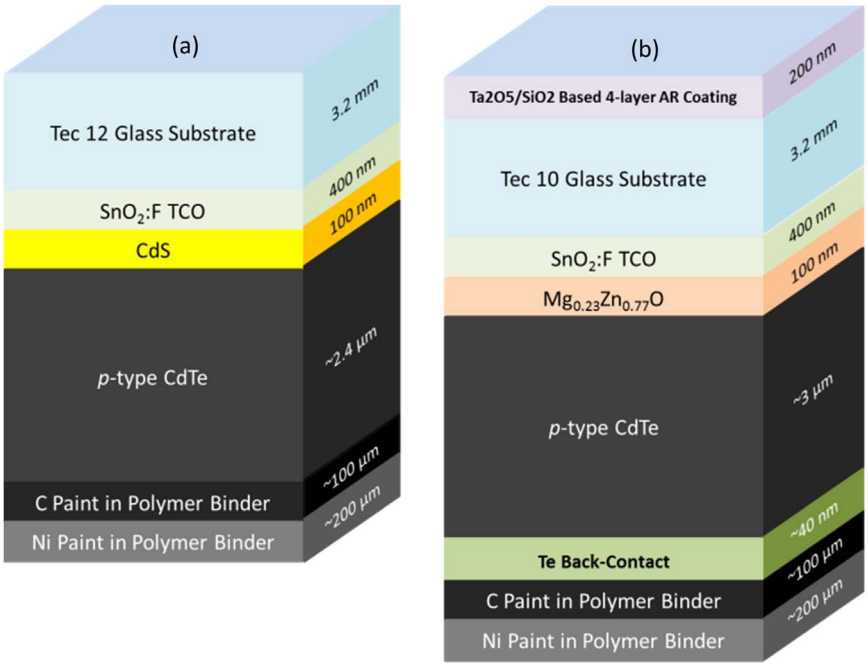

Fig. 1. Schematic of (a) CdS/CdTe baseline device (b) device with changes incorporated to achieve high efficiency (not to scale).

spectroscopy (TEM-EDS). Electrical characterization includes current density-voltage (J-V) measurements to derive device efficiency parameters and spectral response measurements.

2. Device structure for improved efficiency

Thin-film CdTe device structure and processing improvements were characterized to understand their impact on performance and microstructure. At the start of the study, baseline device efficiency was typically 12%, with the device's structure shown in Fig. 1(a). This device had a traditional structure with CdS as the *n*-type window layer while CdTe was the *p*-type absorber. Using CdS as the window layer has a major drawback. CdS is a strong absorber of light above its bandgap of 2.4 eV, and thus the light absorbed within this layer cannot reach the CdTe absorber layer.[15] Photogenerated carriers from CdS are not collected and the light absorbed in this layer is wasted, limiting short-circuit current density (J_{SC}) in the baseline devices. To overcome this limitation, a high band-gap MgZnO (MZO) buffer layer was introduced to replace the CdS window layer. In addition to the traditional Cu back-contact formation, a 20 nm Te layer was also introduced to improve the back-contact. The deposition temperature, film thickness and passivation conditions for CdTe absorber were optimized to achieve improved device performance. At the conclusion of this study, the device structure had been significantly modified, as shown in Fig. 1(b). This improved structure, combined with optimized CdTe absorber deposition and passivation conditions, resulted in the increased device performance of over 18%. Fabrication conditions and characterization of these devices are extensively described in subsequent sections.

3. Experimental

To understand the changes in the optimized new fabrication process, it is important to overview the fabrication of the baseline device shown in Fig. 1(a). The baseline devices were fabricated using a vacuum deposition system at Colorado State University (CSU) capable of performing processes in-line to fabricate a nearly complete CdTe solar cell [16]. The substrate used for the CdS/CdTe reference devices (Fig. 1a) was NSG TEC 12D soda-lime glass produced by Pilkington Group Limited. The NSG TEC 12D glass had fluorine doped tin oxide (FTO) followed by an un-doped, high resistivity transparent (HRT) layer deposited by the glass manufacturer. This HRT layer deposited by glass manufacturer on the TCO was un-doped tin oxide. Only reference devices were fabricated using TEC12D glass while all other devices in this study were deposited on TEC10 glass. Prior to thin-film deposition, the glass substrates were cleaned using International Products Corporation's Micro-90 cleaning solution followed by ultrasonic cleaning and drying under methanol vapor. The baseline device (Fig. 1(a)) fabrication process began with the preheating of the substrate, followed by 130 nm of *n*-type CdS and 2.4 µm of CdTe deposition at a substrate temperature of 440 °C and 445 °C, respectively [16]. After CdTe deposition, sublimation of a $CdCl_2$ layer and an annealing treatment at approximately 400 °C comprised the passivation process for the CdTe absorber. The $CdCl_2$ material was 99.996% pure and Cu content for the material was less than 1 ppm. The substrate was then removed from the in-line vacuum chamber, rinsed with deionized water, and heated again under 40 mTorr vacuum to approximately 150 °C using the in-line fabrication system [16]. A small amount of CuCl was then sublimed onto the CdTe for 110 s with CuCl source temperature at 190 °C and annealed at 200 °C for 220 s to form the device back contact. 99.99% pure copper(I) chloride manufactured by Aldrich-ADL was used and processes was performed under 40 mTorr vacuum with ultrahigh purity nitrogen as the career gas. The back electrode of this device consisted of carbon- and nickel-containing acrylic paints.

Use of HRT layers has been studied to enable the use of thinner CdS layers to decrease above bandgap absorption, but some CdS is still needed to maintain voltage [15]. The CdS *n*-type window layer is a strong absorber of blue light, which causes lack of absorption in the CdTe absorber. Using a more transparent window layer would lead to greater absorption of light in the CdTe absorber layer and higher current generation. MZO has a bandgap of 3.7 eV that is higher than CdS bandgap, which greatly reduces parasitic window layer absorption. ZnO alloyed with MgO to form a HRT layer has been studied by Kephart et al. [17]. In addition to increased ultraviolet transmission, MZO provides a band-alignment more suitable for CdTe [15,17]. The MZO with a composition of $Mg_{23}Zn_{77}O$ was used without an *n*-type CdS window layer to achieve both higher J_{SC} and open-circuit voltage (V_{OC}). All devices fabricated using MZO buffer layers were deposited on NSG TEC 10 soda lime glass that had FTO coated by the manufacturer as the transparent conducting oxide (TCO). TEC 10 glass did not have an un-doped tin oxide HRT layer deposited on FTO. 100 nm MZO films were

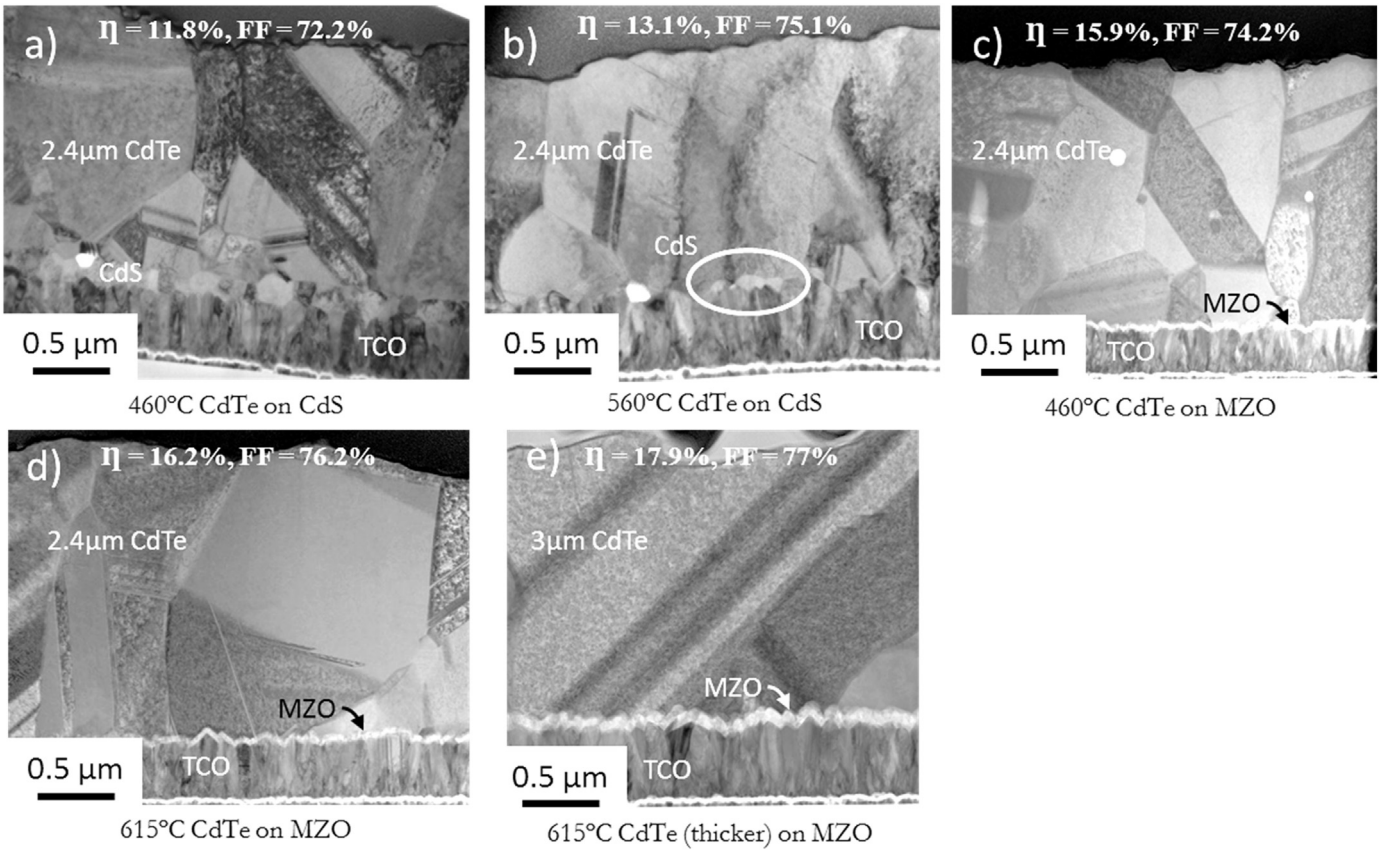

Fig. 2. Cross-section TEM (a) CdS/CdTe baseline device (b) higher temperature CdTe deposition forming larger CdTe grain and CdS depletion (c) CdTe deposition on MZO (d) higher temperature CdTe deposition on MZO, no MZO loss (e) higher temperature and thicker CdTe deposition on MZO. Larger grains lead to higher fill-factor and efficiency.

deposited using RF planar sputter deposition process. MZO acted as a buffer layer on TEC10 glass for CdTe thin-film device fabrication and by replacing CdS with MZO authors were able to completely eliminate the CdS *n*-type window layer. The MZO HRT buffer layer was deposited on TEC10 glass at Colorado State University and was different from the undoped tin oxide HRT layer deposited by glass manufacturer on the TEC12 D that was used for fabrication of devices with CdS window layer. The process gas pressure was set at 5 mTorr with a composition of 1% oxygen in argon. The sputter target was acquired from Plasmaterials Inc. and had a composition of 11 wt% MgO with 89% ZnO with 99.95% purity and a diameter of 10 cm. The substrates were not heated during the sputter deposition [17]. These films were deposited by RF sputtering and were typically 100 nm thick. An initial study of devices using MZO window layers demonstrated devices with 15.5% efficiency with improved J_{SC} and V_{OC} relative to CdS devices [17].

Higher substrate temperatures during growth generally improve grain structure and film quality (Fig. 2). Increasing substrate temperature to 560 °C during deposition of CdTe on CdS window layers produced an improvement in fill-factor [18]. However, the re-sublimation of the CdS window layer restricted further increase in the CdTe deposition temperatures (Fig. 2(b)). In addition to improving transmission and band-alignment, the MZO layer allowed deposition of CdTe films at higher substrate temperatures. Furthermore, MZO was found to be thermally stable at high substrate temperatures and did not re-sublime. This enabled preheating of the substrate to temperatures over 610 °C prior to CdTe deposition–significantly higher than could be achieved with CdS.

Devices described in this study were fabricated on MZO films using a continuous vacuum process in a conventional superstrate configuration.[16,19]. The CdTe sublimation source had a bottom heater to heat the material for sublimation. A top heater positioned above the substrate enabled the substrate to be maintained at the desired temperature. A graphite vapor source containing CdTe was heated to 555 °C ± 3 °C bottom heater and 360 °C top heater, while the substrate was preheated to ~ 610 °C in a separate heater before introducing the hot substrate into the sublimation source. These temperatures and time-set points were determined after several empirical experimental iterations to achieve the desired thickness of CdTe films. The thickness of the CdTe films was maintained at ~ 3.0 μm. It was understood that CdTe deposition would not initiate at the initial substrate temperature of over 610 °C. However, a few seconds after the substrate was placed over the CdTe sublimation source, the substrate temperature would reduce. As the temperature reduced to just the appropriate value for CdTe nucleation to initiate the film growth would start. This caused fewer nucleation sites and thus fewer larger grains. This mechanism led to larger CdTe grains, a higher fill-factor, and thus higher efficiency. This was attributed to fewer grain boundaries, which assisted in reducing recombination in the absorber.

Additionally, the optimal thickness of the large-grain CdTe absorber layer was greater than for the baseline devices. Increasing the CdTe absorber thickness beyond the baseline device of 2.4 μm improved the device performance. The effect of increasing CdTe absorber thickness on MZO/CdTe devices is shown in Fig. 3(a) and (b). Increasing the absorber thickness beyond 2.4 μm improved the fill-factor and J_{SC} of the devices while maintaining the V_{OC}. The carrier lifetime measured by time resolved photoluminescence (TRPL) increased with increased CdTe thickness, as shown in Fig. 3(a). This may suggest that interfaces at the back of the device act as recombination regions. As the thickness was increased, the back interface moved away from the junction, improving its lifetime. Though the lifetime continued to increase for CdTe layers thicker than 3 μm, the thicker layers were more difficult to passivate with the $CdCl_2$ process. An experimentally identified optimum within this study seemed to be of around 3 μm.

After the deposition of the CdTe film, the substrate was then passed

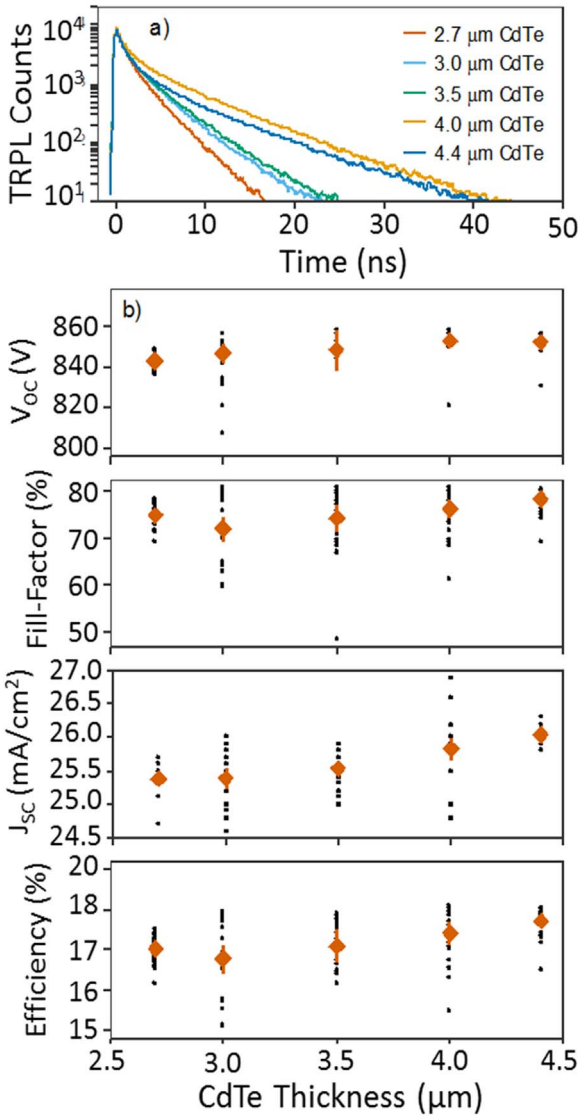

Fig. 3. Effect of varying absorber thickness (a) TRPL measurement showing improved carrier lifetime with increasing absorber thickness **(b)** performance parameters of devices with varying absorber thickness.

over a $CdCl_2$ source for the $CdCl_2$ deposition and activation process immediately after CdTe deposition, without breaking vacuum. An approximately 4 μm $CdCl_2$ film was sublimated on CdTe, where the $CdCl_2$ bottom source temperature was maintained at 447 °C while the top heater—to maintain substrate temperature—was set at 387 °C. This deposition took 180 s, after which $CdCl_2$ activation was carried out for another 180 s, wherein both top and bottom heater temperatures are maintained at 400 °C [18]. The $CdCl_2$ passivation treatment was carried out in an N_2 environment. After $CdCl_2$ activation for 180 s the substrate was transferred to a cooling station for 300 s. This cooling station did not possess a heater. Following cooling, the substrate was removed from the inline fabrication system and rinsed using deionized water.

Copper chloride in controlled quantities has been known to be critical for the formation of back contacts and bulk doping of CdTe photovoltaic films [20]. For the Cu treatment of CdTe film, residual $CdCl_2$ was rinsed with deionized water and substrate was reintroduced into the in-line fabrication tool and heated for 85 s using a heating source set at 330 °C. Following the preheating step, the substrate was introduced into the CuCl sublimation source, where the bottom source temperature was set at 190 °C and the top heater for the substrate was set at 170 °C. CuCl sublimation was performed for 110 s and then the film was annealed in another process station within the tool at 200 °C top and bottom source temperatures for 220 s.

Several materials, such as Au [21], ZnTe [23,24], and Sb_2Te_3 [22,25–27], frequently doped with Cu have been studied as back (hole) contacts to CdTe PV devices. Although reasonable contacts can be made to CdTe using Cu doping, the device performance is quite sensitive to the precise quantity of Cu and subtle process variations [28]. As an alternate to Cu, a Te-rich back contact for CdTe photovoltaics has been studied by Niles et al., Xia et al., and Kraft et al., among others [29–31]. Niles et al. described vacuum evaporated Te as an alternative to chemical etching to avoid the use of acids and the shunting of the device [29]. In addition, Te can be deposited in a highly controlled manner with minimal complexity. Xia et al. [30] found that Cu_xTe, formed from a tellurium back-contact in combination with Cu, had a major impact on improving the fill-factor of CdTe thin-film devices.

In this study, presence of a 20 nm Te layer with Cu at the back surface appeared to form an ohmic contact that caused a substantial reduction in the recombination current, resulting in an improved fill-factor for these devices [30,31]. Evaporation of a 20–100 nm tellurium layer on the Cu-doped back surface of the CdTe, prior to the electrode application, was investigated. 20–25 nm of Te film at the back surface was found to be advantageous, substantially increasing the fill-factor and slightly improving V_{OC}. Further increasing the thickness of Te did not provide any additional benefit. Devices using the Te contact processed without intentional Cu demonstrated over 16% efficiency [14]. The J-V measurements performed at − 75 °C on the Te contacted devices resulted in good fill-factors and no rollover behavior in the fourth power quadrant.

The 20 nm tellurium back contact was deposited using a Cooke Vacuum Products physical vapor deposition (PVD) system: model MK VII – FR. 99.999% pure tellurium pieces used for deposition were obtained from Sigma-Aldrich Corporation. Tellurium pieces were placed in a molybdenum evaporation boat coated with alumina. Acoustic impedance for deposition is set at 9.81 g cm^{-2} s^{-1}. During deposition, the electric current was set between 70 A and 90 A to achieve a steady deposition rate of 5–10 Å/s. The deposition rate and thickness were measured using a quartz crystal monitor and monitored via an external digital display. A sliding shutter between the deposition boat and the substrate allowed for the abrupt start and termination of Te deposition on the substrate. This shutter was manually operated from outside the vacuum chamber. The pressure during Te deposition was maintained at 10^{-5} Torr or less. The substrate was not heated during Te deposition. To verify a continuous and uniform deposition of Te layer, a CdTe film with about 400 nm thick Te layer was fabricated. Thicker Te layer made it easier to image the layer under TEM (Fig. 4).

Soda-lime glass has a refractive index of 1.51 and an average front-surface reflection of 4.1%. The addition of an effective and robust anti-

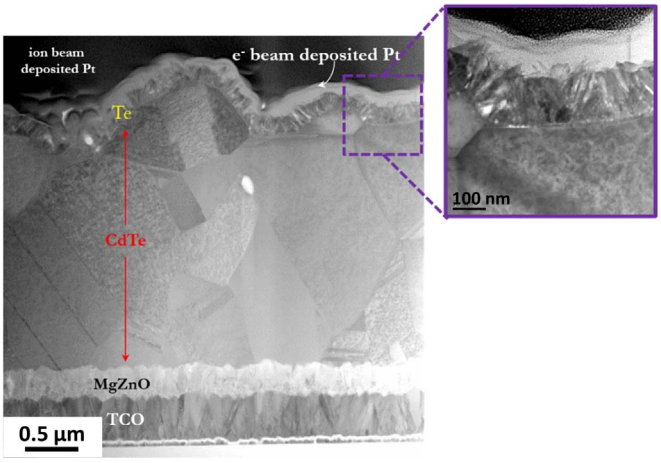

Fig. 4. Cross-section TEM image of CdTe uniform coverage of Te on CdTe surface.

reflection (AR) coating can reduce this value to below 1.5% and allow more light to reach the CdTe absorber, increasing J_{SC} by approximately 1 mA/cm^2 for typical devices. In order to realize these benefits, a 4-layer Ta_2O_5/SiO_2 based AR coating was developed. The AR stack was based on the Reichert design used by Kaminski et al. [32] and had a total thickness of 200 nm.

The antireflection coating was deposited on the uncoated soda-lime glass side of the TEC 10 substrate using ion beam sputter deposition in a Veeco SPECTOR system. This film was of the Reichert design [33]. The design used smooth metal-oxide layers of a precise thickness to provide destructive interference over a wide range of wavelengths and angles of incidence. In this case, Ta_2O_5 was used for the high-index layer, and SiO_2 was used for the low-index layer. Refractive indices for the two oxide materials were measured using variable angle spectroscopic ellipsometry (VASE); thickness results were verified with profilometry. A program was written in MATLAB which calculated the front-surface reflectance of the structure using the transfer-matrix method. This reflectance was multiplied by the photon flux at each wavelength for the AM1.5G spectrum, and a global optimization was performed to minimize the calculated loss in J_{SC} due to reflection. Reflection measurements were performed using an integrating sphere at 8° from normal.

The calculated ideal AR coating increased reflection for photon energies below the bandgap and for high photon energies where the photon flux was low. In the intermediate range, there was a strong reduction in front-surface reflection. To compare the modeled AR coating with the effect in the actual device, reflection was measured on the highest-efficiency device and a comparable device made without AR coating. The actual difference in reflection agreed well with the modeled difference (Fig. 5), with a slight shift to longer wavelengths and interference fringes due to the transparent conductive and window layers. The estimated loss in J_{SC} due to reflection for the AM1.5 global spectrum was 2.7 mA/cm^2 without the coating and 1.6 mA/cm^2 with the coating.

Following the deposition of the 20 nm Te back contact layer, the films are ready to be coated with carbon and nickel paint to form the back electrode. Carbon (graphite) paint in a polymer matrix that was diluted using methyl ethyl ketone (MEK) was sprayed on the Te surface to a thickness of about 50 μm. The carbon paint used was Bonderite S-FN 109B conductive coating. This paint was allowed to dry for 2–5 min, after which similar nickel paint was sprayed. The nickel paint was Loctite EDAG 440 AS E&C. The thickness of this nickel paint was about 100 μm. Both the paints were diluted with methyl ethyl ketone in a ratio of 4:1 and 1:1 respectively. The painted surface was allowed to dry for 6–8 h.

Once the paint was completely dry, the films were delineated into 25 square devices on each substrate, with each square device measuring approximately 0.65 cm^2. Delineation was carried out by masking the painted surface of the film and blasting the unmasked regions, thus exposing the TCO in the unmasked areas. Blasting was performed using plastic media to avoid damage to the glass and the TCO. A thin line of indium was soldered in the regions between the cells that had TCO exposed to form the front electrode contact.

Electrical measurements were performed using a Model 10600 solar simulator from ABET Technologies that used a high-pressure xenon arc lamp with an AM1.5 filter. Current density v/s voltage curves were generated based on electrical measurements performed using the Keithley 2420 SourceMeter controlled by a LabView program. The J_{SC} density was calibrated to cells measured by National Renewable Energy Laboratory (NREL), Golden, Colorado, U.S. The device areas were measured using a webcam that took an image of a backlit solar cell and counted the pixels below certain brightness. Both the light intensity and area were calibrated before each set of measurements. The cells were contacted by a fixture of spring-loaded pins that provide 4-point connection and collected current from all around the front contact of the device.

High quality TEM specimens were prepared using an FEI Nova 600

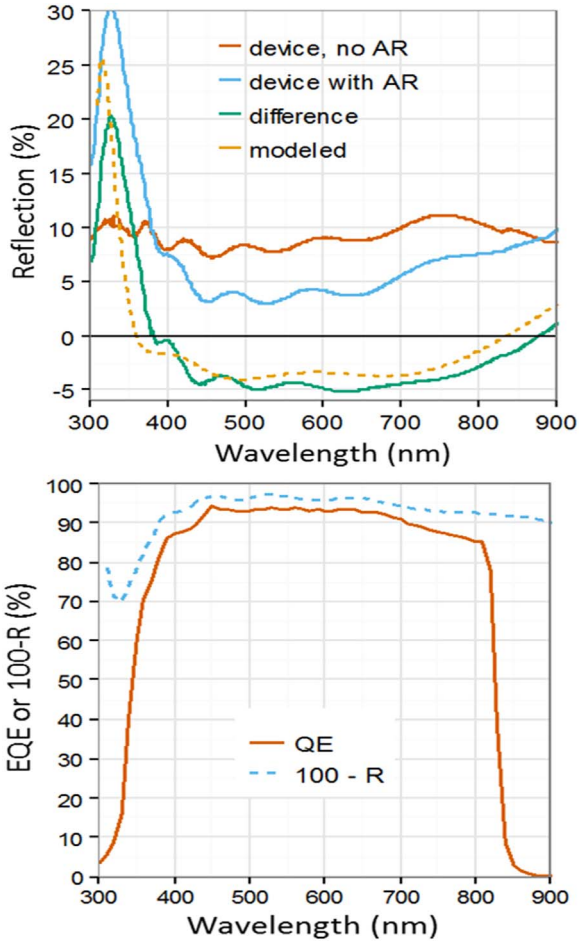

Fig. 5. AR Coating (a) Reflection vs wavelength comparing modeled against actual difference in reflection and **(b)** external quantum efficiency for AR coating used in this study.

Nanolab dual-beam system, where a standard in-situ lift-out procedure was used. This involved depositing a layer of platinum onto the sample surface above the area to be analyzed, using the ion beam with a current of 0.5 nA. A typical area of 20 μm by 2 μm was covered, with a thickness of 2 μm. If the top 50 nm of the sample was required for analysis, then a layer of electron beam deposited platinum (using a voltage of 5 kV and current of 1.1 nA) was deposited before the ion beam platinum. Electron beam platinum is advantageous in that it does not implant ions into the sample surface; however, the deposition of platinum with the electron beam is too slow to use for the whole platinum layer thickness. Two staircase trenches were then cut on either side of the platinum layer which were approximately 25 μm × 15 μm; the depth depends on the sample etching rate, but it was usually of the order of less than 10 μm using an ion beam current of 20 nA. After the formation of the trenches a few micrometers from the platinum, a cleaning cross section was used at the lower current of 7 nA to clean up to the platinum, leaving a sample of approximately 1 μm thick. Once this was done, the sample was tilted to 7° and a U-shaped cut was formed, leaving a small uncut part to support the sample. The omniprobe was then inserted and welded onto the platinum protective layer, with the platinum at 50 pA, and the final support of the TEM sample to the bulk sample was then disconnected using a 1 nA beam. Once this was done, the sample was free and lifted out on the needle by lowering the stage. The next step was to attach the TEM sample to a copper grid and detach it from the omniprobe using a platinum weld at 50 pA and ion beam at 1 nA, respectively.

Once the sample was attached to the copper grid it could be further

thinned down to approximately 100 nm. This was achieved by milling the sample with the ion beam, starting at 1 nA with the sample tilted 0.7° either side of 52°. The sample was milled until it is 500 nm thick. The ion beam current was then reduced to 0.5 nA, and the end 10 μm of the sample was milled on each side until the sample was 200 nm thick. The current was further reduced to 0.3 nA and the end 5 μm was thinned to 150 nm. Finally, the last 5 μm of the sample was thinned using a 100 pA current until the thickness was ~ 100 nm.

Scanning Transmission Electron Microscopy (STEM) was carried out using a FEI Tecnai F20 STEM equipped with Gatan Bright and Dark field STEM detectors, a Fischione High Angle Annular Dark Field (HAADF) STEM detector, a Gatan Enfina Electron Energy Loss Spectrometer, and an Oxford Instruments X-Max 80 mm^2 windowless energy-dispersive X-ray spectrometer (EDX). STEM imaging was performed at 200 kV with a camera length of 100 mm and condenser aperture size of 70 μm using a spot size of seven. HAADF images are collected in conjunction with STEM bright field images. HAADF imaging gives a unique perspective, as the higher the atomic weight of the material, the more the electrons passing through the sample will be detected. Therefore, the amount of signal collected will depend on the atomic weights of the sample, providing atomic weight contrast in the image.

The STEM system was equipped with a Silicon Drift Detector (SDD), allowing high spatial resolution EDX measurements and chemical mapping. This is largely used for mapping the diffusion of elements such as chlorine and sulphur in the cadmium telluride matrix. Point analysis was also useful, as quantification of elements could be acquired with a sensitivity of ~0.5 at% for light elements such as chlorine. EDX spectra were collected for 120 s. Maps were collected using the largest condenser aperture (150 μm) with the largest spot size. This allowed for a high number of counts. The dead time was controlled by changing the process time; each frame took approximately 120 s to collect. Maps were collected in periods from ten minutes to one hour with no discernible sample drift.

Cross-sectional high resolution transmission electron microscopy (HRTEM) was performed on devices to better understand the interaction between the MZO and CdTe. Microscopic elemental distribution within the film stack was mapped using EDS.

Glancing angle X-ray diffraction was conducted using a Bruker D8 Discovery system. The Cu Kα radiation was 1.54060 A° and the grazing incident angle was 2°. The scintillator detector was scanned from 10° to 80° with a step size of 0.05° and scan speed of 1°/min. The measured peaks were fitted using a Pearson VII function in a R programming script and compared with JCPDS card #00-015-0770 for Cadmium Telluride.

4. Results and discussion

The highest efficiency for devices without AR coatings was measured to be 17.9%, as shown in Fig. 6. Reduced reflection losses resulted in higher absorption with the use of AR coating, leading to improved J_{SC}. Such a device yielded the highest efficiency of 18.7%. A similar device from the same substrate was certified by Newport Corporation PV Laboratory, Bozeman, Montana, U.S.A. with a measured efficiency of 18.3% and a V_{OC} of 863 mV, J_{SC} of 26.8 mA, and fill-factor of 79.2% (Fig. 7) [14].

Fig. 6 shows the effect of the different improvements on the J-V and external quantum efficiency (EQE). Comparing the baselines device with the 2.7 μm high temperature CdTe (HT CdTe) device shows that replacing the CdS with the MZO significantly improves the device current. The EQE graph showed that the CdS absorption losses below 500 nm were eliminated. The better band alignment of the MZO, combined with improved film quality from the high temperature deposition, resulted in an increased V_{OC} and fill-factor. The third device with the 3.0 μm absorber showed the effect of the optimized AR stack on device current—the increased thickness further increased the voltage. The increase in J_{SC} can be attributed to increase in absorption at wavelengths greater than 700 nm with increase in absorber thickness, as can be seen in the EQE plot in Fig. 6(b). When the EQE data for increasing thicknesses were plotted against each other, there appeared to be a shift of the CdTe band-edge. The effective bandgap of the absorber appeared to increase which may be due to higher bandgap of MZO in the front. Increase in carrier collection maybe deduced from the increased red-response. Increasing absorber thickness also led to an increase in the fill-factor up to 3.5 μm absorber thicknesses. This increase in fill-factor may be the result of moving the back surface of the device away from the depletion region, resulting in a longer carrier lifetime (Fig. 2(a)) and reduced recombination.

Table 1 shows the performance of the best devices within this study and reinforces the uniformity of the process over a large substrate area. Total of 25 devices were fabricated using this process. The average measured fill-factor for these devices was 79.5%, while the average J_{SC} was observed to be 26.9 mA/cm^2. Earlier MZO/CdTe devices had a V_{OC} of 837 mV, fill-factor of 72.6%, and J_{SC} of 25.2 mA/cm^2.[17] The highest V_{OC} observed within this study was measured to be 863 mV, and the increase from the previous study was attributed to CdTe deposited at a higher substrate temperature (610 °C), resulting in larger CdTe grains and fewer grain boundaries. The J-V plot in Fig. 7(a) shows an excellent fill-factor, and higher absorption can be confirmed from the EQE plot shown in Fig. 7(b). EQE also showed greater absorption at wavelengths lower than 400 nm, suggesting higher charge collection in the absorber with use of MZO and a multilayer AR coating.

Fig. 8 shows the STEM analysis on completed devices (but without the painted electrode layers). The interface between CdTe and 100 nm MZO was continuous and uniform with a homogenous and conformal coverage over the TCO (Figs. 8(b) and 8(c)). CdS has a mismatch of 10% with CdTe and is known to intermix with the CdTe during high

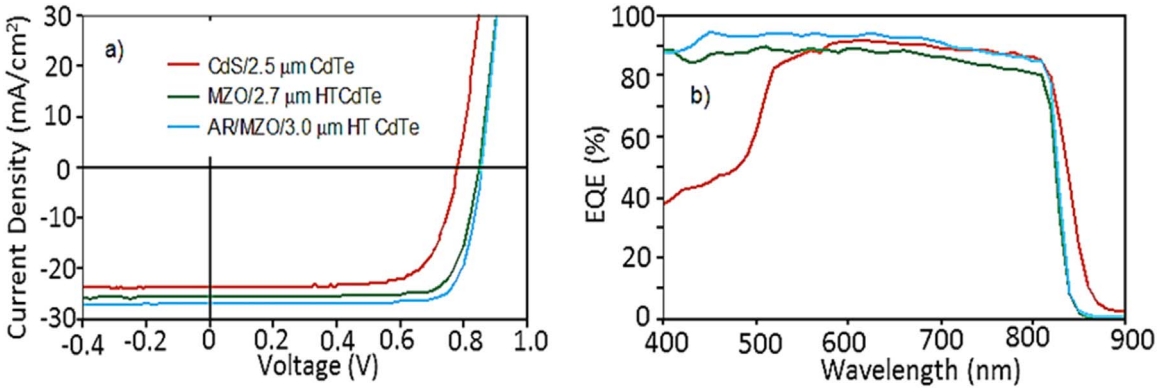

Fig. 6. J-V (a) and EQE (b) comparing performance of CdS/CdTe baseline device, MZO/CdTe high temperature (HT) device and high efficiency high temperature (HT) device with AR coating.

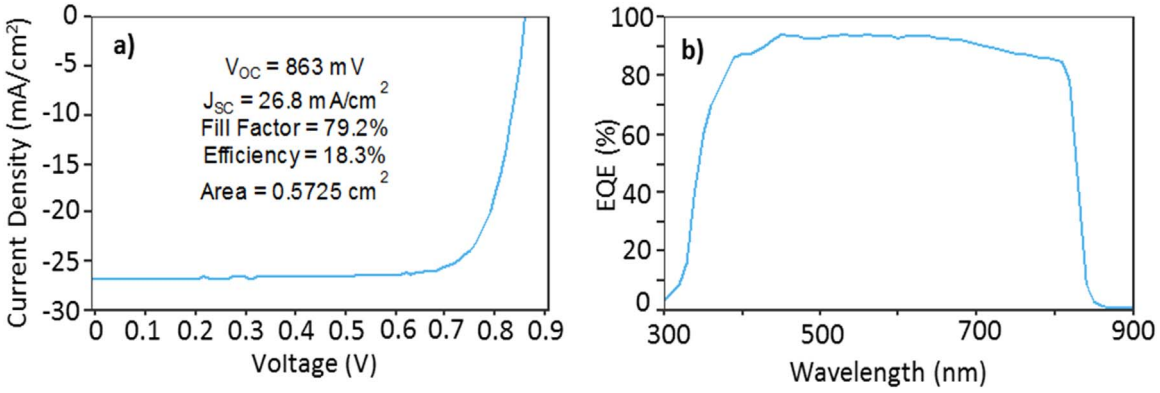

Fig. 7. ILX Lightwave certified results. (a) J-V Curve **(b)** and External quantum efficiency for certified highest efficiency device structure under investigation.

Table 1
Best performing devices measured within the presented study.

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)	Cell Area (cm^2)
1A	858	27.1	80.5	18.71	0.661
1B*	863	26.8	79.2	18.30	0.573**
2	856	27.0	80.1	18.55	0.669
3	856	27.1	79.7	18.46	0.665
4	857	27.0	76.6	18.40	0.666
5	858	26.9	80.5	18.61	0.667
6	858	27.0	80.2	18.59	0.665

*Sample 1B is certified performance for sample 1A by ILX Lightwave, Newport, CA on a masked area**.

temperature deposition and $CdCl_2$ activation [34]. Comparatively, MZO has a greater mismatch with CdTe [17]. EDS maps of these high efficiency devices (Fig. 8(e)) show no signs of MZO diffusing into the CdTe layer within the detection limits of the technique. In addition, the HRTEM image shows an abrupt interface between MZO and CdTe that reinforces minimal intermixing and diffusion between these layers (Fig. 8(d)). Films deposited at a higher substrate temperature (~ 610 °C) exhibit a large CdTe grain size compared to films deposited at a relatively lower substrate temperature [19,35]. The CdTe layer deposited here had an approximate thickness of ~ 3 μm, and the CdTe grains grew from the MZO layer to the back surface as a continuous grain with very few horizontal intercepting grain boundaries.

GIXRD was used to compare the grain texture of baseline CdTe films with those deposited using the new, high-temperature process conditions before and after $CdCl_2$ passivation. At higher 2θ angles, peaks from K_{a2} were observed as a doublet peak. For lattice parameter calculation, 2θ values from the first three high intensity peaks were taken into consideration and compared to the standard. In all cases, the change in the lattice parameter with respect to the standard value was insignificant, suggesting no thermal stresses generated after the $CdCl_2$ treatment.

There was an increase in the peak intensities in the samples treated with cadmium chloride (Fig. 9(a)) indicating improved crystalline quality. To evaluate the preferred orientation (P_{hkl}) of a particular plane in the films, the intensities from the individual and the standard peaks were substituted in the texture coefficient formula and plotted in Fig. 9 [36]:

$$P_{hkl} = \frac{I_{hkl}}{I_{o,hkl}} / \frac{1}{n} \sum_{i=1}^{n} \frac{I_{hkl}}{I_{o,hkl}} \quad (1)$$

Here I_{hkl} is the measured intensity, $I_{o,hkl}$ is the intensity corresponding to the particular plane in the JCPDS card, and n are the number of the peaks considered. As-deposited CdTe (baseline or HT) had a larger texture coefficient, which indicated a strong preferred orientation along {111} plane. After the $CdCl_2$ treatment in the baseline films, the texture coefficient along {111} dropped significantly closer to unity. There was an increase in the texture coefficient along {511} plane, indicating that the preferred orientation had changed. In the films processed at high temperature, the texture coefficient was still larger than unity after the $CdCl_2$ treatment, which suggested that the preferred orientation had not changed significantly.

The full width half maximum (FWHM) of the diffracted peaks provided information about the crystalline quality of the films. For the analysis, the FWHM was measured at the diffracted peaks of the films treated and not treated with $CdCl_2$. From Fig. 9, it was observed that after $CdCl_2$ treatment there was a decrease in the peak width, which suggested that the crystalline quality of the CdTe had increased.

5. Conclusions

High-efficiency devices incorporating several improvements have been fabricated. The device structure is shown in Fig. 1(b). The substrate was TEC10, a product similar to TEC12D but without a HRT layer which had a slightly lower sheet resistance. HRT layer was not needed with the MZO window layer. This was a commercial 3.2-mm thick sodalime glass substrate with approximately 400 nm of FTO deposited by the manufacturer. Deposition of the MZO window layer was performed using radio-frequency (RF) sputter deposition and a 100 nm film was deposited on the FTO [17]. Thereafter, a 3.0 μm CdTe film was deposited using sublimation, followed by a $CdCl_2$ passivation treatment. After rinsing the residual $CdCl_2$ film, CuCl was used to deposit a thin-film of Cu on the CdTe surface via a sublimation process [16,20], and a 20 nm Te film was deposited at room temperature using evaporation to form the back-contact. Following the Te deposition, carbon and nickel paints were deposited.

We conducted a comprehensive study of sublimated polycrystalline CdTe thin-film photovoltaics with an efficiency exceeding 18%. This demonstrates that the inherent simplicity and low-cost manufacturing of CdTe devices is compatible with high efficiency. Sublimated CdTe photovoltaic devices with efficiencies up to 18.7% are reported here with the highest measured fill-factor of 80.5%, J_{SC} of 27.1 mA/cm^2, and V_{OC} of 863 mV. These improvements have been achieved through several process modifications.

Eliminating the CdS window and using MZO enabled preheating of the substrates at temperatures over 600 °C prior to CdTe deposition. Higher substrate temperatures at the start of CdTe sublimation produced larger CdTe grains. The sublimated films were about 3 μm thick. The CdTe grains appeared to grow continuously from the MZO/CdTe interface to the CdTe back surface with very few horizontal intercepting grain boundaries. It has been consistently observed that larger grain size correspond to higher device efficiency (Fig. 2). In addition, using thicker CdTe films contributed in reducing back-surface recombination, since the back surface is situated further from the CdTe absorber bulk. In the reported study, we show that tellurium deposited using

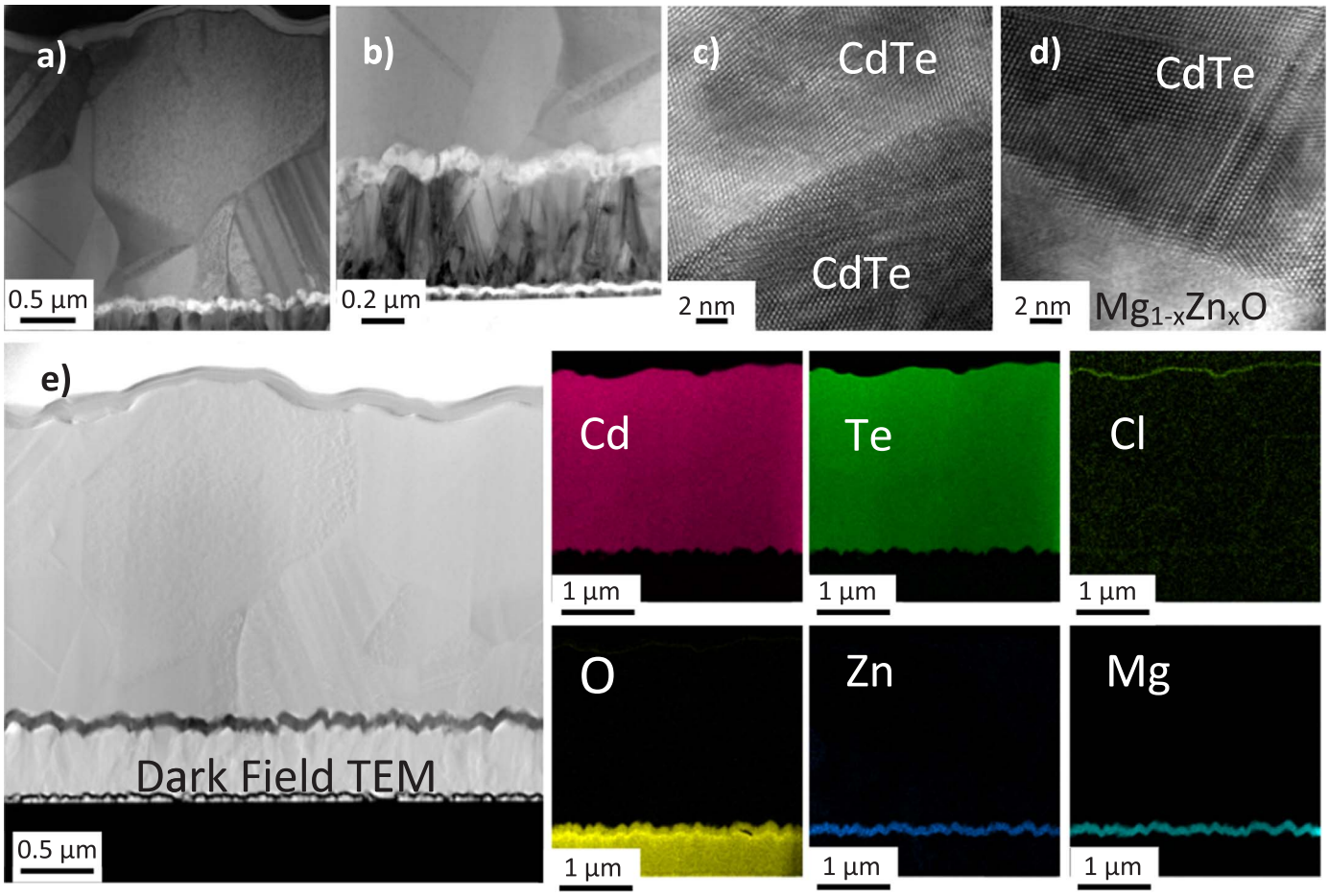

Fig. 8. Microscopic analysis. (a)TEM image TCO/MZO/CdTe/Te film stack **(b)** high magnification TEM image of TCO/ MZO and MZO/CdTe interface showing conformal coverage of MZO **(c)** HRTEM image of CdTe grain boundary showing no apparent signs of line or bulk defects **(d)** HRTEM image of MZO/CdTe interface showing abrupt interface with minimal intermixing **(e)** EDS elemental map of TCO/MZO/CdTe/Te film stack showing no diffusion of materials within detection limits.

evaporation at room temperature enhanced device performance, and that evaporation allowed the deposition of Te to be controlled and uniform (Fig. 4). Reduced recombination in the bulk, as well as reduced back-surface recombination, resulted in a high fill-factor, suggesting higher device quality.

For epitaxial-grown films the interface between absorber and underlying layer must be closely matched to reduce defects and fabricate good devices. However, CdTe is cubic while MZO is hexagonal, and the HRTEM images show an abrupt interface between them. EDS maps show no signs of diffusion of MZO into the CdTe absorber layer. This suggests that improving the quality of this interface can further improve device performance.

Using MZO provides an added advantage of eliminating the CdS window layer. MZO also increases the optical bandgap of the layer that leads to better ultraviolet transmission. This reduces losses from the absorption of photons in the CdS layer, allowing for a greater generation of photo-current and leading to a higher J_{SC}. Adding a Ta_2O_5/SiO_2 multilayer AR coating further reduces reflection losses, improving J_{SC}.

Other studies have shown Cl decorating CdTe grain boundaries and the CdS/CdTe interface after $CdCl_2$ passivation treatment using EDS maps [37]. Using an Electron Energy Loss Spectroscopy (EELS) line scan [35], Li et al. reported a Cl rich region of 1–2 nm at the CdTe/CdTe grain boundary. It was also reported that grain boundaries have enhanced carrier collection after $CdCl_2$ passivation treatment, suggesting that $CdCl_2$ plays a more critical role than just promoting recrystallization [35]. Abbas et al. also found that excessive accumulation of Cl at interfaces and grain boundaries has a detrimental effect on CdTe device performance [38]. Much lower concentrations of Cl were detected using EDS in CdTe films deposited at high temperature on MZO in comparison with those on CdS. Good device performance with such minimal Cl at the grain boundary suggests that the amount of Cl required for enhanced carrier collection at grain boundaries is minimal.

The GIXRD studies confirmed that as-deposited CdTe (baseline or high temperature) has a strong preferred orientation along {111} plane. After the $CdCl_2$ treatment on the high-temperature deposited CdTe, the preferred orientation along {111} plane is maintained. The FWHM comparisons indicate an increase in the crystalline quality of CdTe after the $CdCl_2$ treatment.

Acknowledgements

We would like to thank everyone at Colorado State University's Next Generation Photovoltaics Center who, although not directly involved in this study, contributed to its success through experimental preparation and discussion—particularly Dr. James R. Sites. The authors would also like to thank Dr. Jennifer Drayton for her help with electrical measurements, and Dr. Drew Swanson for performing the time resolved photoluminescence (TRPL) measurements for this study. We are also thankful to Kevan Cameron and the undergraduate staff at CSU's Next Generation Photovoltaics Center for help with tool maintenance and device measurements. This work was partially supported by the National Science Foundation (NSF) Industry/University Collaborative Research Center (I/UCRC) under Award no. 1540007 and the National Science Foundation (NSF) PFI:AIR-RA program under Award no. 1538733. The authors at Loughborough University are grateful to RCUK for funding through the EPSRC Supergen SuperSolar Hub (EP/

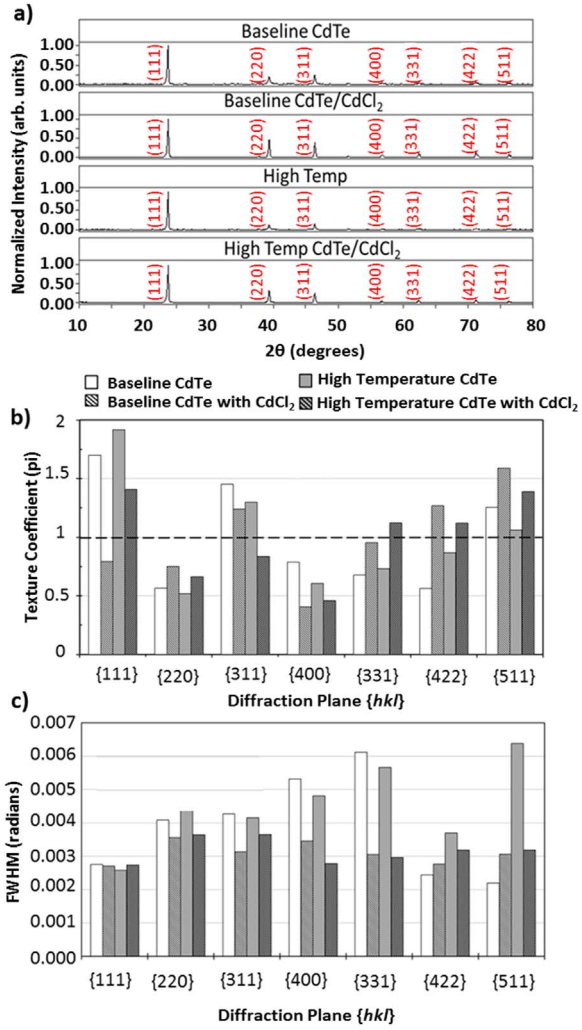

Fig. 9. XRD analysis of film orientation. (a) GIXRD spectra from high temperature CdTe before and after $CdCl_2$ passivation treatment and compared with the baseline CdTe before and after $CdCl_2$ passivation treatment **(b)** Texture coefficients calculated for each diffracted peak **(c)** FWHM measured for each diffracted peak and plotted for comparison.

J017361/1).

Author contribution

The investigation of higher sublimation temperatures was initiated by Dr. Kurt L. Barth. The idea of using a higher temperature deposition for CdTe, along with the $Mg_{0.23}Zn_{0.77}O$ buffer layer, was proposed by Dr. Amit H. Munshi and Dr. Kurt L. Barth. Fabrication of devices and some material's characterization for this study was performed by Dr. Amit H. Munshi. TEM imaging and EDS mapping was performed by Dr. Ali Abbas and analyzed by Dr. Ali Abbas and Dr. John M. Walls. Electrical characterization of finished devices was performed by Dr. Amit H. Munshi. Dr. Jason M. Kephart was responsible for the development of the Ta_2O_5/SiO_2 antireflection coating, as well as the $Mg_{0.23}Zn_{0.77}O$ buffer layer. XRD data was collected and analyzed by Tushar M. Shimpi. The manuscript was mainly written by Dr. Amit H. Munshi, Dr. Jason M. Kephart, Dr. Kurt L. Barth, and Tushar M. Shimpi. Dr. Walajabad S. Sampath is the principle investigator leading the entire project.

Competing interests

The authors declare no competing financial interests.

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