Effect of Substrate Coupling on the Performance and Variability of Monolayer MoS_2 Transistors

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***Abstract*— We study the effect of substrate coupling on the variability and the device characteristics of monolayer MoS_2 field-effect transistors (FETs). Our electrical measurement results reveal significant improvements of key FET device metrics and marked reduction of device variability with reducing the interfacial energy. We attribute the observed improvements of the device characteristics to the reduction of the interface trap density and the suppression of the charged impurity scattering. This study establishes the critical role of substrate coupling on the performance and variability of monolayer MoS_2 FETs.**

***Index Terms*— MoS_2, variability, interfacial energy, FET.**

I. Introduction

MATERIALS discovery and device innovations underlie the advances of the semiconductor industry. A recent example of such research activities includes exploring device prospects of 2-D transition metal dichalcogenides (TMDs), [1], [2]. However, key to the implementation of a realistic electronic system from these nanomaterials is the ability to reliably produce high performance devices with homogeneous electrical properties. Achieving this goal requires a fundamental understanding of the variability in TMD devices.

Past studies have established that stray charges in the surrounding environment, e.g., oxide substrates, are major sources of variability in devices made of nanomaterials. Therefore, various approaches have been implemented for mitigating the device variability, including reducing the oxide thickness [3], [4], using clean fabrication processes [4], [5], and capping nanomaterials with an impermeable film [6]–[8]. Whereas the critical role of oxide substrates on the variations of the device performance is generally accepted, no study has yet examined this problem by studying the adhesion energy at the interface between a 2-D TMD and an oxide substrate. We refer to this energy as the interfacial energy.

Here, we investigate the effect of substrate coupling on the electrical characteristics of MoS_2 transistors. To do so, we fabricated and analyzed four groups of four-point back-gated FETs, where each group represents an interfacial energy that is distinct from the other groups.

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II. Experiment

In our study, we used as-grown monolayer MoS_2 films as the starting material, where MoS_2 was grown using chemical vapor deposition (CVD) on a silicon substrate covered with 285 nm of SiO_2 [9], [10]. In our initial experiments, we found that the as-grown MoS_2 cannot be detached from the substrate by using a standard polymeric stamp [11]. This observation agrees with a previous study by Na *et al.*, reporting the strong adhesion of the as-grown MoS_2 films to the SiO_2 growth substrate [12]. Also similar to their report, our x-ray photoelectron spectroscopy (XPS) measurements (spot size of 10 μm) of the as-grown films (Fig. 1k) showed no detectable covalent or ionic bonding between MoS_2 and SiO_2, thereby suggesting that the bonding at the interface primarily originates from van der Waals interactions. Although the physical origin of this strong adhesion is still unknown, the remarkably high van der Waals force at the MoS_2-SiO_2 interface has been attributed to the high growth temperature [12].

Therefore, to produce MoS_2 with weaker adhesion to SiO_2, we developed a new gold-assisted layer transfer process, described in section II-A. We show in section II-B that these transferred layers have the smallest interfacial energy among the three device groups that were fabricated on SiO_2. Past studies suggest that annealing can lead to stronger bonding between TMD films and the substrate [13]–[15]. Therefore, to create a third set of devices with an intermediate interfacial energy, we did layer transfer of the as-grown monolayer MoS_2 films followed by annealing at 250 °C for 30 minutes under ultra-high vacuum (UHV; 2×10^{-10} torr). This annealing condition has been shown to maintain the MoS_2 film quality [16]. From now, we refer to these three groups of samples as S-I (as-grown), S-II (transferred and then UHV-annealed), and S-III (as-transferred).

A. Device fabrication

To fabricate FETs, we first selected 10 triangular monolayer MoS_2 films at random from four different growth runs. The monocrystalline structure of triangular films allows us to exclude the possible role of grain boundaries on the variations of the device characteristics. Next, we used a combination of electron-beam lithography (EBL), metal evaporation, and lift-off to create three rectangular gold (Au) islands of similar size within each triangular film. We then performed a second EBL step using PMMA resist to create openings that are slightly larger than the Au islands, followed by etching the exposed MoS_2 in a CF_4/O_2 plasma. Figs. 1a-c show the top-view illustration, the cross-section schematic, and an example top-view optical image of an MoS_2 film after these two steps.

To construct the S-II and S-III device sets, we transferred two islands from each MoS_2 film to two different corners

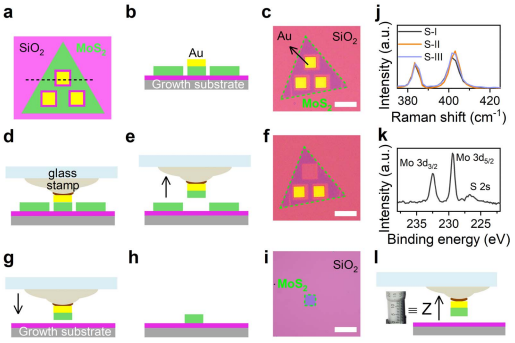

Fig. 1. (a) Top-view illustration, (b) cross-section schematic, and (c) optical image depicting Au-MoS_2 islands within a monolayer flake on SiO_2. (c)-(f) We developed a process based on a stamp-assisted transfer technique for detaching the as-grown MoS_2 from SiO_2. (g) The detached Au-MoS_2 islands were placed in predefined regions of the substrate, followed by (h)-(i) chemical removal of Au. (j) Representative Raman spectra of MoS_2 on the samples S-I, S-II, and S-III. (k) XPS spectrum of an as-grown CVD MoS_2. (l) We estimated the energy release rate by measuring the displacement Z, which is the vertical distance it takes to detach a Au-MoS_2 island from the substrate during a transfer process. Scale bars are 20 μm.

of the same substrate, where no MoS_2 growth had originally occurred. To do so, we developed a new process based on a stamp-assisted transfer technique. In particular, our approach uses a thin-film (20 nm) Au as an intermediate layer between the stamp and MoS_2. We chose Au for two reasons. First, it provides strong binding to the sulfur-based materials, on the order of 1 eV [17]. The second reason is the ease of its processing and chemical etching. Figs. 1d-e show the process steps for detaching a Au-MoS_2 island from the substrate. Our results confirmed that the stack of stamp-Au-MoS_2 can overcome the strong adhesion between the as-grown MoS_2 and SiO_2 (Fig. 1f). The detached islands were then placed at predefined regions of the same substrate, allocated to S-II or S-III devices (Fig. 1g). Fig. 1j shows the equivalency of the Raman data among the S-I, S-II, and S-III device groups.

After the placement, the Au layer was removed chemically (Transene), shown in Figs. 1h-i. We then cleaved the substrate into three pieces to create the S-I, S-II, and S-III samples. The S-II sample was then annealed in a UHV to enhance the adhesion between the transferred MoS_2 layers and SiO_2. Forming Au electrodes using a combination of EBL, metal evaporation, and lift-off completed the device fabrication. Fig. 2a shows the schematic illustration and an example optical image of a back-gated MoS_2 FET on SiO_2.

Past research has shown that h-BN substrates can significantly reduce the long-range Coulomb scattering (and hence increase the carrier mobility) in a variety of 2-D channel materials [18]–[20]. The h-BN substrates achieve this by decoupling the channel material from the oxide substrate. Therefore, to examine the case where MoS_2 is fully decoupled from the SiO_2 substrate, we fabricated a fourth group of devices (S-IV) by transferring CVD MoS_2 islands onto mechanically exfoliated h-BN flakes. Apart from the step involving the stacking of the MoS_2 islands onto h-BN, the other fabrication steps of the S-IV devices were identical to those described above. Fig. 2b shows the schematic illustration and an example optical image of a back-gated FET on h-BN.

B. Estimation of interfacial energy

To gain insight into the effect of the substrate coupling on the device performance, we quantified the adhesion energy

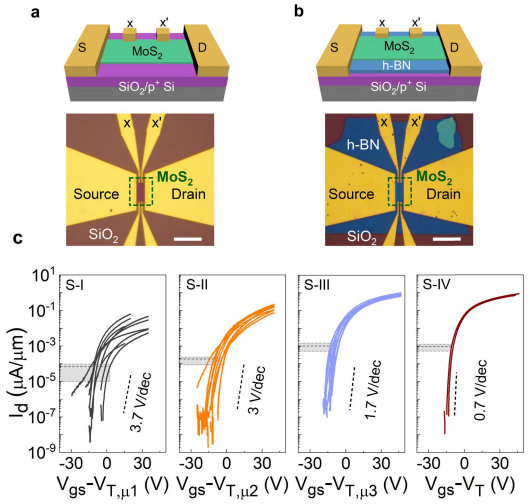

Fig. 2. Schematic and optical image of MoS_2 FETs (a) on SiO_2 and (b) on h-BN substrates. Scale bars are 10 μm. (c) Transfer characteristics of a few tens of FETs measured at $V_{ds} = 100$ mV. Notice the increase of the ON current, reduction of SS, and improvement of the device consistency from S-I to S-IV. The gray shading represents the upper and lower bounds of I_{FB} within each device group.

TABLE I
SUMMARY OF MEASURED Z AND ESTIMATED NORMALIZED G

Sample ID	Experiment	Average Z (μm)	Normalized G
S-I	As-grown	162	1
S-II	Transfer + UHV anneal	108	0.45
S-III	As-transferred	52	0.1
S-IV	Transferred onto h-BN	N.A.	N.A.

at the MoS_2-SiO_2 interface. The interfacial energy γ is given by the product of the energy release rate (G) and the bond density. Since the bond density is the same among all samples in our experiments, we used G as a proxy for γ. We estimated G using the formulation derived from the single-beam cantilever technique [21] $G = (3Eh^3Z^2)/(8L^4)$ where Z, E, L, and h denote the vertical displacement, Young's modulus of the film, beam length, and thickness. The beam theory is commonly used for estimating the surface energy of solid-state materials [21] and also for estimating the adhesion energy between 2-D materials and their growth substrates [12], [22]. To simplify the analysis, we kept the dimensions of the MoS_2 islands and the substrate thickness the same in all transfer experiments. This allowed us to quantitatively compare the magnitude of the energy release rate for S-I, S-II, and S-III simply by comparing their corresponding vertical displacement. Table I summarizes the average measured Z of each device set and the corresponding normalized G, which was calculated by taking the ratio of the average Z for each device set to that of S-I. We measured the vertical displacement (with an accuracy of 5 μm) using the micromanipulator in our layer transfer setup (Fig. 1l), and averaged over four transfer experiments. Our calculations revealed that the interfacial energy of the as-transferred MoS_2 is about 10 times smaller than the as-grown film.

III. Results and Discussion

In Fig. 2c, we show the transfer characteristics of a few tens of FETs from our device groups. All FETs had the same gate length of 3 μm. From the data, we observed that the ON current, SS, and the device-to-device variations

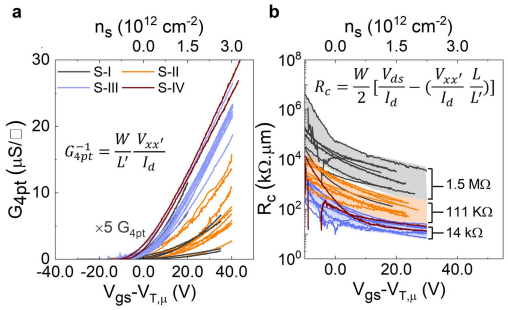

Fig. 3. (a) Comparison of G_{4pt}. For better illustration, G_{4pt} of S-I was multiplied by a factor of 5. The inset shows the equation for calculating G_{4pt}. W, L', and $V_{xx'}$ denote channel width, spacing, and voltage drop between the x and x' electrodes. (b) We found R_c from the four-point measurements. n_s is the charge density calculated from $C_{ox}(V_{gs} - V_T)$.

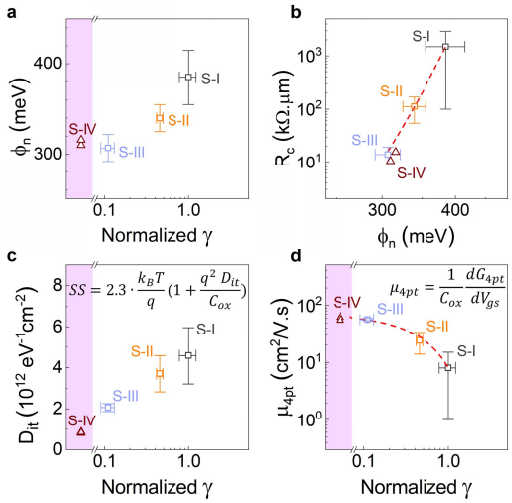

Fig. 4. (a) We observed the lowering of ϕ_n with reducing the interfacial energy. ϕ_n was estimated from I_{FB} in Fig. 2c. (b) The exponential relationship between R_c and ϕ_n agrees with the barrier-limited nature of contacts in MoS_2 FETs. (c) Summary of D_{it} estimated from the SS data in Fig. 2c. (d) Four-point measurements also revealed significant increase of the carrier mobility with reducing the interfacial energy. The pink shading in all plots represents the region where MoS_2 is on h-BN.

improved noticeably with reducing the interfacial energy and approaching those of FETs on h-BN. These results clearly illustrate the critical role of the adhesion energy at the MoS_2-SiO_2 interface on the device performance and variability.

Next, to illustrate the reasons for the observed improvements of the ON current, we performed four-point measurements. The intrinsic channel conductivity G_{4pt} was measured using the voltage drop between x and x' terminals ($V_{xx'}$) when biasing the source and drain contacts (Fig. 2). The specific contact resistance R_c was calculated by subtracting the intrinsic channel resistance ($(G_{4pt} \times L'/L)^{-1}$) from the total resistance (V_{ds}/I_d) [19]. Fig.3a-b show the summary of G_{4pt} and R_c for all FETs. The data indicate that the observed improvement of the ON current with decreasing the interfacial energy is due to the simultaneous increase of the channel conductivity and the reduction of the contact resistance.

To explain the observed reduction of R_c, we estimated the true Schottky barrier height (ϕ_n) using the thermionic emission model. The predictions of this model have been shown to be consistent with ϕ_n extracted from the Arrhenius technique [23]. To estimate ϕ_n, we first determined the flat band current (I_{FB}) from the transfer characteristics of the FETs in Fig. 2c. Specifically, I_{FB} corresponds to the point at which the sub-threshold characteristics begin to deviate from the exponential trend. The gray shading in each plot represents the upper and lower bounds of I_{FB} for each device group. We then estimated ϕ_n by comparing the experimental I_{FB} data against the theoretical predictions given by [23]

$$I_{FB} = q\int_{\phi_n}^{\infty} M(E-\phi_n)f(E)dE \quad (1)$$

where $f(E)$ and $M(E)$ represent the Fermi-Dirac distribution function and the number of modes per unit width. Specifically, ϕ_n was used as a variable in Eq. 1 to match the experimental and theoretical I_{FB}. Fig. 4a shows the summary of the extracted ϕ_n. From the data, we found that ϕ_n decreased with the reduction of the interfacial energy. Moreover, the exponential relationship between R_c and ϕ_n in Fig. 4b is consistent with the barrier-limited behavior of contacts in MoS_2 FETs [23]–[26], indicating that the reduction of ϕ_n was the main cause for the observed improvements of R_c.

It is currently unclear why reducing the interfacial energy caused the reduction of ϕ_n. Notably, this trend coincided with the reduction of the trap density (D_{it}) at the interface of MoS_2 and SiO_2, Fig. 4c. In this plot, we calculated D_{it} from the SS of FETs [27]. On the basis of this observation, we speculate that the interactions between vacancy defects in MoS_2 and oxygen atoms in SiO_2 underlie the apparent variations of ϕ_n with the interfacial energy. This picture is consistent with further decrease of D_{it} when MoS_2 FETs were fabricated on h-BN substrates. However, the physical principles that govern this effect should yet be elucidated.

To better illustrate the trend of how the device variability changed with the interfacial energy, we made the distribution plots for each device parameters (not shown). The data points and the error bars in Fig. 4 represent the mean value and the variance, extracted from those distribution plots. As can be seen, reducing the interfacial energy significantly diminished the variability in FET device performance.

Lastly, we examined the effect of the interfacial energy on the carrier mobility (μ_{4pt}) from the four-point data. The data suggest significant increase (about a factor of 7) of μ_{4pt} with decreasing the interfacial energy (Fig 4d). Moreover, the data show that, with reducing the interfacial energy, the mobility of FETs on SiO_2 substrates approaches those on h-BN. It is well-established that the use of h-BN substrates suppresses the long-range Coulomb scattering originating from the charged impurities in the oxide substrate [18]. Therefore, we infer that the reduction of the interfacial energy has a similar effect on the carrier transport in MoS_2 FETs fabricated on SiO_2.

IV. Conclusion

This study provides an experimental evidence for the critical effect of the substrate coupling on the performance and variability of 2-D TMD devices. Our results establish that reducing the interfacial energy can remarkably improve device characteristics and their consistency. This finding provides an important practical guide for engineering TMD growth and fabrication processes on oxide substrates.

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