Copper-Doped Zinc Telluride Thin-Films as a Back Contact for Cadmium Telluride Photovoltaics

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***Abstract* — With research scale CdTe devices reaching efficiencies over 22%, thin-film CdTe solar cells are part of a growing industry. ZnTe with copper doping can improve overall device efficiency through enhancements in open-circuit voltage and fill-factor. ZnTe has been credited with good device performance and improved device stability. ZnTe displays a promising route for further device improvement. Exploration of ZnTe as a back contact was done with and without copper doping. Devices were characterized to determine how to further improve the incorporation of ZnTe into CdSeTe/ CdTe devices.**

***Index Terms* — CdTe, photovoltaic cells, thin-films, ZnTe.**

I. Introduction

Cadmium telluride (CdTe) solar has been rapidly growing and research scale devices are continually improving in overall efficiency. First Solar has made devices with efficiencies over 22.1% [1]. At Colorado State University (CSU) with CdTe-only devices, efficiencies up to 18.3% were achieved [2]. Now, with further material improvements such as an absorber layer graded with selenium, research scale solar devices with efficiencies over 19% have been demonstrated [3]. Evaporating a 20-30 nm thin layer of Te to form the back-contact in a CdTe device helps in improving fill-factor and open-circuit voltage (V_{OC}).

Looking into further CdTe solar improvements, incorporating zinc telluride (ZnTe) as a back contact has the potential to improve open-circuit voltage and fill-factor. ZnTe has also been credited with improving the stability of devices and improving device performance [4], [5].

Due to the high electron affinity of CdTe, a Schottky barrier forms at the back interface between the semiconductor and metal back-contact. Traditionally, a few monolayers of copper (Cu) are introduced to mitigate this barrier which results in higher device performance. Part of this copper also diffuses into the CdTe absorber layer that leads to p-type doping of the bulk which is desirable. However, using large amounts of elemental Cu or other forms of Cu such as CuCl or Cu(II)Cl are not desirable. Large quantities of Cu in the bulk material can lead to Cu in interstitial sites which is detrimental to CdTe device performance. Excess Cu in the device may also lead to shunting of the device. To avoid these issues related to use of Cu, a more controlled means of Cu for back-contact formation is presented here. This method is used by other research groups for CdTe-only absorber devices [6]. Improvements of copper-doped ZnTe for sublimated CdSeTe/CdTe graded absorber devices are presented in this study. With the addition of copper-doped ZnTe, the buffer layer aides in the valence-band offset to align better with CdTe [7].

II. Experimental

CdSeTe/CdTe graded absorber devices were fabricated and characterized.

A. Device Fabrication

Devices were fabricated in a superstrate configuration by sublimation. Utilizing NSG Tec10 soda lime glass that had fluorine-doped tin oxide layer deposited by the manufacturer as the transparent conducting oxide (TCO). The substrates were cleaned and prepared for deposition of a buffer layer. Instead of traditional cadmium sulfide (CdS), a layer of magnesium zinc oxide layer ($Mg_xZn_{1-x}O$) was sputter deposited via RF magnetron with no substrate heating. MZO is a HRT layer which means it is more transparent than CdS in shorter wavelengths and thus allows higher current generation. It also improves the fill-factor and VOC due to more favorable band-alignment with CdSeTe and CdTe absorber layer. Following the deposition of MZO buffer the substrates were introduced in a single vacuum chamber with multiple sublimation sources [8]. The substrates were heated to ~530°C following which cadmium selenium telluride ($CdSe_xTe_{1-x}$) and cadmium telluride (CdTe) were deposited. Following this a cadmium chloride ($CdCl_2$) passivation treatment was performed without

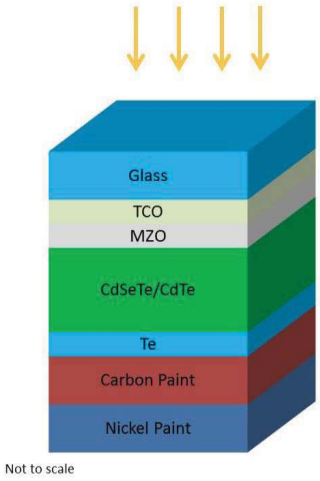

Fig. 1. Superstrate device structure for a standard device.

breaking vacuum. The substrate temperature was maintained at ~470°C while the $CdCl_2$ source was heated to 450°C. After $CdCl_2$ treatment the film is allowed to cool in vacuum for 180 seconds. Thereafter the substrates were removed from the vacuum chamber and excess $CdCl_2$ deposited on the surface is rinsed using deionized water.

The standard device structure deviates at this point. Figure 1 shows the standard device structure. After $CdCl_2$, baseline devices receive a copper chloride treatment where the substrate is heated in a heating source at 330°C for 100 seconds followed by CuCl deposition on the absorber film for 110 seconds with CuCl source heated at 200°C. The substrate is then annealed for 220 seconds at 200°C. The device then receives a layer of evaporated tellurium (~20-30 nm) and is finished with carbon and nickel paint in a polymer binder to form the back electrode.

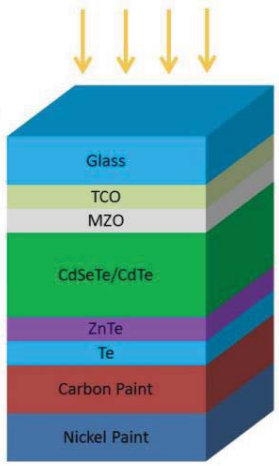

Fig. 2. Superstrate device structure for devices with ZnTe.

As seen in Figure 2, the devices have an added ZnTe layer into the structure after the $CdCl_2$ passivation treatment. Devices are pre-heated to 350°C and temperatures are allowed to reach steady state for 15 minutes. A 100 nm layer of ZnTe was deposited with argon as the working gas via RF magnetron sputtering. The target to superstrate distance was held constant at 6.5cm. Some of the samples were annealed after the ZnTe deposition. Those samples, while still under vacuum at 18 mTorr, samples were held at 350°C for a 15-minute post deposition anneal. The devices received the same finishing steps after the ZnTe deposition. Devices received CuCl treatment after ZnTe deposition. The parameters for CuCl treatment were maintained similar to the process described for fabrication of the standard device. After copper, tellurium evaporation was performed and samples underwent carbon and nickel paint finishing steps. After fabrication, devices were characterized using several techniques.

B. Characterization

Utilizing current density v/s voltage measurements (J-V), devices were analyzed for performance parameters. All J-V measurements were performed at room temperature (~22°C).

Capacitance-voltage (C-V) profiling was performed on devices to determine carrier concentrations.

III. RESULTS AND DISCUSSION

With the addition of ZnTe to the device structure improved overall device efficiency. As seen in Figure 3, from the standard (baseline) device, the V_{OC} significantly increased with the addition of a 100 nm layer of ZnTe before copper doping. The device with ZnTe, annealed for 15 minutes, displays a similar V_{OC} to the ZnTe device but has a better fill-factor that improves the overall efficiency of the device. The device with annealing does shows some indicators of rollover in the first quadrant. Devices were fabricated in the structures shown in Figures 1 and 2.

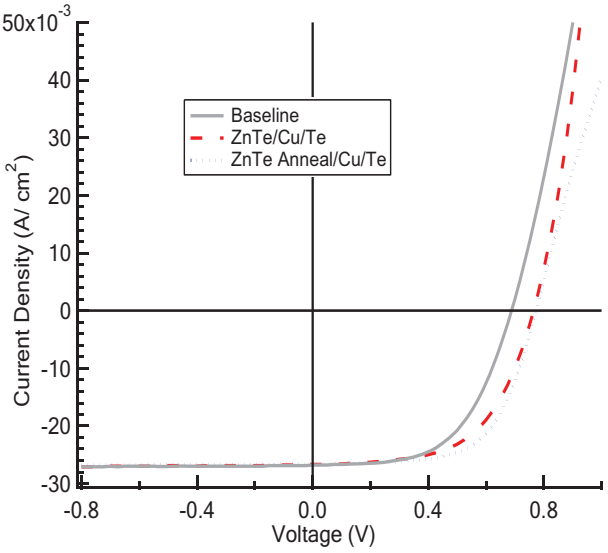

Fig 3. Initial ZnTe device results with a standard (baseline device), ZnTe, and a ZnTe annealed device.

TABLE I
SUMMARY OF DEVICE PERFORMANCE

Device Structure	J_{SC} (mA/cm^2)	V_{OC} (mV)	Fill-Factor (%)	Efficiency (%)
Standard device	26.8	689	56.7	10.47
100 nm ZnTe	26.7	765	57.9	11.83
100 nm ZnTe with a 15 min. anneal	26.6	774	62.9	12.96

Performance parameters from Figure 3, are summarized in Table 1 with J_{SC}, V_{OC}, fill-factor, and efficiency values for the

three devices discussed here. As expected the short-circuit current remained consistent for the devices tested with improvements in the open-circuit voltage and fill-factor. The best device is as shown of the annealed ZnTe device with separate copper doping.

The effects of copper doping were also explored in devices. Figure 4 displays standard devices with and without copper doping as well as a 100 nm annealed ZnTe device with and without copper doping.

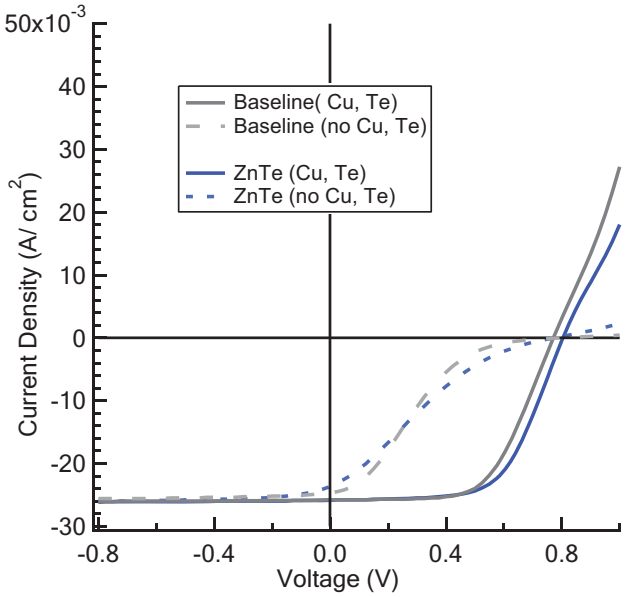

Fig 4. Device performances with and without copper doping.

TABLE II
SUMMARY OF DEVICE PERFORMANCE WITH AND WITHOUT COPPER DOPING

Device Structure	J_{sc} (mA/cm^2)	V_{oc} (mV)	Fill-Factor (%)	Efficiency (%)
Standard device	25.8	771	60.9	12.12
ZnTe anneal	25.8	804	62	12.89
Standard device (no Cu)	24.7	793	18.6	3.64
ZnTe anneal (no Cu)	23.7	775	19.7	3.61

Device performance without any intentional copper doping for the standard and ZnTe annealed devices had large roll over and a poor fill-factor in comparison to the copper doped devices. Device performance with copper significantly improved and increased the fill-factor. Both the standard and ZnTe device indicate signs of roll over at room temperature conditions. Parameters from (Figure 4) the copper doped and no intentional copper doping standard and ZnTe devices can be found in Table 2. Device performance from Table 2 appears to be comparable in terms of open-circuit voltage and short-circuit current. However, fill-factor from the copper doped samples to the no intentional copper doping samples drops significantly which leads to the decrease in overall efficiency in devices.

Utilizing C-V profiling to determine carrier concentrations, the depletion width of the devices were compared. The ZnTe devices from Table II were measured to determine how copper doping impacts carrier concentration as seen in Figure 5.

The C-V measurements performed display a slight increase in carrier concentration for devices with the Cu doped ZnTe sample in comparison to the ZnTe sample with no intentional copper. This conclusion was drawn from the belly of the curve in relation to one another and from the reduction in the distance from the junction. It is important to note that all devices in this study had a consistent thickness of 4.0 µm.

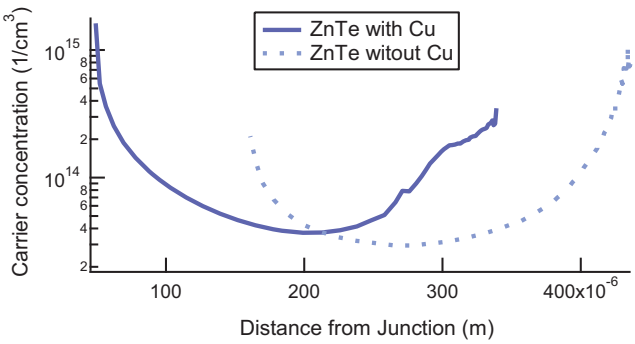

Fig. 5. C-V comparison between copper doped ZnTe and ZnTe with no intentional copper doping.

IV. CONCLUSION

By adding an intermediate ZnTe buffer layer with separate copper doping, to CdSeTe/CdTe devices, efficiency improved due to increased open-circuit voltage and fill-factor. After depositing the ZnTe film at 350°C a post deposition annealing process further improved the device fill-factor. In an attempt to refine the deposition process for ZnTe, devices were processed with and without intentional copper doping.

For future work, a thickness sweep of ZnTe will allow for better understanding of how copper behaves in devices. Future work will also include longer ZnTe post deposition annealing times for continued improvement in fill-factor in comparison to the standard devices created.

Further device characterization of ZnTe in CdSeTe/CdTe graded absorber devices is in process to better understand device the behavior of ZnTe with copper doping.

Through the use of copper with ZnTe, the resulting distance from the junction can be seen in the C-V plots in Figure 5. With the addition of ZnTe, device performance increases through improved open-circuit voltage and fill-factor as seen in Figures 3 and 4.

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