Doping CdTe Absorber Cells using Group V Elements

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***Abstract* —Arsenic dopant was incorporated in CdTe absorber layers in high-efficiency CdTe cells using feedstock doped with 10^{18} cc^{-1} for sublimation of films. The goal of the work was to develop a feasible method for creating a hole density equal to, or greater than that currently achievable using copper doping using a CuCl treatment. Doping with arsenic resulted in a modest increase in open-circuit voltage (V_{OC}) and a large improvement in fill-factor and conversion efficiency when compared with copper-doped devices with similar structure. All experiments were performed in the presence of cadmium overpressure to encourage dopant activation in tellurium vacancy sites. Arsenic incorporation was measured using Secondary Ion Mass Spectrometry (SIMS) at 4E+16 atoms/cc^{-1}, about four times greater incorporation than previously seen by the authors. Using a CdSeTe/CdTe graded absorber and arsenic doping, a conversion efficiency of 16.79% was achieved.**

Index Terms- Cadmium compounds, photovoltaic cells, arsenic, II-VI semiconductors materials, solar energy

I. Introduction

CdTe photovoltaics have demonstrated very low-cost electricity generation, particularly for utility scale applications [1]. With improvements in fabrication processes, research scale small devices have recorded efficiencies as high as 22.1% [2] while commercial modules have achieved 18.6% [3]. While the average cost of electricity in the United States is ¢11/kWh [4], the cost of CdTe generated electricity can potentially fall to as low as ¢1/kWh in the near future. The low cost of production, paired with the continual rise in module efficiency has ensured that CdTe remains one of the most important thin-film photovoltaic technologies. The average production efficiency of such modules has increased from 13.5% to 16.2% between 2014 and 2016 [5], [6].

Continuing to improve the efficiency of CdTe photovoltaics while maintaining a low manufacturing cost is key to further advance CdTe for commercial applications. One way of increasing the efficiency of thin-film photovoltaic devices is to improve the open-circuit voltage. The authors have previously demonstrated 18.7% efficiency for polycrystalline thin-film CdTe-only devices using higher deposition temperatures, a tellurium layer in the back contact, and the use of anti-reflection coating [7] and a CdSeTe/CdTe device with 19.2% efficiency without antireflection coating [8]. This study aimed to demonstrate an efficient method to incorporate and activate group V p-type dopants in CdTe films to further improve open-circuit voltage (V_{OC}) in photovoltaic devices.

Effective doping of the CdTe material is necessary in order to achieve device efficiencies in excess of 20% [9]. Colorado State University's current highest efficiency device had a hole concentration of ~10^{14} cc^{-1}. Group V elements are ideal candidates for doping studies because of the similarity in atomic radii. CSU's current dopant, copper, is significantly smaller than the cadmium atom, and thus has significant interstitial diffusion which limits the doping levels obtainable with copper.

The CdTe was deposited via sublimation using CdTe feed stock that has previously had 10^{18} cc^{-1} of arsenic incorporated into it.

II. Experimental Details

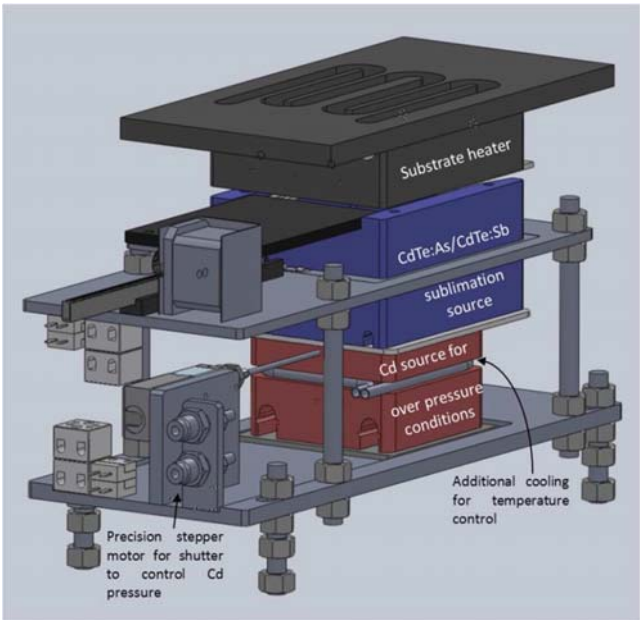

Fig. 1. Schematic of the advanced co-sublimation source

The cells used in the study were deposited on NSG TEC 10 soda lime glass coated with fluorine-doped tin oxide (FTO), a transparent conducting oxide (TCO). A 100nm $Mg_xZn_{1-x}O$ (MZO) buffer layer was deposited using RF sputter deposition.

Deposition of the CdTe films using the Arsenic-enriched feedstock was performed in the advanced co-sublimation hardware at Colorado State University that is shown in figure 1. The substrate was heated to 540ºC before indexing into

another source for sublimation of CdTe. The temperature of the substrate was measured in-situ using a pyrometer located outside the preheating station. The co-sublimation source, as described in earlier papers by Swanson *et al* [10][11], consists of two coaxial sublimation sources that can be individually heated to simultaneously sublimate different materials onto the substrate. In this experiment, The CdTe:As was loaded into the top source, while the bottom source is loaded with >99% pure cadmium. The cadmium was maintained at 280°C to maintain cadmium overpressure during deposition and enhance arsenic activation in tellurium vacancy sites. The top source was maintained at 555°C, which had previously been shown to produce the best devices using undoped CdTe feedstock. Several experiments were performed where the absorber thickness was varied. In the first set of experiments, a 500 nm thick layer of doped CdTe was the sole absorber. In a subsequent experiment, a layer of CdSeTe was deposited prior to the doped CdTe, as seen in figure 3. In these experiments, the total absorber layer varied between 3-4μm. Because of the significant temperature differences between the top and bottom sources, particular attention was paid to independent temperature control of the sources. To maintain independent control over each source temperature, water cooling lines were installed around the sources, providing dispatchable cooling to each source. Without active cooling, the Cd sublimation source would overheat and the Cd pressure would climb to the point where all CdTe deposition was halted.

The CdTe:As depositions were followed by $CdCl_2$ passivation, performed in-line without breaking vacuum. The films were exposed to $CdCl_2$ vapor at 450°C for 10 minutes. All processes were performed in a 40 mTorr N_2 atmosphere.

The CdTe:As feedstock material was prepared by vertical Bridgman based melt growth technique. Raw materials (CdTe) of 6N5 purity and dopants (Cd_3As_2) of 5N purity were sealed in an evacuated quartz ampoule. The mixture was then melted and crystal growth was performed by translating an axial temperature gradient along the melt. SIMS measurement on feedstock indicate an arsenic concentration ~$1x10^{18}cm^{-3}$.

After the deposition of the absorber and the $CdCl_2$ treatment was complete, a 30-nm Te film was evaporated to improve the back-contact. Carbon and nickel paint in a polymer binder were then sprayed onto the films to form the back electrode.

Figure 2 shows a schematic of the full device structure. The individual cells are delineated using a mask and bead blasting to fabricate 25 small scale devices on the substrate. The devices each have an area of ~0.60 cm^2.

III. Results

Figure 3 shows the results of the first series of experiments with a 500nm CdTe absorber layer. When comparing the current density vs voltage (J-V) curves of the undoped (No Cu, No Te) sample to that of the Cu-doped sample (Figure 3), it is observed that the addition of copper doping degrades the performance of the device, particularly the J_{SC} and fill-factor. Alternatively, when comparing the As-doped sample, no such degradation is observed. In fact, the As-doped sample shows a greater J_{SC} and less voltage-dependent collection, resulting in a fill factor of nearly 65%, greater than either the undoped or Cu-doped samples, as seen in Table 1.

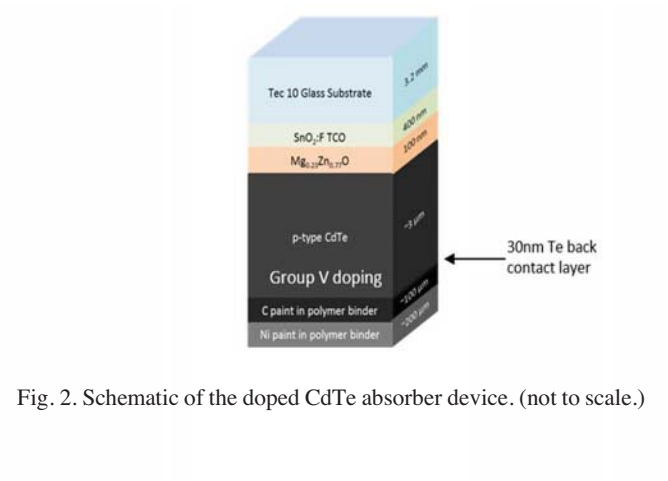

Fig. 2. Schematic of the doped CdTe absorber device. (not to scale.)

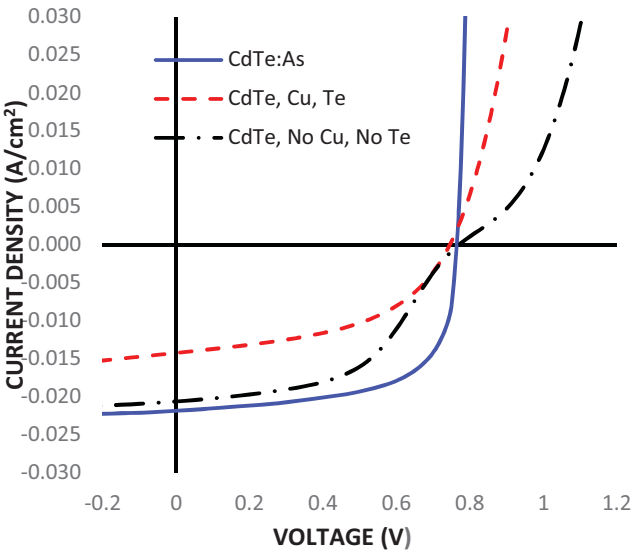

Figure 3: J-V curves for 500 nm CdTe:As, CdTe:Cu, and undoped CdTe

TABLE 1: DEVICE PERFORMANCE FOR THIN CDTE DEVICES WITH VARIOUS DOPANTS

Dopant	Jsc (mA/cm^2)	Voc (mV)	FF (%)	η (%)
None	20.6	769	50.5	8.00
Copper	14.2	745	48.7	5.15
Arsenic	21.8	764	64.8	10.80

Based on the promising results of the thin CdTe absorber devices, the authors next fabricated devices using a graded CdSeTe/CdTe absorber, shown in Figure 4.

Figure 5 shows the J-V performance of a CdSeTe/CdTe:As device compared to a CdSeTe/CdTe:Cu device. This shows that while the Arsenic -doped device displays a modest improvement in both J_{SC} and V_{OC}, it also has a kink, likely attributed to a barrier at the back contact. This may also suggest that while the absorber is uniformly doped with As, a back contact with higher doping may be required to reduce the barrier and thus improve the fill-factor.

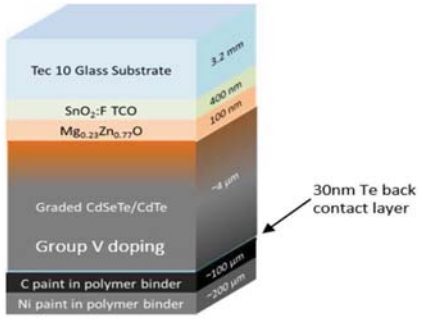

Figure 4: Schematic of the As-doped device structure with a graded CdSeTe/CdTe absorber

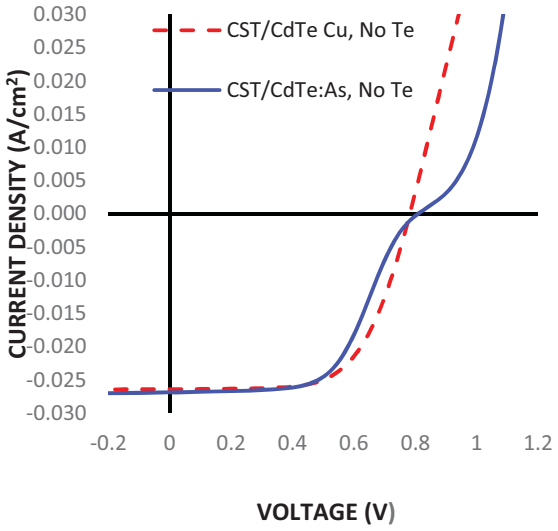

Figure 5: J-V curves for 3.5μm CdSeTe/CdTe:As, and CdSeTe/ CdTe:Cu

The authors have previously shown that adding a 30nm layer of Tellurium as a back contact improves the device's performance in Copper-doped devices by reducing the barrier between the CdTe absorber layer and the carbon and nickle paint that is used as a back electrode. When a 30nm layer of Te is deposited on CdSeTe/CdTe:As device the same advantage is observed as can be seen in Figure 6. In this figure, the two samples are identical in every aspect except for the addition of 30 nm of tellurium on one sample. This addition straightens the kink and consequently restores the fill factor.

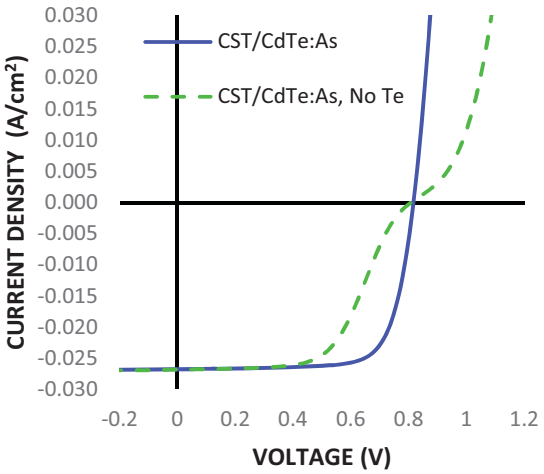

Figure 6: J-V curves for 3.5μm CdSeTe/CdTe:As with Te, and CdSeTe/ CdTe:As without Te

Figure 7 and Table 2 compare the performance of a CdSeTe/CdTe device with no intentional doping to that with traditional CSU doping and back-contact (copper and tellurium) and to that with arsenic doping and a tellurium back contact. Whereas the undoped sample kinks badly beginning at 0.1V, both the copper-doped and arsenic-doped sample show relatively well behaved J-V curves. The arsenic-doped sample shows a slightly lower V_{OC} but a greater J_{SC} and less voltage-dependent current collection than the copper-doped device,

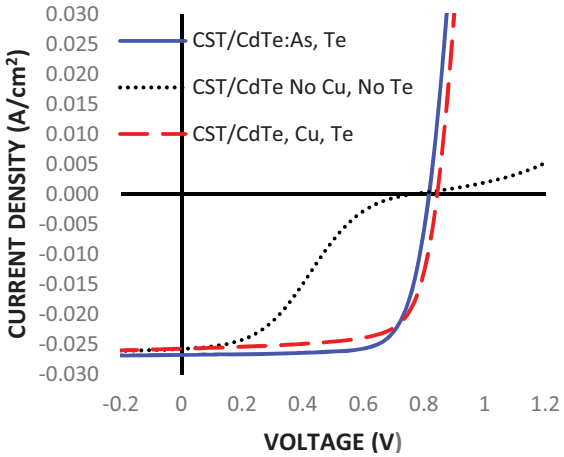

Figure 7: J-V curves of CdSeTe/CdTe devices with Arsenic, Copper, and no intentional doping

leading it to exhibit the highest photovoltaic conversion efficiency found in this experiment at 16.79%.

TABLE 2: DEVICE PERFORMANCE FOR CDSETE/CDTE DEVICES WITH VARIOUS DOPANTS

Dopant	Jsc (mA/cm^2)	Voc (mV)	FF (%)	η (%)
Undoped	25.8	759	33.1	6.48
Copper	26.5	788	67.5	14.10
Arsenic	26.8	818	76.5	16.79

When comparing the Capacitance vs Voltage (C-V) response of the arsenic and copper-doped devices, several things should be noted. First, the arsenic doping achieves a higher doping density, as measured by the belly of the C-V curve, than the copper doping, although only modestly higher. Secondly, because these films were the same thickness, the shrinking of the depletion width in the Arsenic device with respect to the Copper device is further evidence of more effective doping.

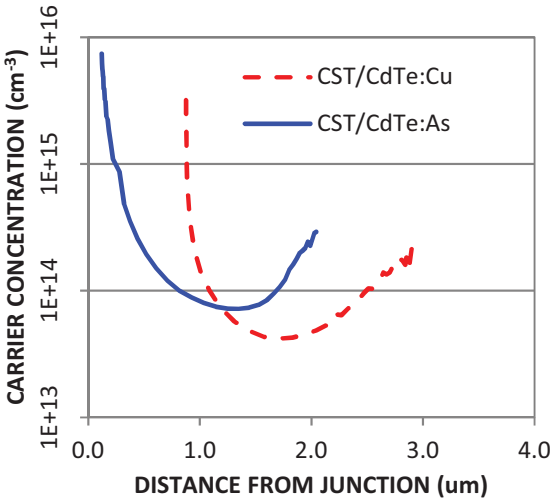

Figure 8: Carrier Concentration Vs. Distance from Junction for Copper and Arsenic-Doped CdSeTe/CdTe devices, derived from C-V measurements

Secondary Mass Ion Spectrometry analysis was performed on the CdSeTe/CdTe:As films to determine the level of arsenic incorporation. Figure 9 shows a relatively stable incorporation density of approximately 4E+16 cc^{-1} throughout the CdTe thickness, with the density slowly climbing through the CdSeTe portion of the film (the first 1-1.5 μm from the front interface.)

IV. DISCUSSION

From the 500nm CdTe results it can be seen that it is difficult to incorporate copper into such a thin absorber layer without adversely affecting the device performance. In this case, the

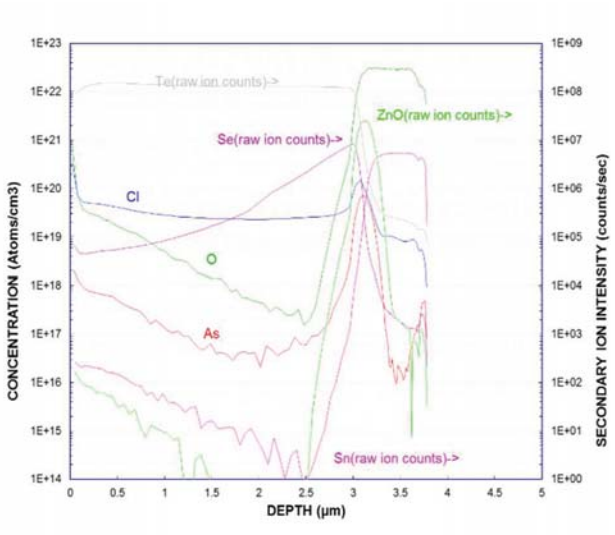

Figure 9: SIMS results showing Arsenic incorporation levels in CdSeTe/CdTe devices

sample was only exposed to the CuCl sublimation source for 5 seconds as compared to over 100 seconds for thicker films, yet the addition of copper results in a substantial loss in both J_{SC} and fill-factor. Because copper doping of CdTe is a proven method of increasing the device performance, it is likely that the degradation is due to increased defect density caused by excess copper in the film. No such difficulties arise when using the CdTe:As feedstock. Because the arsenic is incorporated within the film as it grows, the concern about depositing the dopant after the CdTe film is grown and driving it in via an annealing process is completely eliminated.

Although the C-V plot shows a modest increase in the doping density when arsenic is used instead of copper, figure 4 shows a kink in the arsenic-doped J-V and not in the copper-doped J-V. When considering this difference, it is important to note the difference in the methods of incorporating the two dopants. In the case of arsenic, it is incorporated during film growth, and therefore is distributed uniformly throughout the film. Copper however, is introduced after the CdSeTe/CdTe film is grown, and is diffused into the film from the back. Therefore, although the belly of the two C-Vs show comparable bulk doping densities, the copper-doped sample with have increased copper density at the back of the device, to the point where it removes the back barrier and thus the kink from the J-V curve. At the doping levels thus far achieved using arsenic, the thin layer of tellurium is still necessary to ensure good contact at the back. Further optimization of the doping process may eliminate the need for tellurium at the back.

Finally, a subtle but important difference exists between the methods of incorporating copper and arsenic. While this difference is not immediately apparent from a device performance perspective, it may have powerful implications for device manufacturability. Due to the mobility of interstitial

copper, the CuCl treatment must be performed after $CdCl_2$ step. If it were done prior, the $CdCl_2$ treatment would drive far too much copper into the device, effectively damaging the device. The arsenic however, is incorporated into the film as it grows, during the sublimation of CdTe:As, and thus is present in the film when it receives the $CdCl_2$ treatment. The arsenic survives the $CdCl_2$ process step without hurting the device and thus simplifies the manufacturing process because doping is no longer required as a separate process step.

V. Conclusions

Improvement in doping of the CdTe absorber layer by using arsenic can lead to enhanced photovoltaic conversion efficiency. Using CdTe:As feedstock, the authors were able to achieve greater doping densities than were achieved with Copper-doping methods. By using a graded CdSeTe/CdTe absorber and Arsenic doping, a solar conversion efficiency of 16.79% was achieved. Future work includes further optimization of the CdTe:As sublimation and $CdCl_2$ processes to optimize arsenic incorporation and activation within the film, the use of Transmission Electron Microscopy (TEM) and Energy Dispersive Spectroscopy (EDS) to create elemental maps that will aid in the study of any compositional or morphological changes to the CdTe structure in the presence of arsenic. Finally, it is believed that the large atomic radius of the arsenic atom will reduce the likelihood of interstitial diffusion through the CdTe lattice and will not suffer from the same limitations present using copper-doping methods.

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