Investigation of Sputtered Oxides and p^+ Back-contact for Polycrystalline CdTe and CdSeTe Photovoltaics

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***Abstract* — Adding a thin layer of Al_2O_3 to the back of CdSeTe/CdTe devices has previously been shown to passivate the back interface and drastically improve surface recombination lifetimes. Using such a structure, lifetimes of over 400 ns have been recorded. Despite this, such devices do not currently show an improvement in open-circuit voltage (V_{OC}) that is commensurate with this effect. Devices were fabricated using a range of Al_2O_3 thicknesses at the back interface. High efficiency devices exceeding 16.4% were fabricated with 0.5 nm Al_2O_3.**

Index Terms- Cadmium compounds, photovoltaic cells, aluminum compounds, II-VI semiconductors materials, solar energy

I. Introduction

Thin film CdTe photovoltaic technology has demonstrated significant progress in the past several years, becoming an important technology for utility scale electrical generation. With improvements in fabrication processes, research scale small devices have recorded efficiencies as high as 22.1% [1] while commercial modules have achieved 18.6% [2]. The average production efficiency of such modules has increased from 13.5% to 16.2% between 2014 and 2016 [3], [4]. Recent developments in module technology continue to drive down the cost of CdTe-generated electricity. Utility scale solar costs are projected to fall as low as ¢1/kWh in the near future while the current lowest cost of utility scale electricity reported with CdTe photovoltaics is ¢3.8/kWh [5].

Improving the efficiency of photovoltaics without substantially increasing the manufacturing cost is key to further reductions in the cost/Wp of photovoltaic modules for commercial applications. One method of increasing device efficiency is to reduce surface recombination, thus increasing the open-circuit voltage (V_{OC}). The authors have previously demonstrated 19.1% efficiency for polycrystalline thin-film CdSeTe/CdTe devices using high deposition temperatures and a Te layer in the back contact [6]. This device shows a marked improvement in short-circuit current density (J_{SC}), while maintaining V_{OC} when compared to a CdTe absorber device. Incorporating a thin, patterned layer of Al_2O_3 at the back of the CdSeTe layer, followed by a p^+ layer of amorphous silicon, will cause an upward bending of the conduction band on a band diagram. This highly doped region at the back will reduce back surface recombination and increase the V_{OC} of the device.

The use of a double hetrojunction Al_2O_3 structure has recently been shown to produce carrier lifetimes of >400 ns, several orders of magnitude greater than the typical lifetimes found in CdTe [7]. Additionally, using Al_2O_3 only at the back has still shown lifetimes increased from several nanoseconds to several hundred nanoseconds. Photoluminescence (PL) experiments further show a large increase in PL intensity when a thin layer of Al_2O_3 is deposited at the back. Despite these improvements, these structures do not result in a higher V_{OC}. The presence of a p^+ layer at the back will allow for the extraction of holes, and is expected to create an improvement in V_{OC}.

II. Experimental Details

The devices used in the study were deposited on NSG TEC 10 soda lime glass coated with fluorine-doped tin oxide (FTO), a transparent conducting oxide (TCO). An $Mg_xZn_{1-x}O$ (MZO) buffer layer was deposited using RF sputter deposition. CdSeTe films were sublimated using an optimized deposition process followed by sublimation of the CdTe layer.

The CdSeTe composition used for this study had 40% Se in the source material and as-deposited films had a band-gap of ~1.40 eV from transmission measurements and Tauc plot. The CdSeTe vapor source was heated to 575ºC and CdSeTe films of ~1.5 μm thickness were deposited. After deposition of CdSeTe, the sample was moved to the CdTe sublimation vapor source and a film ~3.5 μm thick was deposited. The CdTe sublimation source temperature was maintained at 555ºC.

After the deposition of the CdTe layer, the substrate was removed from vacuum and Al_2O_3 was deposited via magnetron sputtering. The sputtering was performed in a 5 mTorr Argon atmosphere with 8% Oxygen. RF power was maintained at 240W. Al_2O_3 was deposited to a thickness of 0.25nm – 20 nm on various substrates. The Al_2O_3 deposition rate was measured by sputtering a film onto NSG TEC 10 soda lime glass for one hour and then measuring the film thickness using profilometry. The deposition time was then adjusted to achieve the desired thickness. The Al_2O_3 deposition was followed by $CdCl_2$ passivation.

The CdSeTe/CdTe interface in the cells was formed after an aggressive $CdCl_2$ treatment, which is known to promote recrystallization and grain growth. The CdSeTe/CdTe film stack was exposed to $CdCl_2$ vapor in vacuum (600 seconds at

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approximately 450ºC, followed by 600 seconds at 400ºC annealing) to promote the inter-diffusion of the CdSeTe and CdTe layers. After the $CdCl_2$ treatment, the films were rinsed with deionized water to remove residual $CdCl_2$ from the surface.

Thereafter, the films were heated to ~140ºC, and CuCl was deposited on the film surface for 110 seconds. This was followed by 220 seconds of annealing at 220ºC, both in vacuum.

Figure 1 shows a schematic of the full device structure. The individual cells were delineated using a mask and bead blasting to fabricate 25 small scale devices on the substrate. The devices each had an area of ~0.60 cm^2.

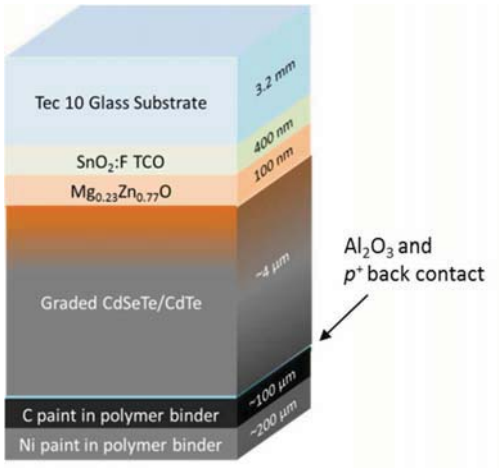

Fig. 1. Schematic of the CdSeTe/CdTe graded absorber device with a layer of Al_2O_3 and P+ doped amorphous silicon (not to scale).

III. RESULTS

Figure 2 shows the results of adding a 0.5 nm layer of Al_2O_3 at the back of the device. With a very thin layer of Al_2O_3, the diode curves of the two devices are very similar. There is no appreciable voltage-dependent current collection. A small increase in the series resistance is seen in the device with Al_2O_3, which primarily affects the fill-factor of the device. The devices' electrical performance metrics can be seen in Table 1. When the alumina thickness was swept from 0.25nm to 20nm, those devices with 0.5nm Al_2O_3 resulted in the best electrical properties.

Figure 3 shows a large increase in the photoluminescence (PL) response of these devices when alumina is deposited at the back. While this pickup in PL intensity is noted for all alumina thicknesses, the devices with 2nm Al_2O_3 resulted in the greatest pickup. It should be noted that the PL response from the CdSeTe/CdTe device is already several orders of magnitude greater than that of the traditional CdTe device, and thus the devices with alumina greatly outperform both CdSeTe/CdTe and CdTe in terms of PL.

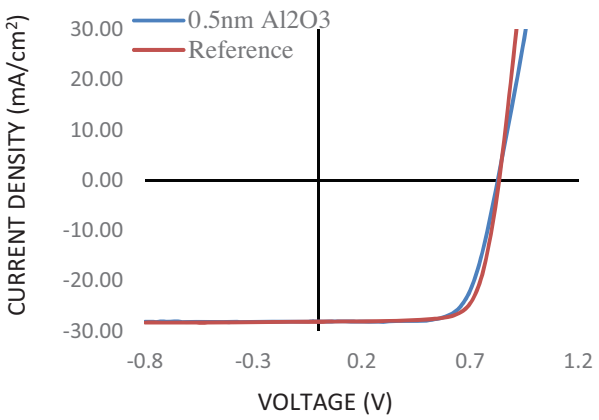

Fig. 2. J-V graph comparing the performance of a device with Al_2O_3 at the back against a CdSeTe/CdTe reference device

TABLE 1: ELECTRICAL PERFORMANCE OF CDSETE/CDTE REFERENCE DEVICE COMPARED TO ALUMINA DEVICE

Device	V_{OC} mV	J_{SC} mA/cm^2	FF %	η %
CdSeTe/CdTe	834	28.1	73.9	17.31
CdSeTe/CdTe w/ Al_2O_3	827	28.1	71.1	16.48

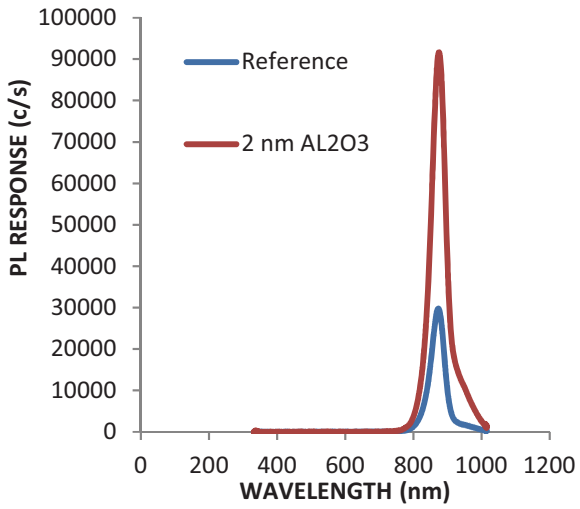

Figure 3: PL Response for a CdSeTe/CdTe reference device compared to a device with Al_2O_3

IV. DISCUSSION

It is clear from the PL response that even a thin layer of alumina at the back of the CdSeTe/CdTe device has a massive impact on the carrier lifetime. This indicates that alumina is passivating the back interface and thus reducing interfacial recombination. The PL peaks are located at 875nm, which corresponds to a band gap of 1.41eV, which is consistent with previous measurements bandgap measurements of the CdSeTe and confirms that the majority of the light is absorbed in the lower bandgap graded CdSeTe absorber material present in the first 1.5μm of the device. The massive increase in band to band recombination is associated with a corresponding reduction in recombination sites within the bandgap. This is consistent with the previous findings from Kephart *et al* that alumina greatly increases carrier lifetime [7].

Despite the great increase in PL response however, no associated increase in the V_{OC} is noted. Figure 2 and table 1 show that the V_{OC}s of the two devices are virtually identical. Further work is required to optimize the structure and translate the large PL gains into device performance increases. Work is currently underway to add a highly doped p^+ layer behind the alumina layer. A p^+ layer is expected to bend the valence and conduction bands upward, allowing for hole extraction while reflecting electrons. This device structure is expected to further increase the carrier lifetime and consequently increase the open circuit voltage and photovoltaic conversion efficiency.

Although the electrical performance parameters have not yet increased in devices with alumina, figure 2 is evidence of an important milestone in integrating alumina into the device structure. While the J-V curves don't yet show any benefit to adding alumina at the back, they also show that it is possible to extract the current from the device with a very thin layer of Al_2O_3 deposited, which has been a challenge in the past. It is unclear whether the mechanism for current extraction is tunneling or a result of discontinuous Al_2O_3 coverage at a film thickness of 0.5nm. Further characterization and microscopy work is underway to clarify this issue.

As the alumina thickness increased from 0.25nm to 2nm, the corresponding PL signal also increased. The maximum PL signal was seen with an alumina thickness of 2nm, but at 0.5nm Al_2O_3 the PL signal still exceeded 70,000 counts/s. It is important to note that the devices with 0.5nm of alumina displayed the best electrical performance. As the alumina thickness grew past 1nm, the electrical parameters began to degrade. 2nm of alumina resulted in devices that were approximately 8% efficient. The device performance continued to decline as the alumina thickness grew past 2nm. This leads to the conclusion that while the alumina layer effectively passivates the back interface and greatly reduces recombination, either a very thin, or a patterned layer is required to allow for current extraction.

V. CONCLUSIONS

Previous work has shown that adding a thin layer of sputtered Al_2O_3 behind the absorber layer of CdSeTe/CdTe devices drastically improves the carrier lifetime. This work shows that high efficiency CdSeTe/CdTe devices can be fabricated with a very thin layer of Al_2O_3 deposited at the back of the device. PL measurements validate the earlier findings that alumina increases the carrier lifetime by reducing interfacial recombination. At this time, there has not been a commensurate improvement in the V_{OC} and further work is required to further optimize the structure and translate the gains in carrier lifetime into device performance. The addition of a highly P-doped layer behind the Al_2O_3 will cause upward bending of the valence and conduction bands at the back which should allow for increased extraction of holes, resulting in an increased V_{OC} and photovoltaic conversion efficiency.

ACKNOWLEDGEMENTS

The authors thank support from NSF's Accelerating Innovation Research, DOE's SIPS and NSF's Industry/University Cooperative Research Center programs. The authors are also grateful to Prof. James R. Sites and his graduate students for the help in the study with PL measurements.

REFERENCES

[1] N. M. Haegel, R. Margolis, T. Buonassisi, D. Feldman, A. Froitzheim, R. Garabedian, M. Green, S. Glunz, H.-M. Henning, B. Holder, I. Kaizuka, B. Kroposki, K. Matsubara, S. Niki, K. Sakurai, R. A. Schindler, W. Tumas, E. R. Weber, G. Wilson, M. Woodhouse, and S. Kurtz, "Terawatt-scale photovoltaics: Trajectories and challenges," *Science (80-.).*, vol. 356, no. 6334, 2017.

[2] W. Eric, "Exclusive: First Solar's CTO Discusses Record 18.6% Efficient Thin-Film Module," *Greentech Media*, 2015. [Online]. Available: http://www.greentechmedia.com/articles/read/Exclusive-First-Solars-CTO-Discusses-Record-18.6-Efficient-Thin-Film-Mod.

[3] S. K. David Brady, Steve Haymore, "First Solar, INC. Announces First Quarter 2014 Financial Results," Tempe, AZ, 2014.

[4] S. K. Steve Haymore, "First Solar, Inc. 2016 First Quarter Financial Results," Tempe, AZ, 2016.

[5] T. Kenning, "Buffett project's record low cost part of pricing 'trend', says First Solar," *pv-tech.org*, 2015. [Online]. Available: http://www.pv-tech.org/news/buffett_projects_record_low_cost_is_part_of_pricing_trend_says_first_solar.

[6] Munshi, Amit, J. Kephart, A. Abbas, J. Raguse, J. Beaudry, J. Sites, J. Walls, W. Sampath, and K. Barth, "Polycrystalline CdSeTe / CdTe Absorber Cells With," vol. 8, no. 1, pp. 310–314, 2018.

[7] J. M. Kephart, A. Kindvall, D. Williams, D. Kuciauskas, P. Dippo, A. Munshi, and W. S. Sampath, "Sputter-Deposited Oxides for Interface Passivation of CdTe Photovoltaics," *IEEE J. Photovoltaics*, pp. 1–7, 2018.