# An Improved Update Rate Baud Rate CDR for Integrating Human Body Communication Receiver

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*Abstract*— **Human Body Communication (HBC) utilizes the electrical conduction property of the human body to use it as a communication medium to connect devices around the body. The body channel has broadband characteristics, which enables wireline-like broadband communication. However, environmental interference proves to be a primary bottleneck in broadband HBC implementation. An integrating front-end followed by periodic sampling enables interference robust broadband HBC. The integration operation is sensitive to data, clock phase mismatch, requiring a Clock Data Recovery (CDR) loop for proper phase alignment between clock and data. This paper analyzes a Baud Rate Mueller-Muller (MM) CDR for an integrating front-end and utilizes the properties of the integration operation to propose a integrating MM CDR, which provides higher update rate than a traditional MM CDR. Simulation results show 1.67x higher clock data frequency offset tolerance of the integrating CDR compared to traditional MM CDR.**

Keywords—***Human Body Communication (HBC); Body Coupled Communication (BCC); Clock Data Recovery (CDR); Mueller-Muller CDR (MM CDR); Baud Rate CDR.***

## I. Introduction

Recently there has been a prolific growth in usage of small form factor wearable and implantable devices, which perform different sensing, actuation, computation, communication tasks in and around the body and form a network commonly known as the Body Area Network (BAN). State of the art BANs use radio waves to communicate between devices on the network. Since all these devices reside in close proximity to the body, the electrical conductivity of the human body can be utilized to use it as the communication medium between these devices. The use of human body to communicate between devices is commonly known as Human Body Communication (HBC) [1]. Since BAN devices are generally battery constrained due to its small form factor and a large portion of the system energy is consumed in communication, having an energy efficient communication medium can enhance the lifetime of such devices significantly. Compared to radio wave communication, HBC provides advantage in terms of higher energy efficiency and enhanced security of communication. Wireless radio communication requires the signal to be modulated to a higher frequency for transmission and demodulated at the receiver end. However, since the human body can act as a broadband channel [2], it can be used for broadband communication between devices. Enabling broadband communication enhances the energy efficiency of HBC significantly by eliminating the need of power hungry modulation and demodulation schemes. The primary bottleneck towards implementing energy-efficient broadband HBC is the environmental interference picked up due to the human body antenna effect [3]. An Integrating Dual Data Rate (I-DDR) receiver is proposed in [4]–[6], which uses time domain integration followed by sampling to achieve interference robust broadband operation. Since the data is sent in a broadband manner, to recover the transmitted data at the receiver end, it is necessary to sample the received data at the proper timing instants. This requires the receiver clock to maintain a certain phase relationship with the incoming data to recover it properly. This is achieved through a Clock Data Recovery (CDR) loop, which is widely used in traditional wireline receivers. However, since the receiver consists of an integrating front-end, the CDR operation varies from a traditional wireline CDR. In this paper, we analyze the feasibility of using the traditional baud rate Mueller-Muller CDR (MM-CDR) [7] for an integrating receiver. We also propose a baud rate CDR, which provides higher update rate than the traditional MM-CDR and can withstand more offset between data and clock frequencies.

The rest of the paper is organized as follows: Section II looks into the system level details of the I-DDR receiver highlighting the different blocks required for the CDR loop. Section III discusses the baud rate MM CDR in an integrating scenario and proposes the integrating MM CDR for integrating receivers. Section IV evaluates the proposed CDR performance in presence of data, clock frequency offset and data interference and Section V concludes the paper.

## II. Integrating Dual Data Rate (I-DDR) HBC Receiver

The integrating HBC receiver [4] front-end consists of an integrator followed by a sampler. The integrator provides differential output and has two phases of operation: reset and evaluate. The differential input voltage is integrated by discharging the parasitic capacitance of the output nodes through input dependent current sources. A dynamic regenerative latch based sampler is used to sample the integrator output (Figure 2). Since both the integrator and sampler have a reset phase, two such chains are required to process data at each phase of the clock resulting in dual data rate operation.

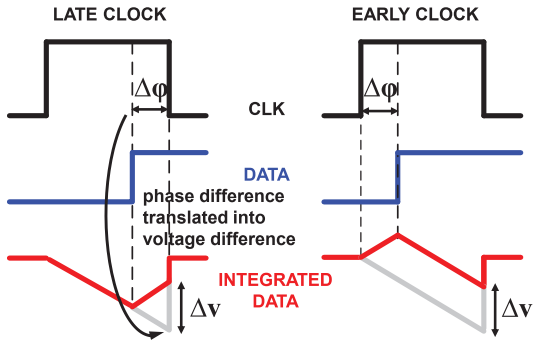


Figure 1: Integration operation enables converting the phase mismatch information between the integrating clock and data into voltage mismatch.

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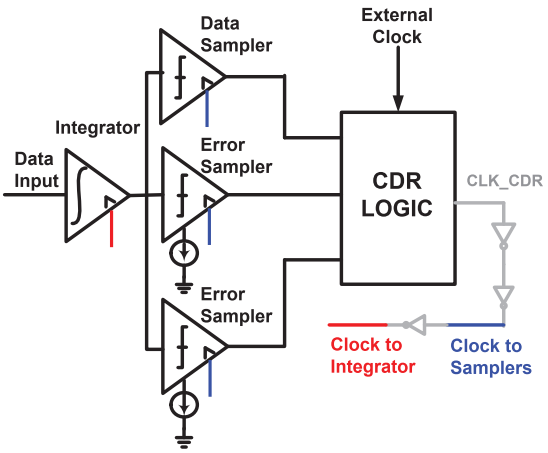


Figure 2: System Level Block Diagram of the I-DDR receiver. The CDR takes input from the data and error samplers to generate the phase locked clock.

It is necessary to time-align the beginning of the integration period and data period to maximize the integrated output. In the locked scenario, the phase difference between the clock and incoming data should be zero degrees. This will enable the integration of the data signal for the complete clock period and achieve maximum integrator output. Any phase offset between the clock and data will directly translate to a reduction in the integrated voltage margin as shown in Figure 1. The CDR loop maintains the proper phase relation between the data and the clock. A baud rate CDR is implemented which requires one sample per clock period and minimizes the power overhead of requiring a 2x clock. The Phase Detector (PD) in the CDR requires two extra error samplers to extract timing offset information as shown in Figure 2. The error samplers requires offset generation, which is done through current steering at the sampler outputs. The error sampler outputs and the data output is used to derive phase mismatch information to correct the phase of the clock. A single loop CDR is used to implement the phase tracking loop. The phase interpolator generates 16 different phases of the clock and the PD increments/decrements a counter based on early/late information to choose the proper clock phase for data and clock synchronization. It is also necessary to implement a glitch correction logic to ensure there are no clock glitches during transition between different phases (due to fast process and slow data rate). Figure 3 shows the internal details of the CDR logic blocks.

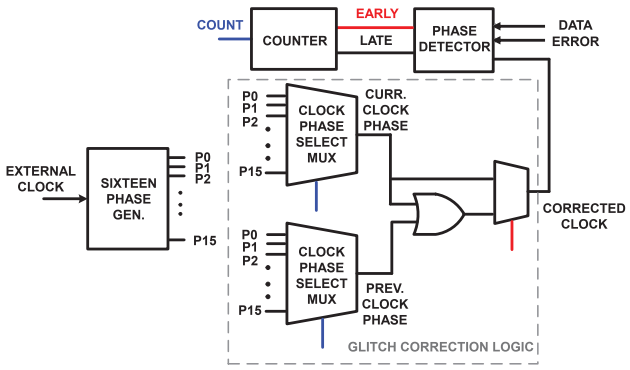


Figure 3: Internal logic diagram of the CDR. The phase detector creates early/late updates, which chooses the correct phase of the phase generator, and passed through a glitch correction logic to generate the system clock.

## III. Clock Data Recovery: Basic Principle

### *A. Mueller-Muller Baud Rate CDR: Non-Integrating Receiver*

The Mueller-Muller CDR requires one data sample per clock period to extract clock-data phase error information. The MM-CDR requires three samplers with thresholds set at +Vref, 0 , -Vref. These samplers provide the voltage information necessary for timing recovery. The CDR provides updates only on data transitions. For example, as shown in Figure 4a, during an 11-00 data transition a late sampling phase in the clock will result in the samplers sampling a voltage <+Vref but >0 (Errp = 0) for data bit 1 and a voltage <-Vref (Errn = 1) for data bit 0. The error information from these samplers along with the data bits can then be used to uniquely determine the early/late clock sampling information. Figure 4a also shows that all 1-0/0-1 data transition will not result in an update of clock information even if there is a mismatch in the clock and data phase. Only 25% of all possible data transitions can generate a phase error update information in case of a MM CDR in a non-integrating scenario. The locked phase of the CDR is free to wander depending on flatness of the received square wave pulse, thus resulting in no unique locking point.

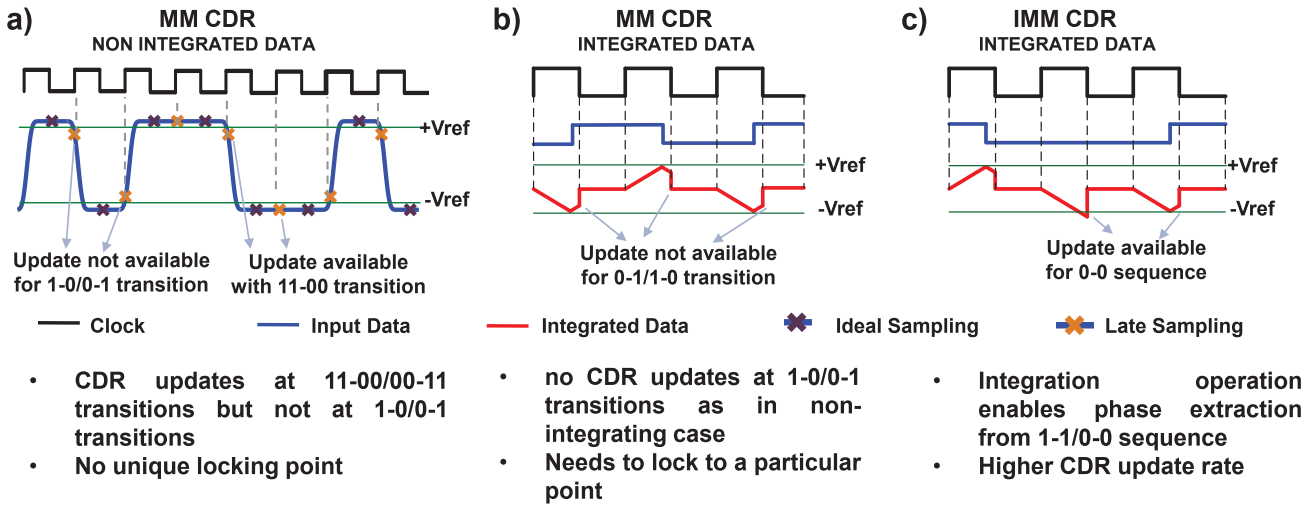


Figure 4: Comparison between CDR update information for :a) MM CDR for non-integrating scenario, b) MM CDR for an integrating scenario, c) Integrating MM CDR with higher update rate for an integrating front-end.

**Traditional Mueller-Muller CDR**

| D(n-2) | D(n-1) | D(n) | D(n+1) | E(n-1) | E(n) | Error Information |
|---|---|---|---|---|---|---|
| X | 0 | 1 | 0 | 0 | 0 | No Info |
| X | 0 | 1 | 1 | 0 | 1 | LATE |
| X | 1 | 0 | 0 | 0 | 1 | LATE |
| X | 1 | 0 | 1 | 0 | 0 | No Info |
| 0 | 0 | 1 | X | 1 | 0 | EARLY |
| 1 | 0 | 1 | X | 0 | 0 | No Info |
| 0 | 1 | 0 | X | 0 | 0 | No Info |
| 1 | 1 | 0 | X | 1 | 0 | EARLY |

$$Errp = 1\ if\ v > +V_{ref}, 0\ if\ v < +V_{ref}$$
$$Errn = 1\ if\ v < -V_{ref}, 0\ if\ v > -V_{ref}$$
$$E(n) = Errp(n) \oplus Errn(n)$$
$$D(n) = current\ data\ bit, D(n-1) = previous\ data\ bit$$

Figure 5: MM-CDR truth table for an integrating receiver front-end. A 0-1 or 1-0 data transition does not necessarily contain phase error information and is dependent on the adjacent bits. This reduces the update rate of the CDR.

### *B. Mueller-Muller Baud Rate CDR: Integrating Receiver*

The integrated output is a function of both the input data and integration duration for an integrating front-end. So any timing offset between the data and clock is directly transferred into voltage information (Figure 1). As a result, the error information for a particular data transition is also dependent on the adjacent bit sequence. It can be seen from the truth table in Figure 5, half the 1-0 or 0-1 data transition results in an update information, depending on the adjacent bit pattern (Figure 4b). So the traditional MM CDR for an integrating front-end does not utilize the extra information provided by the integration operation and the update rate is still 25%. It is interesting to note that although integration converts phase information to voltage, it does not provide unique early/ late information. Hence it is still necessary to look into two consecutive data bits and error information to extract mismatch information.

### *C. Proposed Baud Rate CDR: Integrating Receiver*

For an integrating front-end, the integration operation converts the phase mismatch into voltage domain mismatch. Hence it is possible to extract phase error information even from a scenario when there is no data transition, as can be seen in Figure 4c and the truth table in Figure 6. This is possible as

**Integrating Mueller-Muller CDR**

| D(n-2) | D(n-1) | D(n) | D(n+1) | E(n-1) | E(n) | Error Information |
|---|---|---|---|---|---|---|
| X | 0 | 0 | 0 | 1 | 1 | No Info |
| X | 0 | 0 | 1 | 1 | 0 | LATE |
| X | 0 | 1 | 0 | 0 | 0 | No Info |
| X | 0 | 1 | 1 | 0 | 1 | LATE |
| X | 1 | 0 | 0 | 0 | 1 | LATE |
| X | 1 | 0 | 1 | 0 | 0 | No Info |
| X | 1 | 1 | 0 | 1 | 0 | LATE |
| X | 1 | 1 | 1 | 1 | 1 | No Info |
| 0 | 0 | 0 | X | 1 | 1 | No Info |
| 1 | 0 | 0 | X | 0 | 1 | EARLY |
| 0 | 0 | 1 | X | 1 | 0 | EARLY |
| 1 | 0 | 1 | X | 1 | 0 | No Info |
| 0 | 1 | 0 | X | 0 | 0 | No Info |
| 1 | 1 | 0 | X | 1 | 0 | EARLY |
| 0 | 1 | 1 | X | 0 | 1 | EARLY |
| 1 | 1 | 1 | X | 1 | 1 | No Info |

Figure 6: Integrating MM-CDR (IMM-CDR) truth table for integrating receiver. The early-late information is obtained by looking at two data bits (D(n-1),D(n)) and two error bits (E(n-1),E(n)). The update rate is higher compared to a traditional Mueller-Muller CDR working on integrated data.

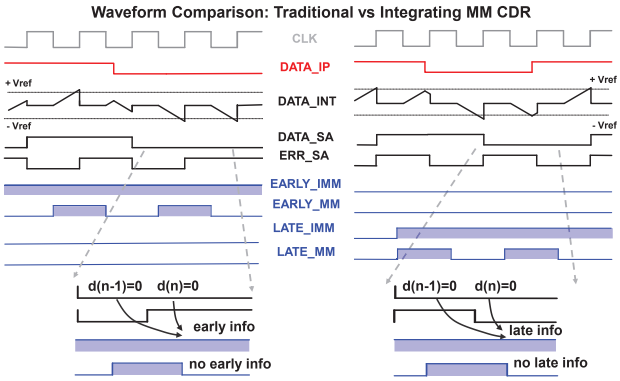


Figure 7: Comparison between traditional MM CDR and integrating MM CDR under integrating conditions. It can be seen from the data sequence that the integrating MM CDR provides update for certain bit sequences, which is not provided by the traditional MM CDR, resulting in a higher update rate.

integration operation enables transfer of information from adjacent bits into the current bit period if there is a phase mismatch between the data and clock. Hence, by taking advantage of the phase-voltage mismatch transfer it is possible to increase the update rate of an integrating MM-CDR compared to a traditional MM CDR as can be seen from the scenario shown in Figure 7. The phase error information is derived from the current data bit (D(n)), previous data bit (D(n-1)), current error (E(n)) and previous error (E(n-1)) information. Although there is possibility of extracting Early/Late update information for all possible combinations of current and previous data bits, it occurs 50% of the time for each combination and is dependent on the adjacent data bits. Hence, the overall update rate of the CDR increases to 50% in this scenario.

### *D. CDR Closed Loop Design: Loop Stability*

The generation of early/late clock information from voltage mismatch is dependent on the offset provided to the error samplers. Since the integrated output is dependent on the clock-data phase mismatch, hence it is possible to control the voltage offset of the error samplers such that the clock is able to lock to a unique phase introducing a *dead-zone* in the closed loop operation. Higher offset values provide more noise immunity but results in frequent generation of updates, reducing loop stability. The offset value to ensure phase locking is dependent on the resolution of clock phases provided to the phase interpolator.

### *E. Glitch correction in Clock*

Since we are using the human body as a broadband channel for communication between devices, the data rate is limited by the body channel bandwidth of around 100MHz [8]. Also the required data rate for most HBC applications is in the range of a few Mbps. However at scaled technology nodes such as 65nm the intrinsic delays of gates are orders of magnitude faster than the MHz range. Hence, the clock phases generated from the phase generator has slew rates which are orders of magnitude lesser than the delay between them, when the operating clock rate is in MHz. This creates a glitch in the clock waveform whenever there is switching between multiple clock phases due to CDR updates, which is not present when the delay between consecutive phases are of the same order as the clock slew rates. Hence a glitch correcting logic (Figure 3) is implemented to prevent spurious glitches on the clock waveform during transition between different clock phases.

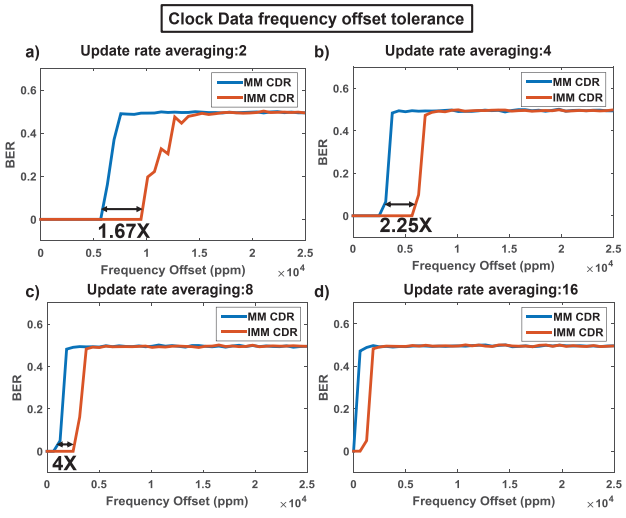


Figure 8: Simulation results showing the data and clock frequency offset tolerance of the traditional and integrating MM CDR for different averaging of early/late update rates. The integrating MM CDR shows higher offset tolerance due to its higher update rate compared to the traditional MM CDR.

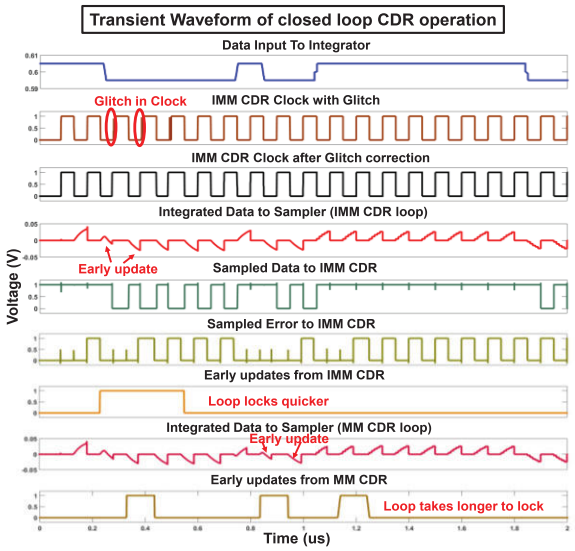


Figure 9: System level transient waveforms of the closed loop CDR operation. The integrating MM CDR (IMM-CDR) generates early updates back to back which helps in locking the loop quicker compared to the traditional MM CDR.

## IV. RESULTS

The proposed CDR loop has been implemented in TSMC 65nm technology and the system performance evaluated in Cadence AMS environment. A MATLAB based simulation model of the system, cross validated with AMS simulations, is developed to calculate the BER performance for large number of input bits under different data, clock frequency offset scenario and presence of different amplitude interferences.

### *A. Update Rate*

The update rate of the integrating MM CDR (IMM-CDR) and the traditional MM CDR for an integrating receiver is evaluated by applying a random bit stream as input and calculating the number of early/late updates in open loop, without adjusting the clock phase. The update rates are calculated over $4x10^6$ bits of data. The integrating MM CDR shows an update rate for 0.501 for early and 0.5 for late updates. On the other hand the traditional MM CDR provides an update rate of 0.25 for early and 0.25 for late updates, which corresponds with the theory.

### *B. Frequency Offset Tolerance*

An offset between data and clock frequency is introduced to check the offset tracking tolerance of the CDR by measuring the BER under different offset scenarios. As can be seen from Figure 8 the integrating MM CDR with higher update rate provides higher data-clock frequency offset tolerance compared to the traditional MM CDR. The update rate of the CDRs are also controlled by taking an early/late update decision only after a certain number of consecutive early/late updates are generated. Figure 8 also shows that an update rate average of four (four consecutive early/late signal generates an update) shows the best Bit Error Rate (BER) performance.

### *C. Interference Tolerance*

The interference tolerance of the integrating MM CDR is simulated under different signal to interference ratio (SIR) condition and evaluating its BER performance. The ratio of interference and data frequency is also varied to measure the interference robustness of the CDR loop, since interference rejection is most optimum when the interference frequency is an integral multiple of data rate. Simulation results show that the CDR can tolerate up to -21dB SIR even when the interference frequency has 25% offset compared to the data frequency.

### *D. Closed Loop System Level Functionality*

The transient waveforms for the CDR closed loop operation is shown in Figure 9. The mismatch between the initial phase of the clock and the data creates an early update signal, which changes the selected clock phase to reduce the phase mismatch. The glitch correction logic ensures the removal of any glitch from the resultant clock waveform, which would have otherwise existed due the clock phase update. The error sampler offsets are chosen to introduce a dead zone in the control loop and hence the loop gets locked to a steady state phase as seen from the waveforms. It can also be seen from the waveforms that the integrating MM CDR locks to a steady state faster than the traditional MM CDR.

## V. CONCLUSION

This paper analyzes the operation of a MM CDR for an integrating front-end (as found in Broadband HBC) and proposes a integrating MM CDR which utilizes the integrating front-end to provide higher update rate compared to a traditional MM CDR. The integrating MM CDR shows > 5000 ppm clock-data frequency offset tolerance, which is 1.67X higher compared to a traditional MM CDR.

## VI. ACKNOWLEDGEMENTS

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