# Nonvolatile magneto-electric field effect transistors for spintronic memory and logic

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## INTRODUCTION:

Here we describe the development of magneto-electric transistor devices to address the need for non-volatile, ultra-low power, ultra-fast, and scalable memory and logic.

There has been an evolution in thinking, as to what should be the target magneto-electric devices as CMOS 'plug-in' replacement logic and memory. The earliest magneto-electric devices were based on a magnetic tunnel junction structure [1,2], which consists of two ferromagnetic (FM) layers separated by a non-magnetic insulator where the device resistance is determined by the relative orientation of the magnetization of the two FM layers. The magnetization of the free layer is exchange coupled to the $Cr_2O_3$ (or other magneto-electric) interface magnetization (Figure 1). A bias voltage applied across the $Cr_2O_3$ layer reverses the interface magnetization, which in turn switches the magnetization of the free layer [3,4].

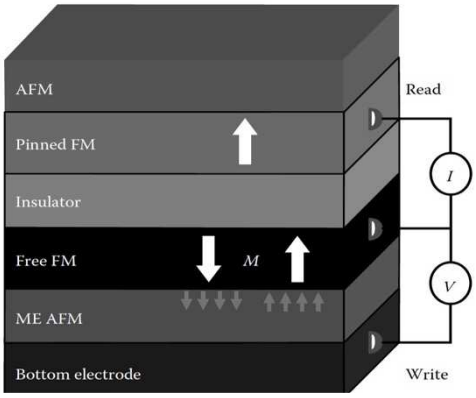


FIGURE 1. VOLTAGE-CONTROLLED MAGNETIC TUNNEL JUNCTION WHERE FREE MAGNETIC LAYER MAGNETIZATION IS CONTROLLED BY A MAGNETOELECTRIC INTERFACE, SEPARATING THE READ AND WRITE ASPECTS OF THE DEVICE [1,5].

More recently attention [5-9] has shifted to the magneto-electric transistor (the ME-spinFET), where the most basic structure is outlined in Figure 2. Magneto-electric transistor schemes are based on polarization of the semiconductor channel, by the boundary polarization of the magneto-electric gate. The advantage to the magneto-electric field effect transistor is that such schemes avoid the complexity and detrimental switching energetics associated with exchange-coupled ferromagnets. Spintronic devices based solely on the switching of a magneto-electric, will have a switching speed will be limited only by the switching dynamics of that magneto-electric material and above all are voltage controlled spintronic devices. Moreover, these magneto-electric devices promise to provide a unique field effect spin transistor (spin-FET)-based interface for input/output of other novel computational devices. This is spintronics without a ferromagnet, with faster write speeds (<20 ps/full adder), at a lower cost in energy (<20 aJ/full adder), greater temperature stability (operational to 400 K or more), and scalability, requiring far fewer device elements (transistor equivalents) than CMOS.

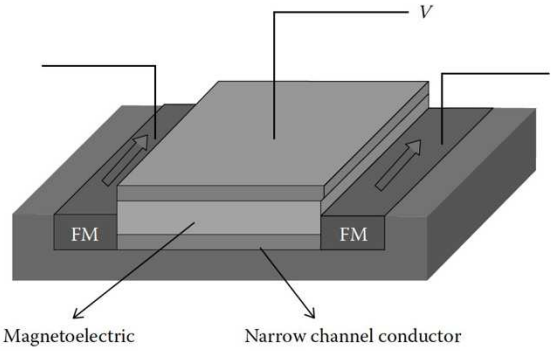


FIGURE 2. THE BASIC TOP GATED MAGNETO-ELECTRIC SPIN-FET WITH A FERROMAGNETIC (FM) SOURCE AND DRAIN. THE THIN CHANNEL CONDUCTOR/SEMICONDUCTOR (BLUE) COULD BE ANYTHING REALLY, SUITABLE TO THE TASK (GRAPHENE, INP, GASB, PBS, $MoS_2$, $WS_2$, $MoSe_2$, $WSe_2$, ETC.) [5,7].

Magneto-electric field effect transistor device concepts that emphasize the value of using a narrow channel conductor, with strong spin-orbit coupling (SOC), will have, however, enhanced on/off ratios and even greater functionality.

## THE ANTI-FERROMAGNET SPIN-ORBIT READ (AFSOR) LOGIC DEVICE

The anti-ferromagnet spin-orbit read (AFSOR) logic device structure (Figure 3) has interesting advantages: the potential for high and sharp voltage 'turn-on'; inherent non-volatility of magnetic state variables; absence of switching currents; large on/off ratios; and multistate logic and memory applications. The design will provide reliable room-temperature operation with large on/off ratios ($>10^7$) well beyond what can be achieved using magnetic tunnel junctions [10,11]. Again, the core idea is the use of the boundary polarization of the magneto-electric to spin polarize or partly spin polarize a very thin semiconductor, ideally a 2D material, with very large spin orbit coupling.

If the semiconductor channel retains large spin orbit coupling, then the spin current, mediated by the gate boundary polarization, may be enhanced and, to some extent, topologically protected. The latter implies that each spin current has a preferred direction, as indicated in Figure 3.

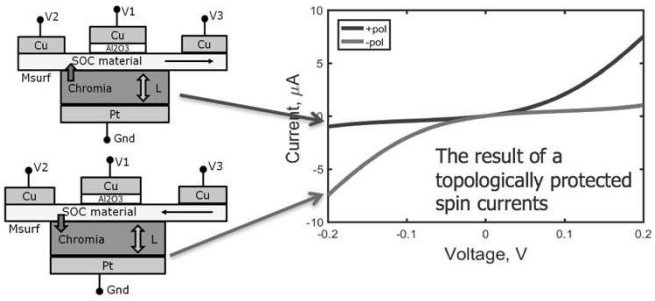


FIGURE 3. AT LEFT, THE SCHEME OF ANTI-FERROMAGNET SPIN ORBIT READ (AFSOR) LOGIC. A) THE STATE WITH POSITIVE V1 APPLIED AND THE SURFACE OR INTERFACE MAGNETIZATION OF THE MAGNETO-ELECTRIC GATE MSURF POINTING UP. B) THE STATE WITH NEGATIVE V1 APPLIED AND SURFACE MAGNETIZATION MSURF POINTING DOWN. AT THE RIGHT, SOURCE TO DRAIN CURRENT VERSUS VOLTAGE. FROM [10,11]

## THE MAGNETO-ELECTRIC SPIN-FET MULTIPLEXER

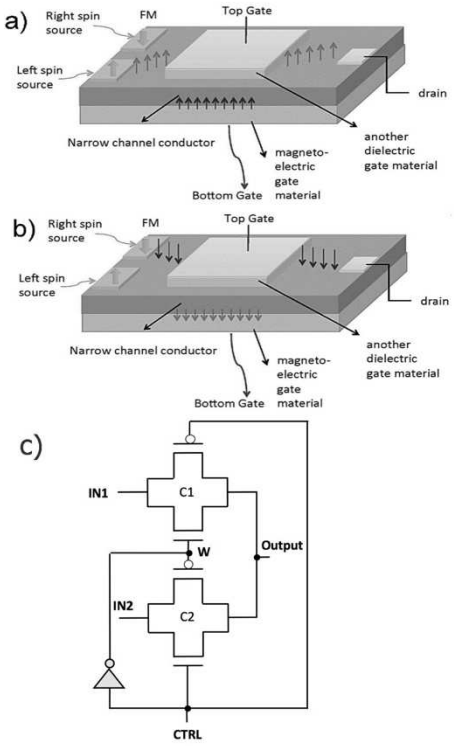


FIGURE 4. THE BASIC NONVOLATILE ME SPINFET MULTIPLEXER (SPIN-MUX), WITH FERROMAGNETIC SOURCE CONTACTS. THE THIN CHANNEL CONDUCTOR/SEMICONDUCTOR WOULD BE POLARIZED (A) UP OR (B) DOWN. THE CMOS EQUIVALENT IS SCHEMATICALLY INDICATED IN (C). FROM [10,11].

There is a variant of Figure 3, where inversion symmetry is not as strictly broken, that leads to a nonvolatile spintronics version of multiplexer logic (MUX). The magneto-electric spin-FET multiplexer (Figure 4) also exploits the modulation of the spin-orbit splitting of the electronic bands of the semiconductor channel through a "proximity" magnetic field derived from a voltage-controlled magneto-electric material. Here, by using semiconductor channels with large spin-orbit coupling, we expect to obtain a transverse spin Hall current, as well as a spin current overall. Depending on the magnitude of the effective magnetic field in the narrow channel, we anticipate two different operational regimes. Like the AFSOR magneto-electric spin FET, the magneto-electric spin-FET multiplexer in Figure 4 uses spin-orbit coupling in the channel to modulate spin polarization and hence the conductance (by spin) of the device. There is a source-drain voltage and current difference, between the two FM source contacts, due to the spin-Hall effect when spin-orbit coupling is present. This output voltage can be modulated by the gate or gates, which influences the spin-orbit interaction in the channel especially when it is both top and bottom gated especially. The spin-Hall voltage in the device can be increased by using different FMs in the source and drain. To increase the spin fidelity of current injection at the source end, one could add a suitable tunnel junction layer (basically a 1nm oxide layer) between the magnetic source and the 2D semiconductor channel. This latter modification would result in diminished source-drain currents though.

## SUMMARY

The challenges in pushing forward these technologies extends not only to the fabrication and characterization of a new generation of nonvolatile magneto-electric devices, but also to ascertaining the optimal implementation of CMOS plug in replacement circuits.

## ACKNOWLEDGEMENTS

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