Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits

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***Abstract*—A Verilog-A based model for the magneto-electric field effect transistor (MEFET) devices is implemented and a variety of logic functions based on the device are proposed. These models are used to capture energy consumption and delay per switching event and, to benchmark MEFET with respect to CMOS. Single source MEFET device can be used for conventional logic gates like NAND, NOR, inverter and buffer and more complex circuits like the full adder. The dual source MEFET is an enhanced version of the MEFET device which functions like a spin multiplexer (spin-MUXer). Circuits using MEFET require fewer components than CMOS to generate the same logic operation. These devices display a high on-off ratio unlike many magneto-electric devices, and they operate at very low voltages resulting in lower switching energy. Benchmarking results show that these devices perform better in terms of energy and delay for implementing more complex functions rather than the basic logic gates.**

Keywords—Magneto-electric; ME-MTJ; narrow channel; 2D; MEFET; benchmarking; CMOS; proximity effect; chromia.

I. Introduction

Many spintronic devices have been proposed since early in the millennium. One of the candidates is the magneto-electric spin field effect transistor (MEFET) proposed in [1-4]. This device is an enhancement to the spin transistor proposed by Datta and Das [5]. In the original spin transistor, the applied gate voltage controls the channel spin precession, through electric field generated due to the spin orbit dependent Rashba effect. This results in a change in the drain to source (I_{DS}) current which represents the state variable of the device. Verilog-A based models have previously been proposed for the Rashba effect based SpinFET transistors in [6-8]. Unfortunately, this effect is weak making it difficult for the realization of an effective room temperature Datta-Das transistor.

The MEFET is different from the conventional spin transistor as the channel is polarized by a ME chromia (Cr_2O_3) layer through proximity effect. Depending on the direction of orientation of chromia spin vectors, the channel spin vectors are oriented in either 'up' or 'down' direction. This device works on voltages around 100 mV, possesses inherent memory due to the non-volatile AFM order of the ME and has a sharp turn-on voltage [9-10]. This device also has an on-off ratio of ~ 10^6 reported in [11], which is comparable to CMOS and advantageous for implementing logic functions. This device also features an extremely low switching delay of around 3 ps.

Two versions of the MEFET device are envisioned with a single and dual source MEFET. Both of these structures allow us to capitalize on the devices' beneficial features, while making significant improvements to operational circuit capabilities over those of CMOS. The previously proposed ME device i.e. the magneto-electric magnetic tunnel junction (ME-MTJ) utilizes voltage-controlled exchange bias in heterostructures using a ME antiferromagnet (AFM) exchange coupled with a ferromagnetic (FM) layer. Such devices can be used to design CMOS like functions and memory devices, due to their logic capabilities and inherent non-volatility respectively [12-22].

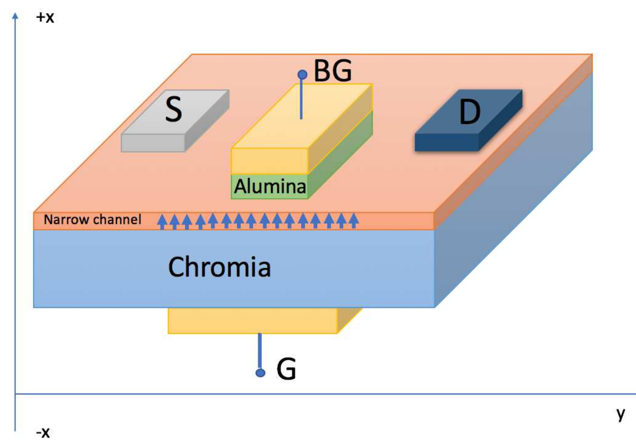


Figure 1: Single source MEFET device structure.

The ME-MTJ and its derived devices have been modelled in MATLAB and Verilog-A and circuit options have been presented previously in [22-23]. Furthermore, a device-to-circuit level coupled simulation framework for the ME-MTJ based devices has been proposed in [16] and in-depth analysis of these devices has been presented in [24]. The ME-MTJ based devices have been benchmarked with respect to CMOS and other device architectures. However, due to the large

exchange coupling delays for switching the FM layer, the ME-MTJ has a poor performance. In comparison, the MEFET performs 10x better due to instantaneous switching of the FM layer. They also have significantly better on-off ratios (~10^7) compared to the ME-MTJ with its on-off ratio of just 10x.

II. MEFET Device Construction

The single source version, shown in Figure 1, is a 4-terminal device with source ("S"), drain ("D"), gate ("G") and back gate ("BG") terminals [25]. The device may have either a source that is a fixed spin FM polarizer with chromia acting as the channel spin polarizer or that the chromia simply acts on a channel with large spin-orbit coupling. The channel assumed for simulations is a p-type tungsten diselenide (WSe_2) which is a single layered semiconductor with high hole mobility of ~2100cm^2/Vs and on-off ratio of ~ 10^9 [11]. There are two dielectrics, one at the top i.e. alumina, the other is chromia, at the bottom of the channel.

The spin polarized current is injected into the channel through the source terminal and polarized by the chromia, resulting in a spin polarized current at the drain. Both 'up' and 'down' spins can be detected at the drain. The "BG" terminal is grounded and the input voltage is applied across the "G" and "BG" terminals to create a vertical field across the chromia layer and to align its spin vectors either along +x or –x axis, depending on the polarity of voltage applied. The state of the device is read using a clocked CMOS active pull up device. The clocking of this component reduces the leakage drastically.

The second device i.e. the spin-MUXer is a 5-terminal device with dual sources ("S_1" and "S_2") with opposite spin polarizations, drain ("D"), gate ("G") and back gate ("BG") terminals. "S_1" and "S_2" have fixed 'up' and 'down' spin respectively. Two NMOS transistors are used to control spin injected into the device. A MEFET device can also be used as the enable switch. The device structure is otherwise similar to the single source version.

III. Verilog-A Model

The modeling scheme for the MEFET device is shown in Figure 2. $R_{channel}$ is the resistance across the two-dimensional (2D) narrow channel and an additional resistance R_{int} is added in series to the $R_{channel}$ to define the boundary conditions for switching.

There are two aspects of the model developed here: (a) ME control of the channel spin polarization which is based on the proximity induced polarization in the narrow 2D channel and the (b) spin inject/detect function which is based on the injection into the source and then detection at the drain.

A. *Magneto-electric control of the channel spin polarization*

In this subsection, the gate voltage modulation is taken into account. The ME layer induces spin polarization in the channel due to the proximity of magnetic atoms or a magnetically ordered substrate [4]. Chromia is highly resistive [26] serving as a dielectric gate to the 2D channel. It also has high interface polarization which can be controlled by voltage [1,4,15,27,28]. When voltage is applied across the "G" and "BG" terminal, this is equivalent to charging of the ME capacitor. The computed delay element is associated with the boundary magnetization between the ME film and the interface of the channel. The switching time of the MEFET device is limited only by the switching dynamics of the ME.

B. *Spin detect/inject function*

The charge current is injected into the source and the boundary magnetization between chromia and channel gives rise to damped precession of the spins. The spin current is then detected at the drain through a pull up component (Figure 2).

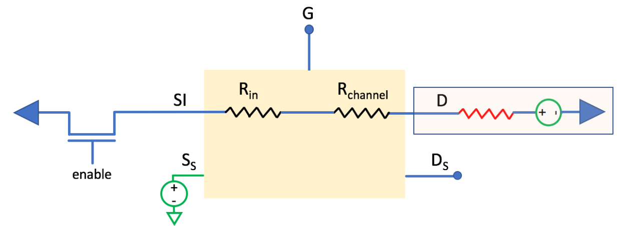


Figure 2: Single source MEFET modeling scheme. Rin and Rchannel represents the internal and channel resistance of the device.

For the single source version, additional spin state terminals ("D_S" and "D_S") are added to validate the spin state injected/detected at the source/drain terminals as shown in Figure 2. The 'up' and 'down' spins are represented by constant voltages sources with '+1 V' and '-1 V' respectively at the "S_S" terminal. To model the dual source MEFET, three additional terminals are included to detect the state of spin current injected into the sources i.e. ("S_{1S}" and "S_{2S}") and the corresponding spin current detected at the drain terminal ("D_S"). The model is developed such that, before the simulation is run, the injected spin orientation can be selected, making the model flexible to obtain various logic functions.

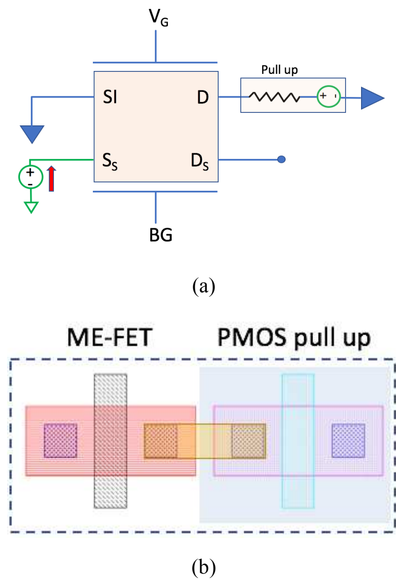
IV. Circuit Simulation

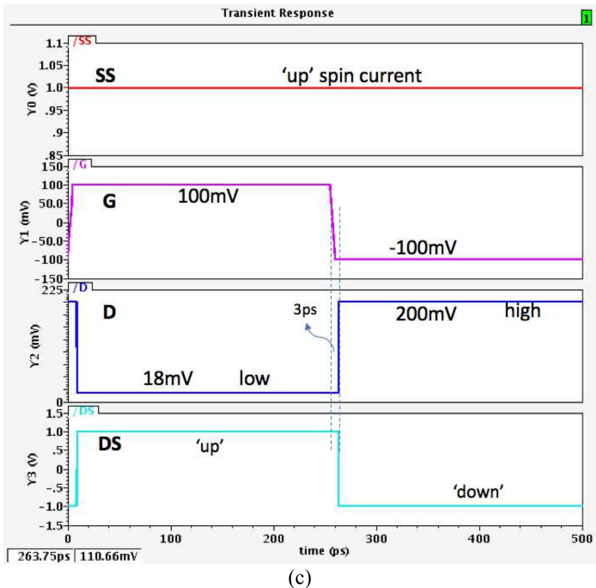
Using the MEFET devices, and their memory and spin properties, we can create conventional logic devices. Transient simulations have been performed using Spectre at a technology equivalent to the 15-nm node.

A. *Single Source MEFET Device*

The single source version behaves like an inverter/buffer depending on the direction of spins injected into the source. Figure 3 shows the circuit schematic, layout and transient simulation of the MEFET inverter. As the gate voltage exceeds the positive switching threshold of chromia i.e. +V_{ME}, the spin vectors are oriented in 'up' direction, orienting the spin vectors in the channel along the +x-axis. Thus, the spin state detected at the drain end is along +x axis i.e. 'up'

direction since the channel is conductive, resulting in a low voltage at the output (18 mV) after a delay of 3 ps.





(c)

Figure 3: (a) Circuit schematic, (b) layout and (c) transient simulations of the MEFET inverter.

The full adder can be made from 15 devices (Figure 4), in around a third of the minimum number of transistors needed for the CMOS equivalent. This does not include the reset function which will contribute a small percentage to the system delay and energy costs. However, the path from carry-in to carry-out is just one gate, so assuming the A and B states can be pre-loaded, the signal path through the adder is defined by a single gate. Leakage is defined by the number of gates and the clocking details.

For multi-stage circuit design, reset functionality is needed to reset the state of the chromia spin vectors. At the beginning of each cycle, the circuit path is reset. The output voltage for the logic level '1' and '0' is 133 mV (high) and 10 mV (low) respectively (Figure 5(a)). The layout of this circuit is 674 F^2 (Figure 5(b)) compared to an area of 1590 F^2 for a CMOS based full adder [29,30].

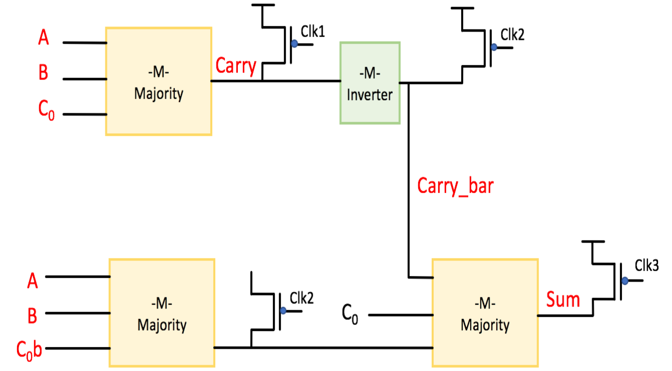
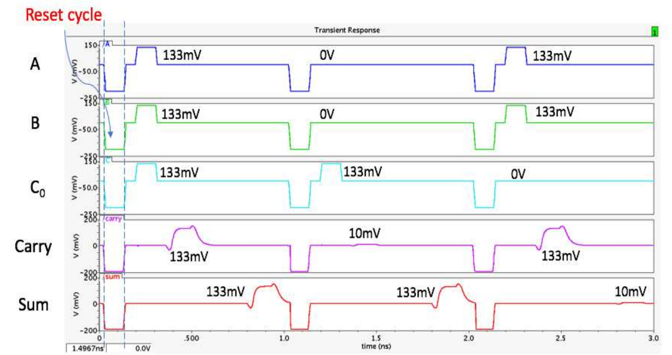
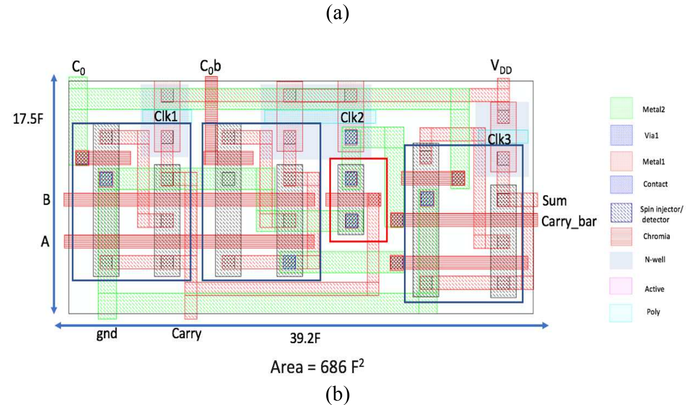


Figure 4: Circuit schematic of the single source MEFET 1-bit full adder.



(a)



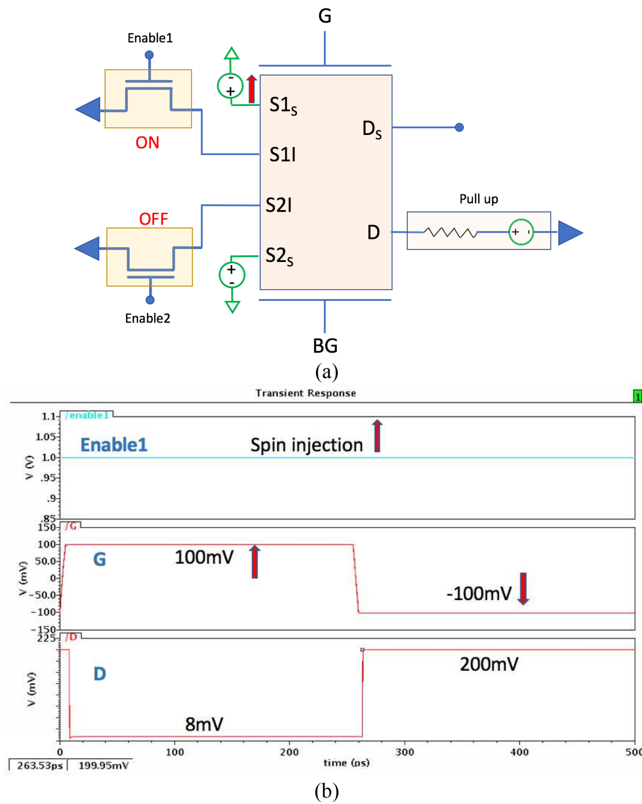
(b)

Figure 5: (a) Transient simulation results and (b) layout of the single source MEFET 1-bit full adder.

There are effectively two stages of the device that create a low resistance path between the output and only one of the inputs. The spin-MUXer selects either the 'up' or 'down' spin depending the polarity of applied gate voltage. In Figure 6, only 'up' spin injected is enabled and the output goes high when the polarity of gate voltage is negative.

Inverter/buffer like functionality can also be derived from the MUXer. It is observed that the circuit shown in Figure 6(a) behaves like an inverter. Similarly, a buffer like operation can be obtained by injecting 'down' spins.

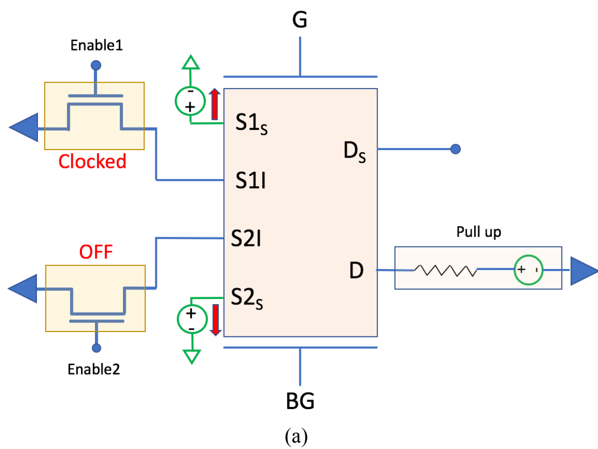
B. *Dual Source MEFET Device*



(a)

(b)

Figure 6: (a) Circuit schematic and (b) transient simulations of the dual source MEFET based spin-MUXer for ‘up’ spin injection.

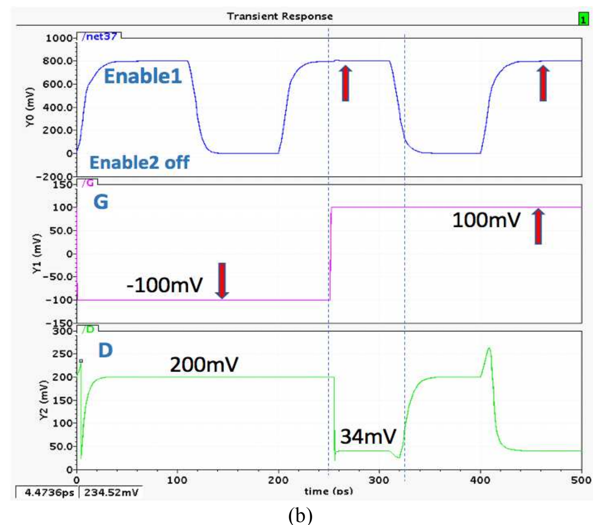


(a)

Figure 7 shows the circuit schematic and transient simulation results of the dual source MEFET NAND gate. The function can be obtained using a single device compared to two components required in the single source version. The ‘up’ spin injected is clocked whereas the ‘down’ spin injection is disabled. When gate voltage is low indicating that the chromia spin vectors are aligned in ‘down’ direction, the output voltage goes high (200 mV) since the channel is non-conducting. When the gate voltage is high, the output voltage goes low (34 mV) for ‘up’ spins injection into the source.

V. MEFET Benchmarking

It is important to consider how circuits constructed using the MEFET compare to other charge and non-charge based devices, especially concerning the energy-delay product [16-18]. In addition, the capacity of the circuits to be scaled up is important if any new technology is to compete with CMOS. The MEFET devices are thus benchmarked with respect to CMOS devices in Figure 8. The switching speed for the stand-alone MEFET device is between 3 ps and 20 ps, giving a range of possible energy and delays. The energy can be attributed to the leakage components due to the CMOS pull-up which is required to read the output state of the device.



(b)

Figure 7: (a) Circuit schematic and (b) transient simulation results of the dual source MEFET NAND gate.

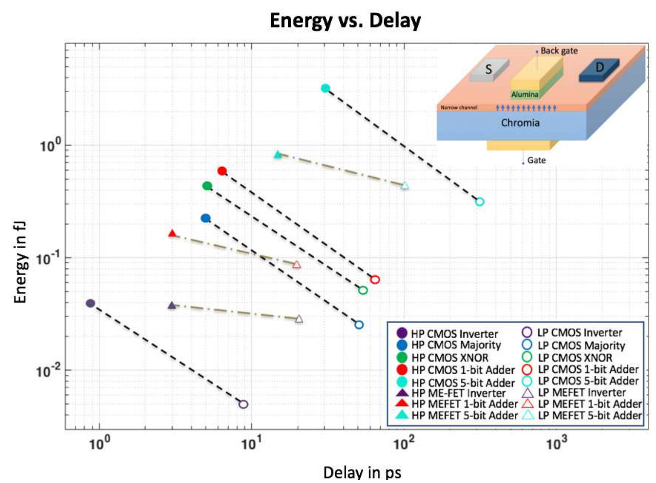


Figure 8: The single magneto-electric spin transistor (triangles) is compared to high performance (filled circles) and low performance (open circles) CMOS. The switching speed is estimated to lie between 3 ps (filled triangles) and 20 ps (open triangles) for an MEFET device, giving a range of possible energy versus delay estimates (dashed-dot lines).

For inverter operation, CMOS has better performance than the MEFET. However, for more complex circuits, such as the 1-bit full adder, MEFET is more competitive. The CMOS full adder requires up to 36 components. However, the MEFET based adder has better energy delay performance, as it requires only 15 components including read and reset circuitry (Figure 8).

VI. Limitations of this work

This work presents a model for the MEFET device to simulate the logic functions derived from this device. One of the major limitation of this work is the theoretical models for the spin injection are not included. It is assumed that the current injected into the system is capable of switching the magnetization of the FM assuming spin transfer torque effect and the spin injection efficiency is 100%. Although these models are necessarily of limited accuracy, they are nevertheless important at such an early stage of device implementation, as it is important to see how the device can be used for logic operations and how it compares with CMOS, which is the focus of this paper.

Conclusion

A variety of logic function derived from the MEFET devices have been verified for functionality using the custom designed Verilog-A models. These devices exploit voltage-control of spin-polarization that has been induced via interface exchange in a thin semiconducting channel. These devices offer non-volatility, compact circuit footprint, faster write speeds (~3 ps) at lower cost in energy (~aJ) making the MEFET transistors of considerable interest for post-CMOS technology. Benchmarking results indicate that these devices have better performance in terms of energy and delay for implementing complex logic functions compared to CMOS.

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