An Analog QAM Demodulator for Millimeter-Wave Communications

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***Abstract*—Recent interest in wide-band multi-giga-bit-per-second wireless communications over mm-wave bands has created both new opportunities and design challenges. The realization of such technologies including multi-giga-samples-per-second data conversion and digital signal processing systems is extremely challenging. In this brief, we propose a fully analog QAM demodulator as a step towards eliminating the power hungry and ultra-high speed digital components. The proposed low-complexity, low-overhead solution is shown to be robust against analog processing errors.**

EDICS Category: COMM110, COMM200

I. Introduction

THE need for high-throughput wireless communications continues to grow as new applications such as virtual reality and multi-gigabit-per-second (multi-Gbps) point-point wireless communications emerge. Indeed, bandwidth expansion no longer provides a viable solution for the crowded bands below 30 GHz. On the other hand, spectrally efficient high-order modulations such as 256-QAM exert very stringent requirements on the design. Consequently, migration to the underutilized mm-wave spectrum (30-300 GHz) is now being considered as the next frontier for future wireless systems [1], [2].

Nevertheless, mm-wave communications is not without its own challenges. High frequency path loss (as predicted by the Friis equation) is the first roadblock that is usually addressed by deploying high gain antenna arrays. The second challenge lies on the excessive speed and power dissipation of digital signal processing backend.

Over the past few decades, the transition from analog to digital processing has enabled the designers to implement sophisticated, precise, and flexible signal processing that is not easily realizable in analog domain. High rate digital processing at multi-Gbps, however, entails several challenges on the preceding mixed-signal unit. In particular, the high bitwidth requirement of a spectrally efficient modulation such as 16 or 64-QAM mandates data converters with high resolution (e.g., $\geq$10) and high sampling rates (e.g., 10+ gigasamples-per-second). The design of such high resolution high sampling-rate data converters, if at all possible, requires massive amount of parallelism, thereby exacerbating power consumption. On the digital data-processing front, the extreme data rates demand a high-level of parallelization. The latter requires logic replication which in turn increases the chip power consumption and area. Parallelization orders of 8 or more are common in current mm-wave designs that support IEEE 802.15.3c/802.11ad standards for transmission over channels with bandwidths up to 2 GHz. Some of the aforementioned design challenges are highlighted in [3], [4], [5] and the references therein. Digital design tends to become even more challenging as researchers consider Tera-bit wireless communication over Tera-Hz bands where the available bandwidth, and hence the required sampling rate, are expected to be even higher [6].

High-order, multi-GBaud QAM transmission has been studied primarily in the context of optical communications (see, [7], for example). The existing work has been traditionally using fully digital QAM demodulation schemes. The work in this brief explores an alternative route - namely QAM demodulation in analog domain - with the following contributions. First, the reduced complexity of the analog demodulator makes it suitable for wireless systems where power consumption is a much more critical concern compared to the optical communication counterparts. Second, the proposed design makes QAM demodulation independent of fine gain tuning. Third, the results are readily applicable to any square QAM constellation. Finally, receive signal strength indication (RSSI) measurement could be also accomplished as a by-product of this design.

The structure of this brief is as follows. Section II presents the demodulator architecture using 16-QAM as a design example. System robustness against analog processing errors is considered in Section III. Simulation results are presented in Section IV. Section V compares the complexity of the proposed design to that of a traditional digital demodulator. Section VI concludes the brief and provides directions for future research.

II. 16-QAM Demodulator

For square M-QAM constellations, the demodulation is traditionally done using independent $\sqrt{M}$-level quantization of the I and Q signals. For this scheme to work, the symbols have to be properly scaled before demodulation and the sensitivity to scaling mismatch grows with the constellation order. Automatic gain control (AGC) implements a coarse gain adjustment whose primary purpose is to prevent saturation and clipping in the receiver front-end, as well as improving the signal-to-quantization-noise-ratio (SQNR) of the analog to digital converter (ADC). This coarse tuning is usually not sufficient to meet the bit-error-rate (BER) requirement. The final gain

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adjustment is usually done as part of channel estimation or equalization prior to demodulation [8]. Our objective in this work is to study a minimal complexity demodulator without the need for digital processing, and consequently, the scaling approach is not pursued in this design.

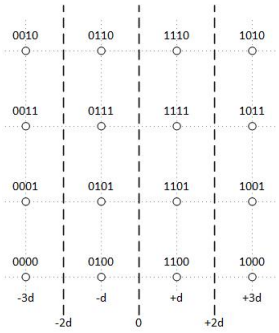

Fig. 1. Gray-coded 16-QAM constellation

Minimum-error demodulation in I (or Q) dimension requires a quantization threshold that is equidistant from its two nearest symbols. This *relative* relationship between the symbols and thresholds could be achieved by leaving the symbol intact and adjusting the threshold instead. For the 16-QAM constellation shown in Fig. 1, it is straightforward to show that

$$\mathbb{E}|I| = \mathbb{E}|Q| = 2d \tag{1}$$

where I and Q are the in-phase and quadrature components of the QAM symbol and $\mathbb{E}$ is the expectation operator. Considering the fact that I (or Q) quantization thresholds are $\pm 2d$ and 0, the expectations calculated in (1) directly provide the correct quantizer reference voltage without explicitly scaling the signal itself. This eliminates the need for a programmable, high resolution analog gain component that would be required for a traditional signal-scaling scheme. Moreover, the proposed threshold estimation approach enables the quantizer to automatically adapt as the signal strength varies.

The expectation in (1) is implemented using an envelop detector comprising a rectifier and an inexpensive passive low-pass filter. The 4-level, 2-bit quantizer is implemented using comparators and a few logic gates. The design is identical and independent for both I and Q paths. The use of a single envelop detector further simplifies the design considering that the expectations for the I and Q paths are the same. A functional diagram of the demodulator is shown in Fig. 2. The extension

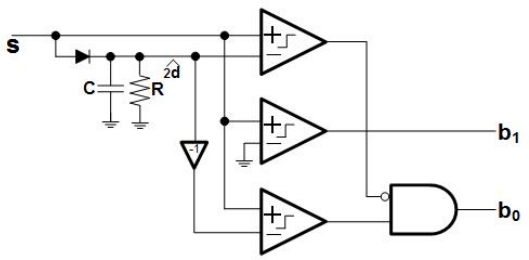

Fig. 2. Functional diagram of the proposed 16-QAM demodulator (I or Q)

to higher order QAM constellations is straightforward. For instance, 64-QAM has $\mathbb{E}|I| = \mathbb{E}|Q| = 4d$. Simple scaling produces the required $\pm 2d$. $\pm 4d$, and $\pm 6d$ threshold levels.

To design the low-pass filter, we assume that a portion of the transmission period is allocated to training. Given a packet size of L symbols, fractional training overhead Ovh, and a symbol rate F_{Sym}, the training duration is $\frac{Ovh \times L}{F_{Sym}}$. A first-order filter converges to its 99-percentile in five time constants and consequently, the filter time constant is derived as [9]

$$\tau = RC = \frac{Ovh \times L}{5F_{Sym}} \tag{2}$$

The threshold estimation could continue using data symbols after the training period. This provides automatic tracking of the gain variations.

Even though the proposed design does not need explicit signal scaling, some coarse gain control is still needed in the final design to prevent saturation. The calculated $\mathbb{E}|I|$ could be used as an approximate received signal strength indicator (RSSI) for the AGC purpose. If an exact power measurement is needed instead, then $\left(\mathbb{E}|I|\right)^2$ may be used at the expense of an additional analog multiplier.

A natural question here is the robustness of analog processing for this application. This question is answered analytically and experimentally in the next two sections, respectively.

III. Error Analysis

In this section, we analyze the effect of threshold estimation errors on the system performance. The errors are caused by the estimation process itself as well as the errors associated with analog processing.

For an M-QAM constellation with a minimum distance of $2d$, the threshold to be estimated is $\mathbb{E}|I| = \frac{\sqrt{M}d}{2}$. The estimation error is assumed to be normally distributed with zero mean and variance σ^2. The 99.7-percentile range of the error, or 3σ, is used to define the normalized error range as

$$e_T = \frac{3\sigma}{\frac{\sqrt{M}d}{2}} \tag{3}$$

Used as a design parameter, e_T specifies the amount of variation that the system could tolerate without violating the link budget. For instance, $e_T = 0.1$ indicates that the system would tolerate estimation errors within $\pm 10\%$.

A threshold error of size e could be equivalently modeled as a signal error of size $-e$ assuming an error-free threshold. Threshold estimation error could then be modeled as a complex additive white Gaussian noise of variance $2\sigma^2$.

The average power of an M-QAM constellation is given as [10]

$$P_S = \frac{2}{3} c_M (M-1) d^2 \tag{4}$$

where we further assume that for a given receiver noise, the transmitted power is scaled with a factor c_M such that the same bit error rate is maintained for different constellation orders. The signal-to-noise ratio associated with threshold estimation is then $\text{SNR}_T = \frac{P_S}{2\sigma^2}$, or

$$SNR_T = 10\log(12) + 10\log(c_M) + 10\log\left(\frac{M-1}{M}\right) - 20\log e_T \quad \text{(dB)} \tag{5}$$

TABLE I
ESTIMATION SNR AND LOSS FOR M=16, 64, 256

	SNR_T (dB)			Δ (dB)		
BER	16	64	256	16	64	256
10^{-3}	30.5	36.7	42.6	0.17	0.16	0.16
10^{-4}	30.5	36.8	42.8	0.25	0.24	0.24
10^{-5}	30.5	36.8	42.9	0.33	0.31	0.31
10^{-6}	30.5	36.9	43.0	0.41	0.39	0.38
10^{-7}	30.5	36.9	42.9	0.49	0.46	0.46
10^{-8}	30.5	37.0	43.0	0.56	0.53	0.53

Using the 16-QAM average power as the reference, $c_{16} = 1$, the corresponding factors for higher order constellations are derived using the QAM BER equation given in the Appendix. It is easy to show that $c_{64} \approx 4$ and $c_{256} \approx 16$ for all practical bit error rates. This implies that for the same BER, SNR_T increases by 6 and 12 dB for 64 and 256 QAM, respectively.

We further assume that the threshold estimation error is stochastically independent from the receiver thermal noise. This leads to an effective system SNR of

$$SNR = \frac{1}{\frac{1}{SNR_R} + \frac{1}{SNR_T}} \tag{6}$$

where SNR_R is the target receiver signal-to-noise-ratio. The loss associated with threshold estimation is then

$$\Delta = 10 \log \frac{SNR_R}{SNR} = 10 \log \left(1 + \frac{SNR_R}{SNR_T}\right) \quad \text{(dB)} \tag{7}$$

The loss Δ is an implementation loss associated with threshold estimation. For a given error range e_T, Δ is the extra transmission power that would be required to meet the link budget.

Table I shows the estimation SNR and loss for different QAM constellations assuming $e_T = \pm 10\%$. Larger constellations use higher transmission power for the same bit error rate and this helps with threshold estimation. The relatively high estimation SNR translates into small overall SNR loss of the system. This indicates that the design is both low-loss and scalable. In other words, the analog demodulation does not pose an additional constraint on the SNR requirement.

The estimation error and thermal noise are not strictly independent as the estimation error is dependent upon the quality of the received symbols. The validity of this assumption is investigated in Section IV.

The threshold estimation range, e_T, and the training time constant τ are the system design parameters that are used to explore the trade-off between overhead, performance, and circuit/process reliability.

IV. SIMULATION RESULTS

Fig. 3 shows the simulation results. The reference *Ideal* curve is the 16-QAM theoretical BER given in the Appendix. In the first experiment labeled *Error Only*, the threshold is not estimated. The ideal thresholds are used but they are disturbed by $e_T = \pm 10\%$. The idea is to observe the relative robustness of the system to the measurement errors alone. At 10^{-4} BER, the loss is about 0.25 dB and the results match well with (7). This is expected as the measurements errors are added independent of the receiver noise.

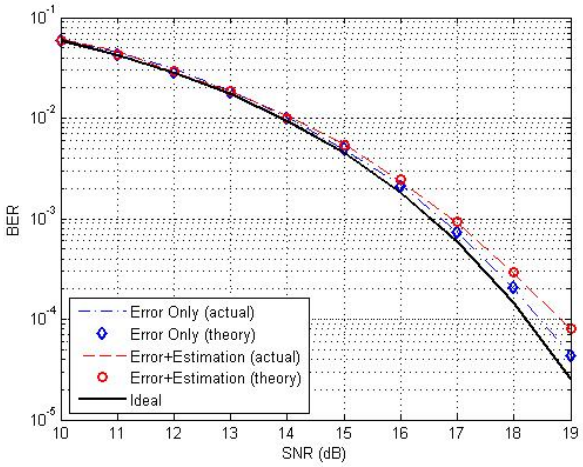

Fig. 3. Simulation results

In the next experiment, labeled *Error+Estimation*, the thresholds are estimated using 15% overhead while the same measurement error of $e_T = \pm 10\%$ is used. At the same BER of 10^{-4}, the SNR loss is now increased to 0.5 dB. Note that the effective error range is no longer 10% as the estimation errors are now added to the measurement errors. In the figure, we used the variance of the threshold estimates and updated the corresponding e_T in (7) in order to get an accurate prediction of the loss. Even though the threshold estimates are now affected by the receiver noise, the good match indicates that the two noise sources could be considered independent. Therefore, one could accurately predict the system performance using (7) so long as e_T is allocated as the total budget for threshold variation (estimation and measurement errors both).

The relatively small loss in the system performance deems acceptable considering the fact that demodulation is analog and the associated processing errors are taken into account. The required training overhead is also comparable to fully digital demodulation schemes [11].

V. COMPLEXITY

Despite being analog, the proposed demodulator is effectively using a $\frac{\log_2 M}{2}$-bit ADC. This is the minimum required resolution for demodulating an M-QAM signal. Recall that this work was in part motivated by the desire to eliminate or simplify the ADCs used in digital implementations. One subtle difference between the two systems is the ordering of quantization and detection operations. Quantization is done first followed by detection in the digital implementation whereas the analog system simultaneously detects and quantizes. It is instructive to compare the relative complexity of the two approaches. As the basis for comparison, we use the additional number of ADC bits that would be required for a digital design.

Considering the demodulation function only, we assume that the ADC resolution is merely determined by the quantization noise. For a given target signal-to-noise ratio SNR_R and a normalized signal power of one, the noise power is given as

$N = \frac{1}{SNR_R}$. Given a quantization loss budget of Δ dB, we have

$$\frac{\frac{1}{N}}{\frac{1}{N+\frac{N_Q}{ovs}}} = 10^{\frac{\Delta}{10}} \tag{8}$$

where N_Q is the quantization noise power and ovs is the ADC oversampling ratio. The required number of ADC bits, N_b, is derived from [12]

$$SQNR = -10 \log N_Q = 6.02 N_b + 1.76 \tag{9}$$

where SQNR is the signal-to-quantization-noise-ratio. From (8) and (9), the number of additional ADC bits, ΔN_b, for digital implementation is derived as

$$\Delta N_b = \left\lceil \frac{-10 \log \left(\frac{(10^{\frac{\Delta}{10}} - 1) ovs}{SNR_R} \right) - 1.76}{6.02} \right\rceil - \frac{\log_2 M}{2} \tag{10}$$

By equating the loss Δ in (7) and (10), we can compare the analog and digital systems that achieve the same performance. More specifically, we consider the resolution advantage of the analog design as a function of its error range e_T. Fig. 4 shows this relationship for 16-QAM, $ovs = 2$, and target BER of 10^{-4}. For $e_T = \pm 10\%$, the associated loss is 0.25 dB and 3 more ADC bits are required. This translates into an additional $(2^{2+3} - 1) - (2^2 - 1) = 28$ comparators per quantizer. The number of extra comparators rises to 60 if the error range is reduced to $e_T = \pm 5\%$. The results

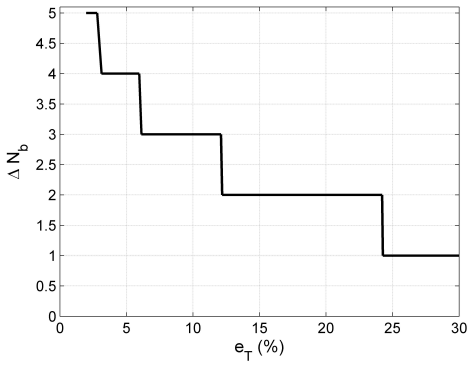

Fig. 4. ADC bit savings

show that by performing detection on the analog waveform, the proposed design eliminates the loss associated with the quantization and a minimal-complexity ADC could be used. It should be noted that the analysis is conservative as it does not include the additional complexity associated with digital processing. At the minimum, the digital processing involves pulse shaping. The bit growth within the filter and the parallelization of the processing incurs additional complexity and power consumption at high data rates.

It may appear that the bitwidth advantage of the analog solution comes at the cost of training overhead. Note, however, that the digital system would need comparable training in order to correct the signal scaling before demodulation. A truly fair comparison of the two solutions requires complete transceiver designs including synchronization, equalization and other required functionalities. The objective of the analysis above was to gain some insight on the relative complexity of an alternative solution when digital implementation is inefficient or infeasible.

VI. Conclusion

In this brief, we proposed the system design for a fully analog QAM demodulator as an alternative to power-hungry digital implementations. System robustness over estimation and measurement errors was shown via simulations. It was shown that with reasonable training overhead, the proposed design offers significant reduction in complexity compared to a traditional digital demodulator. Simple analytical expressions were derived to predict the system performance. Design parameters were provided for exploring training and performance trade-offs.

While the demodulator is a major component of the receiver, there are other critical components in the system (such as equalization and synchronization, to name a few) that need to be designed as parts of a fully functional analog transceiver. These challenging design problems represent an exciting direction for future research.

Appendix

The bit error rate expression for M-QAM is given as [13]

$$P_b \approx \frac{4}{\log_2 M} \left(1 - \frac{1}{\sqrt{M}}\right) Q\left(\sqrt{\frac{3 \log_2 M}{M-1} \frac{E_b}{N_0}}\right)$$

where $Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-\frac{u^2}{2}} du$, and $\frac{E_b}{N_0} = \frac{SNR}{\log_2 M}$.

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