Well-Posed Verilog-A Compact Model for Phase Change Memory

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***Abstract*—In this work, we demonstrate a well-posed compact model for phase change memory (PCM) devices based on $Ge_2Sb_2Te_5$ (GST) chalcogenide. This model supports all modes of simulation including transient, DC, and AC. The model is developed in Verilog-A and simulated using HSPICE. It is computationally simple and successfully captures the key high level behaviors of memory switching, including the resistance dependence on programming voltages, currents and pulse time-scales.**

***Index Terms*—Phase change memory, chalcogenide, Verilog-A, well-posed model**

I. Introduction

Phase change memory (PCM) is a non-volatile memory technology that is emerging as a leading contender for storage class memories as well as in-memory computing applications based on crossbar array architectures with co-located memory and processing units [1]–[3]. Emerging memory devices such as PCM, STT-RAMs (Spin-Transfer Torque Random Access Memory) and RRAM (Resistive RAM) have also shown the capability to be programmed to store analog resistance levels, and are being explored for realizing area and power efficient accelerators for machine learning and embedded AI applications [4]–[8].

For designing neuromorphic and in-memory computing architectures using non-volatile memory (NVM) devices, efficient compact models are required, capturing their key operating characteristics. In this paper, we present a well-posed model for phase change memory (PCM) devices based on $Ge_2Sb_2Te_5$ (GST) chalcogenide. Several models for the GST based PCM device have been proposed earlier, capturing various aspects of the device physics [9]–[19]. The hierarchical model in [9] incorporates the device geometry and device physics, though it is computationally quite expensive. Simpler models have also be developed using basic circuit elements such as controlled voltage/current sources, resistances and capacitances to model the device behavior [10], [11]. The model presented in [10] captures the binary switching of the device from crystalline to amorphous state, and vice versa. The state switching is based on the analysis of the quenching time once the device temperature exceeds the melting point. A further enhancement of this model showed the capability of demonstrating multiple resistance states within the device as a function of programming current and quenching time [11]. A single equation was used to define the model's I-V response, describing both the off state (low field) and the on state (high field) behavior, with a set of blending functions used to combine the two regimes.

Our model, based on the one discussed in [11], is developed in Verilog-A. It is computationally simple as it uses basic circuit elements and successfully captures the high level dynamics of resistance switching, including its dependence on programming voltages, currents and pulse time-scales. Our results also show the capability of the model to emulate multi-bit storage characteristics of PCM, with pulse-width and pulse-quench based programming schemes. In addition, our model is well-posed and supports different modes of simulation including transient, DC and AC, as per the guidelines discussed in [20], [21], which so far has not been addressed in previous models.

The rest of the paper is organized as follows. In Section II, we first briefly describe the physics of PCM devices and their switching characteristics. The development of the compact model in Verilog-A is discussed in Section III, emphasizing the techniques used to make the model well-posed. In Section IV, we present simulation results based on the proposed model and compare the obtained characteristics with experimental device data.

II. Device physics and operation

Phase change memory (PCM) device consists of a chalcogenide alloy sandwiched between two metal electrodes. Depending on the amplitude and timescales of the programming pulses, the chalcogenide material can be heated and quenched to a high resistive amorphous phase (also called the RESET state) or re-crystallized to a low resistive poly-crystalline phase (also called the SET state) [1]–[3]. This transition between the crystalline and amorphous regions through Joule heating is reversible and allows the device to be used as a programmable resistor, and hence as a memory storage device. Typically observed contrast in conductance (ON/OFF ratio) of PCM devices is between $100 - 1000$. Furthermore, by controlling the amplitude and falling rate of the programming pulse, it is also possible to gradually change the shape of the amorphous volume in the critical current path of the device,

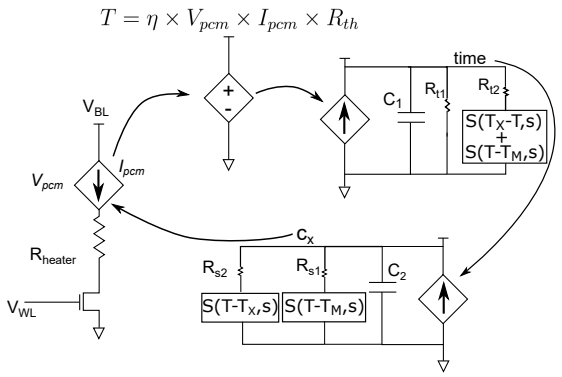

Fig. 1. Schematic of the continuous compact Verilog-A model for the PCM device. This model is inspired from [11], and also satisfies the guidelines for compact model development specified in [20].

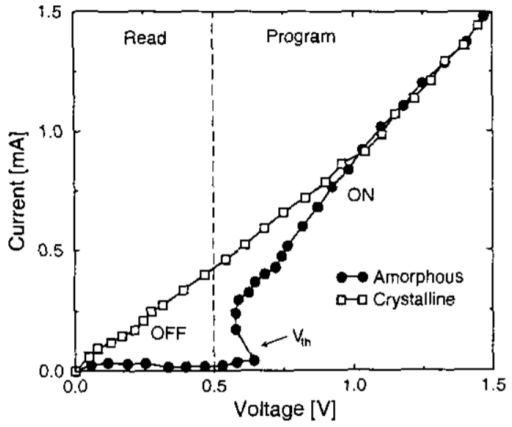

Fig. 2. Typical experimental I-V characteristics of PCM device (reproduced from [25]).

enabling stable analog changes in conductance, and multi-bit storage [3], [22].

Different structures for the PCM devices have been demonstrated such as the mushroom, pore and bridge cell configurations [1]. The mushroom cell is more widely used, where the bottom electrode, which also acts as the heater, is much smaller in diameter ($< 50\,\text{nm}$) compared to the top electrode dimension [1]. More recently, confined PCM cells have been demonstrated, which enables strong control of Joule heating even in the presence of voids [23], [24].

III. Compact Model

Building up on a previously published discontinuous model [11], we have developed a well-posed Verilog-A model of the device (Fig. 1), where the device resistance is calculated based on a lumped parameter c_x that represents the crystalline fraction within the device. The current through the device is given as:

$$I_{PCM} = I_\alpha(V_{PCM}, c_x) + F(I_{PCM}; I_{th}).[-I_\alpha(V1, c_x) + F(V_{PCM}; V_{hold}).I_{ON}(V_{PCM})] \quad (1)$$

where the OFF state current I_α and programming region current I_{ON} is:

$$I_\alpha = \frac{\exp(n(c_x).V_{PCM}) - 1}{n(c_x).R(c_x).\exp\left(\frac{E_a(c_x)}{k_B}\left(\frac{1}{T} - \frac{1}{T_{ref}}\right)\right)} \quad (2)$$

$$I_{ON} = \frac{V_{PCM} - V_{hold}}{R_{ON}} \quad (3)$$

I_{th} represents the threshold current below which switching does not take place and V_h is the hold voltage, which is the x-intercept of the linear region of the I-V curve (see Fig. 2). I_{ON} represents the current during the ON state or programming state of the device, when the conductance of the device increases. Note that the device resistance R_{ON}, when sufficiently large currents are passing through the device (such that some portion of the chalcogenide alloy is in the molten phase), is significantly lesser that the typical SET resistance of the device.

TABLE I
Parameters used in the well-posed Verilog-A PCM compact model.

Symbol	Value	Symbol	Value
R_{th}	65 MK/W	R_{s1}	$1\,\mu\Omega$
C_1	1 nF	R_{s2}	$1\,\Omega$
R_{t1}	$1\,\text{G}\Omega$	R_{heater}	$410\,\Omega$
R_{t2}	$1\,\mu\Omega$	E_a (in eV)	$0.27 - 0.25c_x$
T_X	200°C	Γ_a	2.3 eV
T_M	600°C	A	1.06×10^{-23} ns
C_2	20 nF	V_h	0.5 V
R_{ON}	$1000\,\Omega$	I_{th}	$40\,\mu$A

Based on the device current and voltage, the temperature (T) rise in the material is estimated using a lumped thermal resistance model, assuming a heating efficiency of $\eta = 1\%$ [26]. We also assume that in scaled PCM devices, the thermal time constant is significantly smaller than typical SET and RESET pulse-widths.

The crystallization dynamics in the device is described using the Johnson-Mehl-Avrami-Kolmogorov (JMAK) expression [27], giving the instantaneous crystallization fraction c_x within the device, which is then used to approximate the device resistance using the following expressions:

$$c_x = 1 - \exp\left(-t/\tau(T)\right) \quad (4)$$

$$R = R_{SET} \times c_x + R_{RESET} \times (1 - c_x) \quad (5)$$

where $\tau(T) = A\exp(\Gamma_a/k_BT)$ and the device resistance varies between the SET ($R_{SET} = 10\,\text{k}\Omega$) and RESET resistance ($R_{RESET} = 1\,\text{M}\Omega$). The functions F in equation 1 are the blending functions that combine the different regions of the model's I-V curve. We used a smooth step function $S(x, s)$ to model temperature controlled switches in the auxiliary circuits (Fig. 1) [21]. They are given by the following expressions:

$$F(x; x_{th}) = \frac{1}{(1 + \exp\left(-(x - x_{th})/\alpha\right))} \quad (6)$$

$$S(x, s) = 0.5\left(\frac{x}{\sqrt{x^2 + s}} + 1\right) \quad (7)$$

where, s is the smoothening parameter controlling the transition rate of the step function $S(x, s)$. The different parameters used in our model are listed in Table I.

We follow the guidelines listed by the NEEDS (Nano-Engineered Electronic Device Simulation) initiative [20] to develop a mathematically well-posed model that converges for different modes of simulations such as transient, AC and DC. For this to be satisfied, the Verilog-A model should adhere to a set of coding guidelines. Some of the key requirements include describing the model as a set of Differential Algebraic Equations (DAE) and avoiding any abrupt bias dependent switching statements in the Verilog-A code. The I-V expression for the PCM (equation 1) as presented in [11] is an algebraic expression. By employing smoothened step functions (equation 7), we eliminate sharp temperature dependent switching in the auxiliary circuit (which computes the quench time and crystalline fraction) of the model. Hence, our continuous model is capable of operating in all the different modes of simulation.

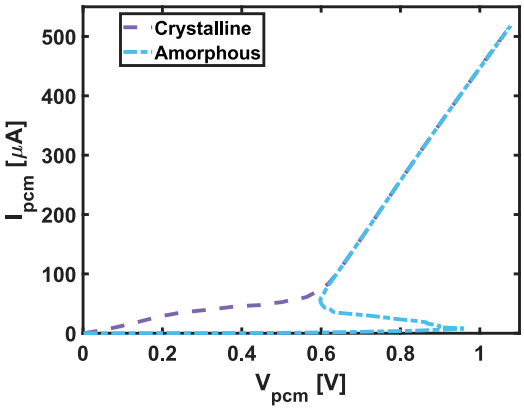

Fig. 3. I-V response of the well-posed PCM Verilog-A model. The behavior was captured by applying a voltage ramp at the Word Line (WL), i.e., the gate of the access NMOS for the two states of initialization (SET and RESET).

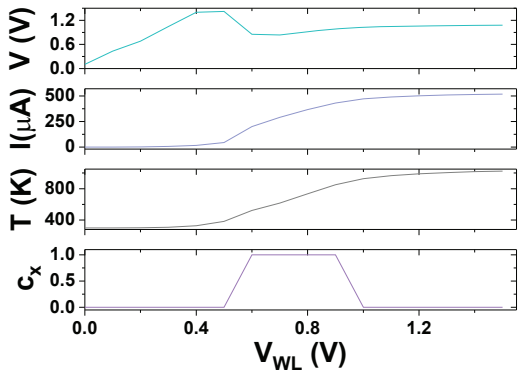

Fig. 4. DC behavior of the PCM device from HSPICE simulations. From top to bottom: the waveforms of the PCM voltage drop (V), current (I), temperature (T) and the crystalline fraction (c_x) as a function of V_{WL}.

IV. Simulation Results

We simulated the switching behavior of the PCM device connected in series with an NMOS access transistor from a commercial 65 nm CMOS technology. Our simulations show that the model captures the essential features of typical I-V characteristics (Fig. 3) similar to what is seen in the experimental device data in Fig. 2. The simulations were conducted by applying a voltage ramp at the Word Line (WL) for the two states of initialization (SET and RESET).

The model also works in the DC mode; Fig. 4 shows the steady state response of the internal parameters, T and c_x at different voltage values applied to the gate of the access transistor (V_{WL}).

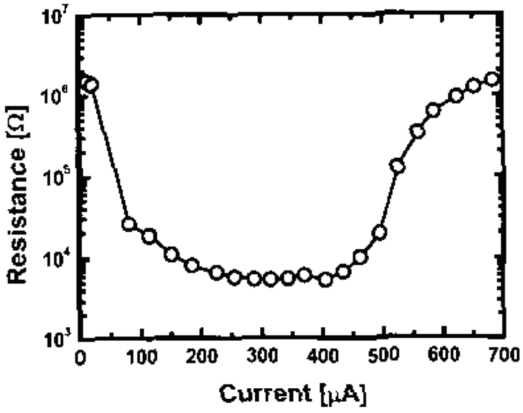

Fig. 5. Experimental resistance vs. programming current characteristics of a PCM device (reproduced from [28]).

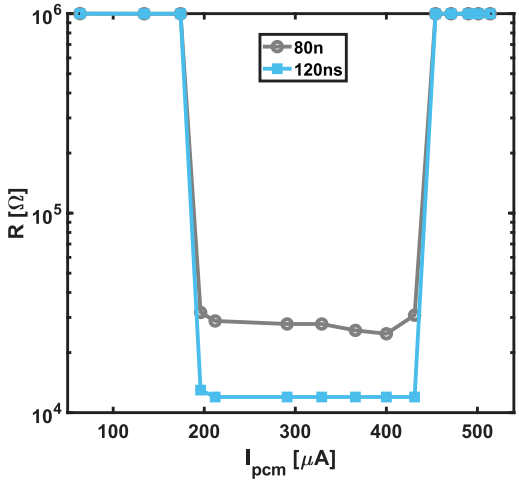

Fig. 6. The R-I curve obtained using the model for programming pulse widths of 80 ns and 120 ns.

Next, we compared the dependence of the device resistance as a function of the applied programming current. Typical experimental characteristics of a PCM device is shown in Fig. 5. Starting from a high resistance state, the device resistance can be reduced by applying low amplitude SET pulses; however,

once the applied pulse amplitude is sufficiently large to induce melting in the chalcogenide, the device is programmed to its RESET state. The proposed model's behavior shown in Fig. 6 closely matches this experimentally observed programming trend.

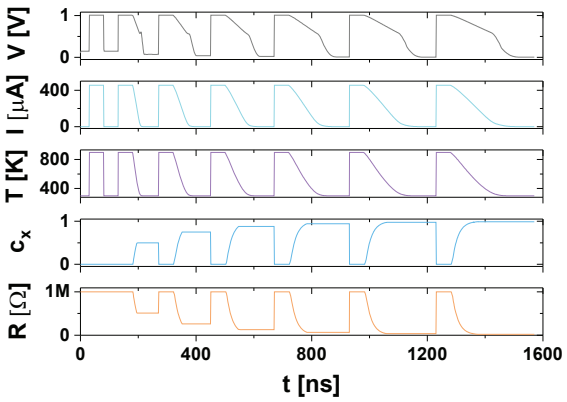

Fig. 7. Simulated device parameters as a function of the duration of the falling edge of the input pulse. Application of each pulse initially resets the pulse and then brings the final resistance to an intermediate value below R_{reset} depending on the duration of the falling edge. From top to bottom: the waveforms of the PCM voltage drop (V), current (I), device temperature (T), crystalline fraction (c_x) and the device resistance (R).

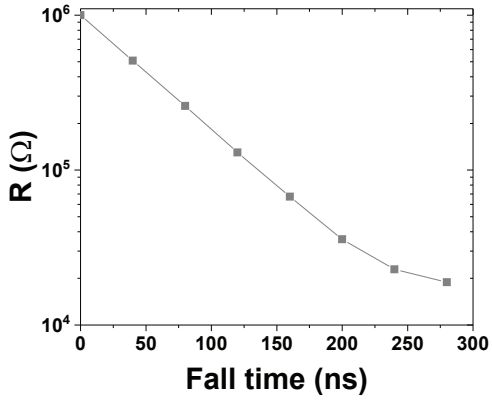

Fig. 8. PCM final resistance as a function of falling edge of input pulse, plotted from the resistance values as shown in Fig. 7.

We also studied the response of the device model to show multiple conductance levels between R_{SET} and R_{RESET} using two approaches. Dependence of the device resistance on quench time has been demonstrated in [29]. We also employed the same scheme in the simulations by applying pulses having variable fall times in the range of 50 ns to 300 ns. The last two panels in Fig. 7 show the gradual change in the crystalline fraction and the device resistance as the fall time of the programming pulse is increased. Fig. 8 shows the programmed resistance from the model as a function of the fall time.

Another method of programming the device to various intermediate conductance levels by applying partial SET pulses was demonstrated in [30]. We also simulated the similar behavior using the model, by applying a sequence of short duration pulses, as shown in the waveforms in Fig. 9. Each programming pulse has a constant amplitude ($V_{WL} = 0.7$ V) and duration (20 ns). Fig. 10 shows the device resistance as a function of the number of programming pulses.

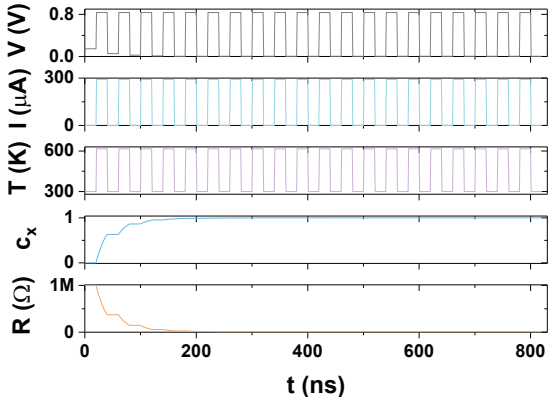

Fig. 9. Gradual conductance change by application of a series of low amplitude partial SET pulses. From top to bottom: the waveforms of the PCM voltage drop (V), current (I), device temperature (T), crystalline fraction (c_x) and the device resistance (R).

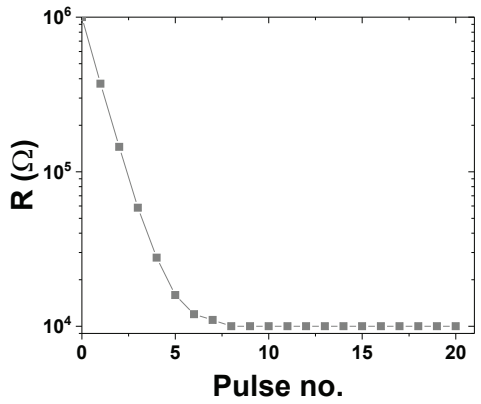

Fig. 10. PCM resistance as a function of the number of partial SET pulses, plotted from the resistance values as shown in Fig. 9.

V. Conclusion

We have developed a well-posed Verilog-A compact model that accurately captures the essential aspects of experimentally observed memory switching in phase change memory devices. The model also shows multiple resistance states depending on the programming schemes employed. Future work includes incorporating reliability aspects such as resistance drift and stuck-at fault simulation capability in the model, towards evaluating large memory arrays and neuromorphic circuits using PCM devices.

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