

Atomristor: Nonvolatile Resistance Switching in Atomic Sheets of Transition Metal Dichalcogenides

Ruijing Ge,^{†,‡,§,¶} Xiaohan Wu,^{†,‡,§} Myungsoo Kim,[†] Jianping Shi,[‡] Sushant Sonde,^{§,⊥,¶} Li Tao,^{¶,†} Yanfeng Zhang,^{‡,¶} Jack C. Lee,[†] and Deji Akinwande^{*,†}

[†]Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758, United States

[‡]Department of Materials Science and Engineering, College of Engineering, Peking University, Beijing 100871, China

[§]Institute for Molecular Engineering, University of Chicago, 5640 South Ellis Avenue, Chicago, Illinois 60637, United States

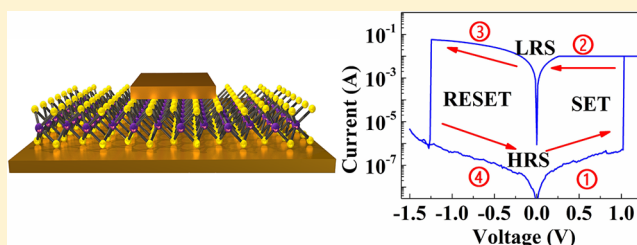
[⊥]Center for Nanoscale Materials, Argonne National Laboratory, 9700 Cass Avenue, Lemont, Illinois 60439, United States

[¶]School of Materials Science and Engineering, Southeast University, 2 Southeast University Road, Nanjing 211189, China

Supporting Information

ABSTRACT: Recently, two-dimensional (2D) atomic sheets have inspired new ideas in nanoscience including topologically protected charge transport,^{1,2} spatially separated excitons,³ and strongly anisotropic heat transport.⁴ Here, we report the intriguing observation of stable nonvolatile resistance switching (NVRS) in single-layer atomic sheets sandwiched between metal electrodes. NVRS is observed in the prototypical semiconducting (MX₂, M = Mo, W; and X = S, Se) transitional metal dichalcogenides (TMDs),⁵ which alludes to the universality of this phenomenon in TMD monolayers and offers forming-free switching. This observation of NVRS phenomenon, widely attributed to ionic diffusion, filament, and interfacial redox in bulk oxides and electrolytes,^{6–9} inspires new studies on defects, ion transport, and energetics at the sharp interfaces between atomically thin sheets and conducting electrodes. Our findings overturn the contemporary thinking that nonvolatile switching is not scalable to subnanometre owing to leakage currents.¹⁰ Emerging device concepts in nonvolatile flexible memory fabrics, and brain-inspired (neuromorphic) computing could benefit substantially from the wide 2D materials design space. A new major application, zero-static power radio frequency (RF) switching, is demonstrated with a monolayer switch operating to 50 GHz.

KEYWORDS: Nonvolatile memory, RF switch, TMD monolayer, flexible electronics



Recently, nonvolatile resistance switching has been observed in various solution-processed multilayer two-dimensional (2D) material morphologies, including pristine, reduced and functionalized graphene oxide mixtures, partially degraded black phosphorus, functionalized MoS₂ and composites, and transitional metal dichalcogenide (TMD) based hybrids,^{11–14} where the resistance can be modulated between a high-resistance state (HRS) and a low-resistance state (LRS) and subsequently retained absent any power supply. In addition, several researchers have reported nonvolatile resistance switching (NVRS) in multilayer h-BN.^{15,16} However, it was believed that NVRS phenomenon was not accessible in single-layer atomic sheets^{11,17} due to excessive leakage current that is known to prevent nanometre scaling in conventional oxide-based vertical metal–insulator–metal (MIM) configuration.¹⁰ Sangwan et al. circumvented this issue with the discovery that rearrangement of atoms at certain grain boundaries in single-layer MoS₂ produced NVRS in lateral devices.¹⁸ However, for practical nanotechnology, vertical MIM devices are of contemporary preference owing to their smaller footprint and denser integration.

In this article, we report the first observation of NVRS phenomenon in a variety of single-layer TMD atomic sheets (MoS₂, MoSe₂, WS₂, WSe₂) in desired MIM configuration (Supplementary Table), overcoming a fundamental limitation in ultrascaled bulk materials. These devices can be collectively labeled atomristor, in essence, memristor effect in atomically thin nanomaterials or atomic sheets. Furthermore, controlled experiments with active (Ag), noble (Au), and graphene electrodes, and on a single-crystalline device also produce NVRS, suggesting a rich multiphysics mechanism at the atomic limit. Moreover, the rapid commercialization of large-area synthesis and the ever-increasing portfolio of 2D nanomaterials and alloys indicate that atomic sheets can play a substantial role for numerous emerging applications such as nonvolatile switches and memory fabrics, memristor circuits, and computing. Compared with the traditional flash memory application using TMD atomic sheets,^{19,20} the resistance switching memory has the advantage of lower programming

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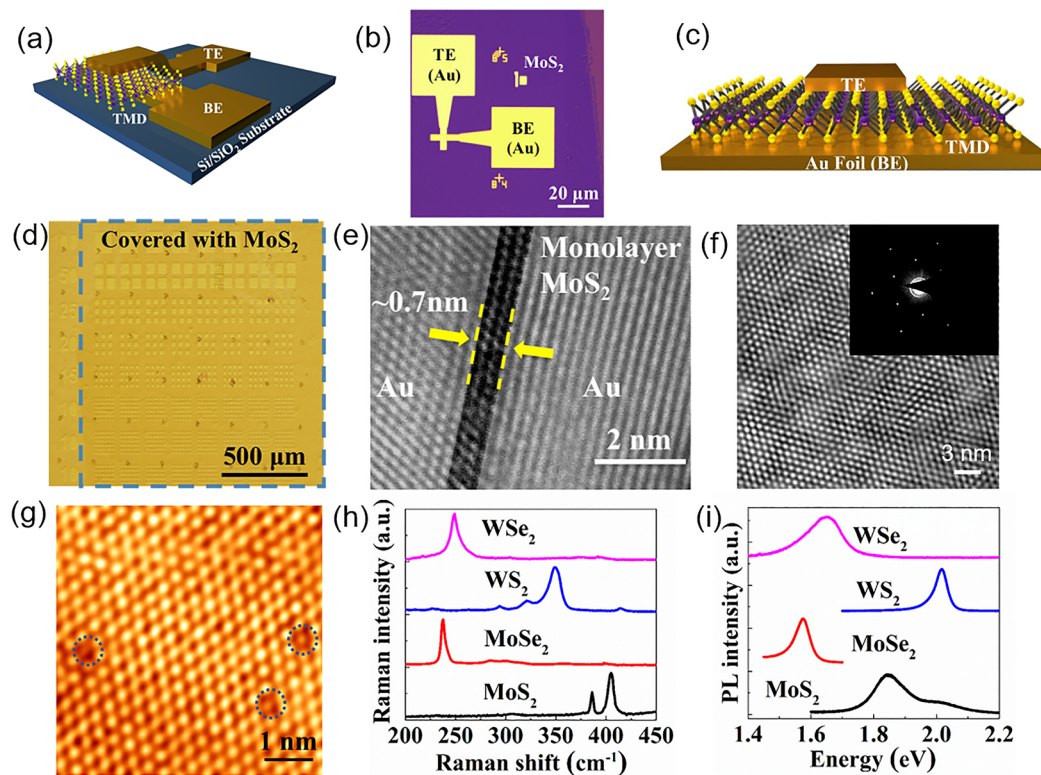


Figure 1. Schematic, device, and material characterization. (a, b) Schematic and optical image of metal–insulator–metal structures of TMD crossbar sandwich. (c) Schematic of TMD lithography-free and transfer-free sandwich (TE and BE are gold, if not specified) based on MoS₂ grown on Au foil. (d) Optical image of fabricated MoS₂ litho-free devices with Au electrodes on Si/SiO₂ substrate. The dash box in panel d indicates the area covered with MoS₂. (e) TEM cross-section image of Au/MoS₂/Au litho-free device revealing the atomically sharp and clean monolayer interface. (f) Atomic resolution TEM image of MoS₂ after transfer onto TEM grid. The hexagonal honeycomb structure has an in-plane lattice constant ~ 0.31 nm indicating high-quality synthesized MoS₂. Inset: selective area electron diffraction (SAED) pattern captured from MoS₂ film, consisting of only one set of hexagonally arranged diffraction spots, suggestive of single-crystal growth. (g) Atomically resolved STM images of monolayer MoS₂ on Au(100). The S vacancy defects ($\sim 10^{12}/\text{cm}^2$) are indicated by the dashed circle. (h, i) Raman and PL spectrum of MOCVD-grown monolayer MoS₂, MoSe₂, WS₂ and WSe₂, used in some of the MIM device studies.

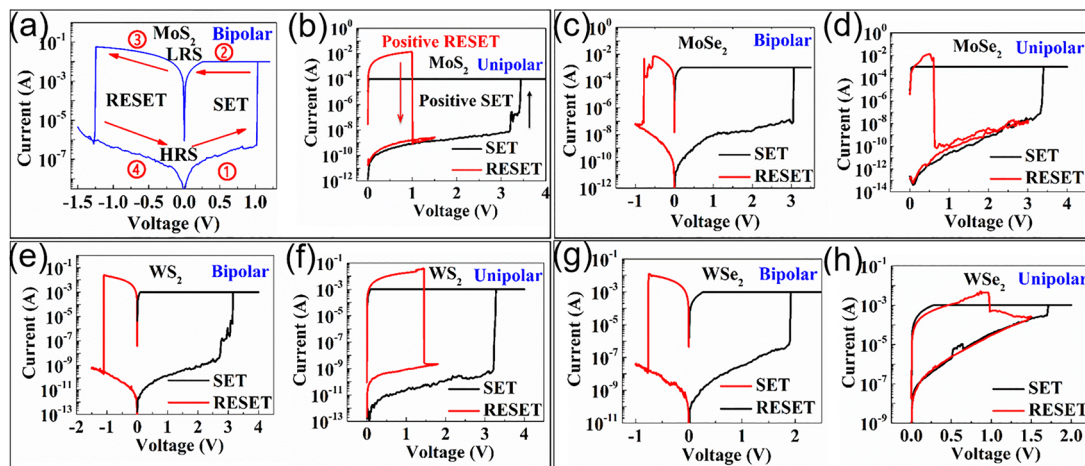


Figure 2. Typical I – V curves of monolayer TMD atomistors. (a) Representative I – V curve of bipolar resistive switching behavior in monolayer MoS₂ crossbar device with lateral area of $2 \times 2 \mu\text{m}^2$. Step 1: voltage increases from 0 to 1.2 V. At ~ 1 V, the current abruptly increases to compliance current, indicating a transition (set) from a high resistance state (HRS) to a low resistance state (LRS). Step 2: voltage decreases from 1.2 to 0 V. The device remains in LRS. Step 3: voltage increases from 0 to -1.5 V. At -1.25 V, the current abruptly decreases, indicating a transition (reset) from LRS to HRS. Step 4: voltage decreases from -1.5 to 0 V. The device remains in HRS until next cycle. (b) Representative I – V curve of unipolar resistive switching behavior in monolayer MoS₂ crossbar device with lateral area of $2 \times 2 \mu\text{m}^2$. For unipolar operation, both SET and RESET transitions are achieved under positive bias. (c–h) Representative I – V curves of bipolar and unipolar resistive switching behavior in monolayer (c, d) MoSe₂, (e, f) WS₂, and (g, h) WSe₂ crossbar MIM devices alluding to a universal nonvolatile phenomenon in related TMD atomic sheets. The areas of the crossbar devices are $0.4 \times 0.4 \mu\text{m}^2$ for MoSe₂, $2 \times 2 \mu\text{m}^2$ for WS₂, and $2 \times 2 \mu\text{m}^2$ for WSe₂.

voltage and overcomes the problem of the leakage of stored charges in the floating gate through tunneling oxide if scaling down to nanometers, which enables higher integration density.^{7,21}

Synthetic atomic sheets prepared by standard chemical vapor deposition (CVD) and metal–organic CVD and subsequently transferred (Supplementary Figure 2) onto device substrates^{22,23} were investigated for NVRS effect in MIM configuration as illustrated in Figure 1a and c. Optical images of so-called crossbar and lithography-free MIM devices are shown in Figure 1b and d, respectively. To avoid effects due to metal oxides, inert metal, gold, is used as electrodes (if not specified) and thus ensures that 2D materials play the active role in the resistive switching behavior. Cross-sectional transmission electron microscopy (TEM) was conducted to evaluate a representative fabricated MIM sandwich (Figure 1e), revealing a sharp and clean interface. The MoS₂ monolayer grown on Au foil is characterized by atomic resolution TEM and STM (Figure 1f,g), which indicate the relatively high quality, and also show local sulfur vacancy defects in the MoS₂ film. Additionally, SEM, TEM, AFM, Raman, and photoluminescence characterization of MoS₂ grown on Au foil are included in Supplementary Figure 1. Raman and photoluminescence spectroscopy were used to characterize the MX₂ sheets on Si/SiO₂ substrate showing clear evidence of single-layer spectra as displayed in Figure 1h and i, respectively.

DC electrical measurements were performed on as-fabricated crossbar devices consisting of atomic sheets with Au bottom and top electrodes and revealed nonvolatile resistance switching in the monolayer MX₂ active layers (Figure 2). For instance, MoS₂, the prototypical TMD, featured low currents corresponding to a high-resistance state until the application of ~ 1 V, which SET the atomic-layer switch to a low-resistance state that persists until a negative voltage is applied to RESET it (Figure 2a). A compliance current is applied at SET process to prevent irreversible breakdown, while no compliance current is applied at RESET process. Absent electrical power, this atomic switch consumes zero-static power and affords data retention under ambient conditions (Supplementary Figure 3) for more than 100-times longer than previously reported lateral counterpart.¹⁸ Interestingly, the single-layer nonvolatile switch required no electro-forming step, a prerequisite in transition metal oxides (TMOs) that initializes a soft dielectric breakdown to form a conductive filament for subsequent NVRS operation.^{6,7} Although it has been shown that electroforming can be avoided with thickness scaling into the nm-regime, excessive leakage current from trap-assisted tunnelling is a limiting consequence.^{7,10} Here, an on/off ratio above 10^4 can be achieved, highlighting a defining advantage of crystalline monolayers over ultrathin amorphous oxides.

Low-voltage “READ” characteristics of the HRS and LRS exhibit a linear profile over a small voltage range (Supplementary Figure 4), though the magnitudes of the current can differ by a ratio of more than 10^4 . While the “READ” profiles appears superficially similar, temperature-dependent studies over a larger voltage range indicate uniquely different transport mechanisms in the two states (Schottky emission in HRS and localized direct tunnelling in LRS) and will be discussed further with respect to Figure 4.

Certain single-layer MoS₂ devices of the same MIM construction feature unipolar switching where voltage of the same polarity is used for both SET and RESET programming (Figure 2b). Motivated by the observation of NVRS in MoS₂,

the quartet of single-layer MX₂ was investigated and all showed similar intriguing characteristics of (predominantly) bipolar switching, and (occasional) unipolar switching as demonstrated in Figure 2c–h. These collective results of NVRS in representative atomic sheets allude to a universal effect in nonmetallic TMD monolayers, which open a new avenue of scientific research on defects, charge, and interfacial phenomena at the atomic scale, and the associated materials design for diverse applications. It should be noted that the unipolar devices can also work at opposite bias, which in some cases is referred to as nonpolar switching mode. Regarding the polarity dependence, the precise understanding of the factors that produce either bipolar or unipolar switching in monolayer sheets is yet unclear and is a complex competition among several parameters including lateral area, grain size, and electrodes and interfacial details. Atomistic modeling and microscopy studies are required for elucidation. A recent study in TMOs has suggested the coexistence of bipolar compliance conditions.²⁴ Nevertheless, the underlying physics of unipolar switching has been previously established to be due to electro-thermal heating that facilitates diffusion.^{6,7} A symptom of this effect is the relatively higher RESET current needed to increase the local temperature to break the conductive link.⁷

In the majority of experiments, Au was selected as an inert electrode to rule out any switching effect that might arise from interfacial metal oxide formation. Indeed, devices of identical processing with Au electrodes using Cr as an adhesion layer (for the lift-off of TE), but without a TMD active-layer, did not reveal NVRS (Supplementary Figure 5). Furthermore, to rule out the undesirable contribution of polymer contamination from microfabrication, very clean devices including lithography-free and transfer-free devices (Figure 3a) were made, which also produced the NVRS effect, alluding to an intrinsic origin. The

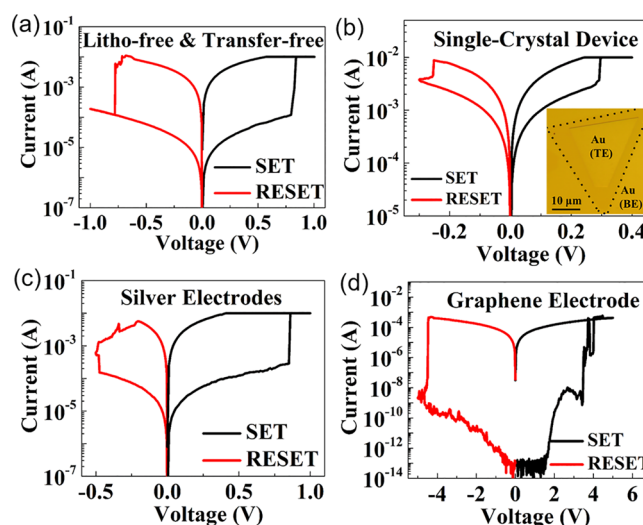


Figure 3. Typical I – V curves of monolayer MoS₂ nonvolatile sandwiches with different device conditions. (a) Representative I – V curve of clean (litho and transfer-free) Au/MoS₂/Au device with lateral area of $15 \times 15 \mu\text{m}^2$. (b) Representative I – V curve of a single-crystal MoS₂ device with Au electrodes. The optical image of the device is shown in the inset, where the dash line is an outline of the single-crystal MoS₂ triangle. (c) Representative I – V curve of a MoS₂ litho-free device using silver as top and bottom electrodes. (d) Representative I – V curve of a MoS₂ crossbar device using graphene as the top electrode and gold as bottom electrode with an area of $1 \times 1 \mu\text{m}^2$.

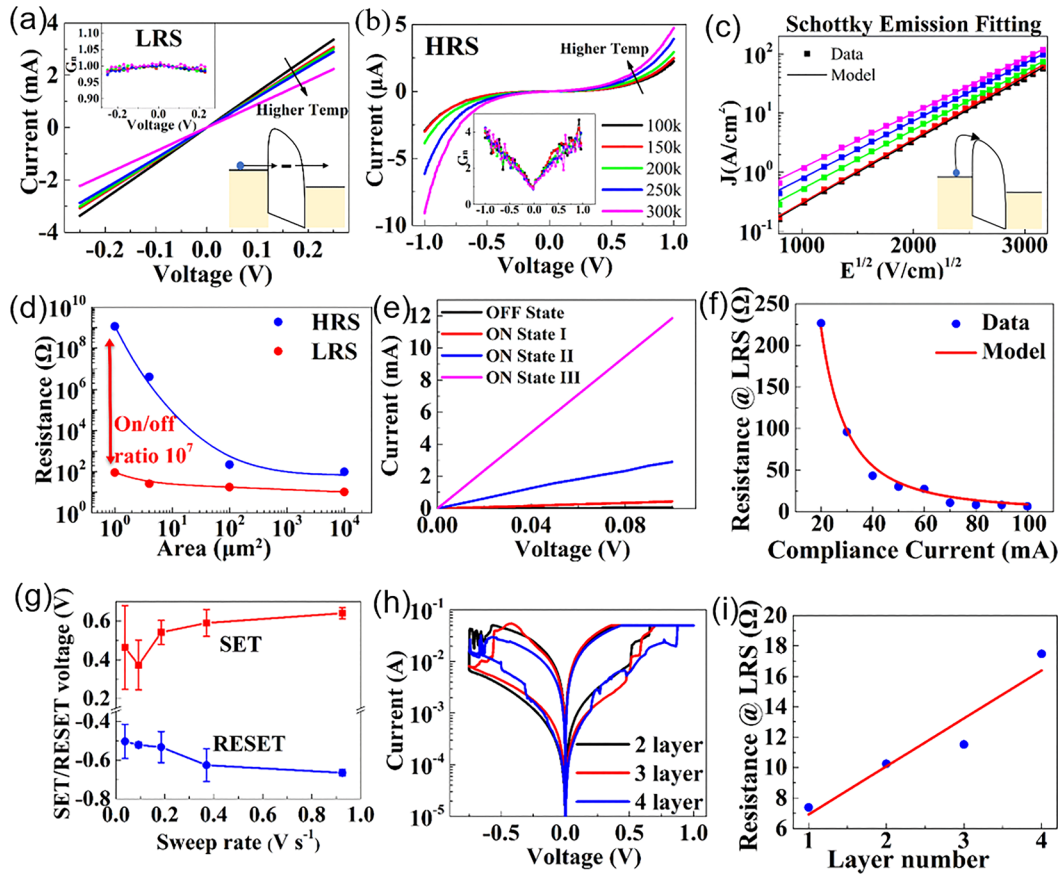


Figure 4. Dependence of temperature, area scaling, compliance current, sweep rate, and layer thickness of MoS₂ nonvolatile switching devices. (a) *I*–*V* characteristics at LRS based on MoS₂ crossbar devices at different temperatures indicating a metallic character (temperature legend is in part b). The inset shows the normalized conductance G_n and the schematic of proposed mechanism based on Ohmic direct tunneling via defect(s). (b) *I*–*V* characteristics at HRS at different temperatures. The current increases as the temperature increases. The inset shows the normalized conductance G_n . (c) Fitted data using Schottky emission model for HRS. The inset shows the schematic of the model. The device area is $2 \times 2 \mu\text{m}^2$. (d) Area-dependence of low and high resistance states with Au/1L-MoS₂/Au structure. The resistances of each state are determined at a low voltage of 0.1 V. The line curves are visual guides. (e) Dependence of the READ current on the compliance current after SET process in MoS₂ litho-free atomistor. Four separate resistance states (three ON states and one OFF state) are obtained in a single device by varying the compliance current at 20 mA (ON state I), 40 mA (ON state II) and 80 mA (ON state III). (f) Relationship between LRS resistance and compliance current indicating a sub-10 Ω resistance is achievable for RF switch applications. The fitting curve is obtained with an inverse quadratic model, $y \propto x^{-2}$. (g) Dependence of the SET and RESET voltages on the sweep rate. The area of this litho-free device is $15 \times 15 \mu\text{m}^2$. (h) Layer dependent *I*–*V* characteristics of MoS₂ litho-free MIM switches, each with an area of $15 \times 15 \mu\text{m}^2$. (i) Relationship between LRS resistance and layer number of few-layer MoS₂ litho-free devices. The straight line is a visual guide. For layer-dependent studies, the preparation method for monolayer is MOCVD and PDMS transfer, while few-layer devices are CVD-grown and wet transfer.

lithography-free and transfer-free devices are based on monolayer MoS₂ grown directly on gold foil.²⁵ Subsequently, gold top electrode is deposited using e-beam evaporation via laser shadow mask. Thus, no transfer process or lithography process is used, excluding possible residues from transfer and lithography.

For 1L-MoS₂ switches with pure Au electrodes, HRS tunnel resistance is typically ~ 0.1 – $10 \text{ M}\Omega\text{-}\mu\text{m}^2$, which is within estimates from local probe measurements.²⁶ It has been previously reported that line or grain boundary defects in polycrystalline 2D multilayers play an intrinsic role in switching.²⁷ While a possible factor in monolayers, it is not an exclusive factor as shown in Figure 3b from an MIM device realized on a single-crystal (boundary-free) CVD MoS₂, highlighting the potential role of localized effects. Also, the phenomenon is not restricted to inert electrodes since monolayer TMD with electrochemically active (Ag) electrodes^{6,12} produce NVRS as presented in Figure 3c. Moreover, monolayer graphene is also a suitable electrode option (Figure

3d). Interestingly, these results open up the design space for electrode engineering (work-function and interface redox) from inert to active metals to 2D semimetals, the latter offering the potential of atomically thin subnanometre switches for ultraflexible and dense nonvolatile computing fabrics.

To gain insight into the underlying mechanism(s), electrical measurements over five degrees of freedom, namely, temperature, area scaling, compliance current, voltage sweep rate, and layer thickness were conducted using MoS₂ as the active layer owing to its greater material maturity. The *I*–*V* characteristics at different temperatures are analyzed to explain the electron transport mechanisms at LRS and HRS. At LRS (Figure 4a), metallic Ohmic conduction can be deduced since the current decreases as the temperature increases, and the normalized conductance $G_n = (dI/dV)/(I/V)$ is approximately unity, a signature of linear transport attributed to direct tunnelling, $J \propto KV \exp\left(\frac{-4\pi d\sqrt{2m^*q}}{h}\right)$, where J is the current density, m^* is

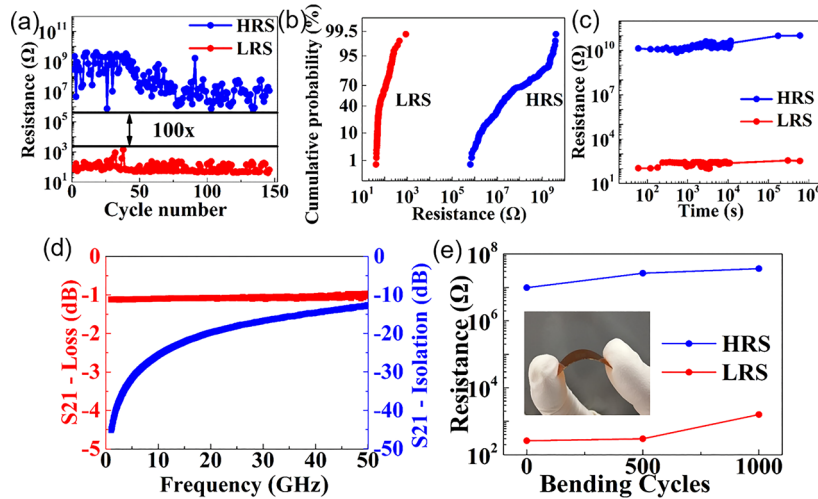


Figure 5. Representative atomristor performance. (a, b) Endurance and resistance distribution of MoS₂ crossbar MIM device with 150 manual DC switching cycles. (c) Time-dependent measurements of MoS₂ crossbar switch featuring stable retention over a week at room temperature. The resistance of the HRS and LRS is determined by measuring the current at a small bias of 0.1 V. The area of this 2L-MoS₂ crossbar device is $2 \times 2 \mu\text{m}^2$. (d) Experimental nonvolatile RF switches based on $1 \times 1 \mu\text{m}^2$ monolayer MoS₂ show promising performance with an insertion loss of ~ 1 dB and isolation of ~ 12 dB up to 50 GHz. The cutoff frequency figure of merit is ~ 1.8 THz. (e) Stable resistance of the high-resistance and low-resistance states after 1000 bending cycles at 1% strain.

the effective mass, ϕ is the tunnel barrier height, h is Planck's constant, and K is proportional to the lateral area (A) and dependent on the barrier parameters (m , ϕ , d).²⁸ d is the 2D barrier thickness. The direct tunneling model produces linear transport and is consistent with a MIM band diagram (Figure 4a). At HRS (Figure 4b), nonlinear I – V characteristics are observed, with the current increasing as the temperature increases. Considering different transport models, the HRS data were best-fitted by the Schottky emission model with good agreement (Figure 4c);²⁸ $J \propto A^* T^2 \exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\epsilon_r\epsilon_0})}{kT}\right]$,

$A^* = \frac{120m^*}{m_0}$, where A^* is the effective Richardson constant, m_0 is the free electron mass, T is the absolute temperature, q is the electronic charge, ϕ_B is the Schottky barrier height, E is the electric field across the dielectric, k is Boltzmann's constant, ϵ_0 is the permittivity in vacuum, and ϵ_r is the optical dielectric constant. The effective thickness of ~ 1 nm is used and m^*/m_0 is ~ 1 . The extracted barrier height is ~ 0.47 eV at 300 K, and the refractive index $n = \sqrt{\epsilon_r}$ is 6.84.²⁹ Considering the complexity of the interface system, further theoretical works are desired to be performed to elucidate the underlying physics.

Area scaling studies clearly show distinct profiles with the LRS relatively flat, while the HRS features a more complex relation (Figure 4d). The LRS profile is consistent with the theory of a single (or few) localized filament(s).^{6,7,9} Below $100 \mu\text{m}^2$, the HRS resistance scales inversely with area due to uniform conduction. For larger sizes, the resistance becomes area-invariant and is attributed to the presence of localized grain boundaries. We note that the average domain size of typical CVD MoS₂ monolayer is $\sim 10^2$ – $10^3 \mu\text{m}^2$. The SET/RESET voltage–area scaling is presented in Supplementary Figure 6. The current and resistance dependence on compliance current (Figure 4e,f) reveal a linear scaling that can be credited to an increase in the cross-sectional area of a single filament or to the formation of multiple filaments.⁹ On the basis of the temperature-dependent conduction experiments, the existence of Schottky barrier through TMD-metal

interface,^{30,31} and area-dependent studies, the resistance switching of MoS₂ devices can be explained by the proposed model that, in the SET process, the electrons are transported through a filamentary-like 1D conductive link, and in the RESET process, the conductive path is broken, resulting in a Schottky barrier at the device interfaces. Atomistic level elucidation of the mechanism(s) via advanced imaging and theoretical modeling is a matter of great interest and focus of further research.

For applications, such programmable resistance states are suitable for multilevel memory. In addition, the intrinsic low-resistance values, approaching $\sim 5 \Omega$ (Figure 4f), open up a new application for low-power nonvolatile electronic radio frequency (RF) switches. The dependence of the SET/RESET voltages on sweep rate (Figure 4g) suggests that slower rates afford more time for ionic diffusion resulting in reduced voltages, an important consideration for low-voltage operation. Layer-dependent studies up to four layers (Supplementary Figure 7) demonstrate that the switching phenomena persists (Figure 4h), with a distinction that the LRS resistance increases with layer number (Figure 4i).

Given the worldwide interest in layered atomic materials,^{4,32} it is important to consider potential applications. One emerging target is next-generation solid-state memory, with phase-change and TMO devices currently the leading candidates over the past decade. Atomristor devices offer distinct advantages in terms of ultimate vertical scaling, down to an atomic layer with forming-free operation. With the replacement of metal electrodes with graphene, the entire memory cell can be scaled below 2 nm. Moreover, the transparency of graphene and the unique spectroscopic features of 2D materials affords direct optical characterization for in situ studies and in-line manufacturing testing. Presently, manual endurance data (Figure 5a,b) are not yet sufficient to meet the stringent requirements for solid-state memory, a reflection of the nascent state of atomristors compared to TMO memristors, which had similar endurance ($<10^3$ cycles) in early research but has now advanced above 10^6 cycles.⁷ Oxygenation by interface engineering or doping may improve endurance, similar to what was

observed for amorphous-carbon memory devices.³³ The pulse cycling test for practical applications is an important matter that will be the focus of future studies. Retention of nonvolatile states tested up to a week (Figure 5c) is already sufficient for certain neuromorphic applications involving short and medium term plasticity.³⁴ Moreover, the subnanometre thinness of monolayers is promising for realizing ultrahigh densities. At a loose pitch of 10 nm, an atomristor density of $10^{15}/\text{mm}^3$ would provide ample room to mimic the density of human synapses ($\sim 10^9/\text{mm}^3$).³² For single-bit single-level memory storage, this corresponds to a theoretical areal density of 6.4 Tbit/in².

Nonvolatile low-power RF switches represents another major application of atomristors. Contemporary switches are realized with transistor or microelectromechanical devices, both of which are volatile with the latter also requiring large switching voltages, unideal for mobile technologies. Recently, phase-change switches have attracted interest;³⁵ however, the high-temperature melting requirements and slow switching times have limited their utility. In this light, atomristors offers an unprecedented advancement for high-frequency systems owing to its low voltage operation, small form-factor, fast switching speed, and low-temperature integration compatible with Si or flexible substrates. Initial experimental nonvolatile RF switches show promising results with acceptable insertion loss of ~ 1 dB and isolation of $\sim >12$ dB up to 50 GHz (Figure 5d). The extracted ON resistance, $R_{\text{ON}} \approx 11 \Omega$ and OFF capacitance, $C_{\text{OFF}} \approx 7.7$ fF. This results in a figure of merit (FOM) cutoff frequency, $f_{\text{co}} = 1/(2\pi R_{\text{ON}} C_{\text{OFF}}) \approx 1.8$ THz. The FOM is used for evaluating RF switches.^{35,36} Further advancements especially in terms of scaling are expected to yield significantly higher FOM (Supplementary Figure 10). Importantly, the unique combination of (approximately) area-independent LRS resistance and area-dependent HRS capacitance yields a FOM that can be scaled to 100s of THz by reduction of device area, a defining advantage over phase-change switches,^{35,36} where capacitance is proportional to width but R_{ON} , inversely dependent, hence, preventing frequency scalability without significantly compromising loss. Furthermore, the high breaking strain and ease of integration of 2D materials on soft substrates can afford flexible nonvolatile digital and analog/RF switches that can endure mechanical cycling (Figure 5e and Supplementary Figure 8).⁴

In summary, we report nonvolatile resistance switching in monolayer TMDs (MoS_2 , MoSe_2 , WS_2 , WSe_2), alluding to a universal effect in TMD monolayer films. This unexpected result in atomically thin sheets is likely due to the inherent layered crystalline nature that produces sharp interfaces and clean tunnel barriers, which prevents excessive leakage and affords stable phenomenon so that NVRS can be used for existing applications in memory/computing, and new applications in zero-power RF switching.

2D CVD Materials Preparation. CVD-synthesized monolayer MoS_2 were grown on SiO_2/Si substrates using sulfur and MoO_3 as precursors at 850 °C for 5 min.²² In addition, some monolayer MoS_2 , MoSe_2 , WS_2 , and WSe_2 samples were grown at 500 °C for 24 h by wafer-scalable MOCVD.²³ Molybdenum hexacarbonyl ($\text{Mo}(\text{CO})_6$, MHC, Sigma-Aldrich 577766), tungsten hexacarbonyl ($\text{W}(\text{CO})_6$, THC, Sigma-Aldrich 472956), diethyl sulfide ($\text{C}_4\text{H}_{10}\text{S}$, DES, Sigma-Aldrich 107247), and dimethyl selenide were the chemical precursors for Mo, W, S, and Se, respectively. Multilayer TMDs were purchased from 2Dlayer (<http://2dlayer.com/>). The growth of monolayer MoS_2 on Au foil was performed inside a

multitemperature-zone tubular furnace (Lindberg/Blue M) equipped with a 1-in.-diameter quartz tube. The sulfur powder was placed outside the hot zone, sublimated at ~ 102 °C, and then carried to the downstream growth zone by Ar gas (50 standard cubic centimeter per minute (sccm)). The MoO_3 powders (Alfa Aesar, purity 99.9%) and Au foils (Alfa Aesar, purity 99.985%, thickness $\sim 25 \mu\text{m}$) were successively placed on the downstream region of the quartz tube. The MoO_3 powders were heated from room temperature to ~ 530 °C within 30 min with a heating rate of ~ 17 °C/min. The growth pressure on Au foils was set at 30 Pa, and the growth time for 60 min at 750 °C.

2D Materials Characterization. For MoS_2 grown on SiO_2/Si substrates, Raman spectroscopy and photoluminescence were performed on a Renishaw in-Via system using a 532 nm wavelength source. Scanning electron microscope images were collected on a ZEISS Neon 40 instrument with beam at 5 kV energy. The EDX mapping was carried on a FEI Talos F200X (S)TEM running at 200 kV equipped with SuperX EDS detector. The MoS_2 grown on Au foil were systematically characterized using Raman spectroscopy (Horiba, LabRAM HR-800, excitation light ~ 514 nm), SEM (Hitachi S-4800, acceleration voltage of 1–5 kV), PL (Horiba, LabRAM HR-800, excitation light of 514 nm in wavelength), AFM (Veeco Nanoscope III), and TEM (JEOL JEM-2100 LaB6 for HRTEM; acceleration voltage of 200 kV). The UHV low temperature STM system was utilized under a base pressure better than 10^{-10} mbar. The scanning conditions are $V = 0.75$ V, $I_T = 0.20$ nA, $T = 78$ K. A modulation signal of 10 mV at 932 Hz was selected under a tunneling condition of 1.20 V, 0.20 nA. Prior to STM observations, the CVD MoS_2/Au samples were loaded into the UHV systems and degassed at about 600 K for several hours with the base pressure greater than 10^{-9} mbar.

Device Fabrication and Measurement. The crossbar device fabrication started with BE patterning by electron beam lithography and 2 nm Cr/60 nm Au metal stack deposition on a (285 nm) SiO_2/Si substrate. The litho-free device employed global electrode (2 nm Cr/60 nm Au) as BE and pure Au for the TE. Single-layer TMD was then transferred onto the fabricated substrate using polydimethylsiloxane (PDMS) stamp transfer method (Supplementary Figure 2). In this transfer process, monolayer TMD was brought into conformal contact with PDMS. Then substrate-TMD-PDMS system was soaked into diluted water. Since the original substrate (SiO_2) was hydrophilic, it was easy for water to diffuse into the TMD-substrate interface, which helped separate the two layers. The PDMS-TMD film was then brought into contact with the target fabricated substrate. The PDMS stamp was subsequently peeled off to leave monolayer TMD films on the target substrate. For crossbar devices, TE, using the same fabrication process as BE, was patterned and deposited. While for the litho-free device, the TE (60 nm Au) was deposited via a shadow mask. The devices were measured on a Cascade or Lakeshore probe station with an Agilent 4156 semiconductor parameter analyzer under ambient conditions.

RF Device Fabrication and Measurement. The 2D nonvolatile RF switch fabrication starts with patterning ground-signal-ground (GSG) pad structure for RF measurement. We used e-beam evaporation to create the ground pads and the bottom signal electrode consisting of 2 nm thick Cr and 38 nm thick Au. Synthesized monolayer MoS_2 was then transferred to the bottom signal electrode by the dry transfer method. The active MoS_2 area was defined by EBL and plasma etching. The

top signal electrode was defined by EBL and e-beam evaporation method to form the metal contacts consisting of 2 nm Cr and 38 nm Au. The top and bottom electrodes overlap dimension was $1\ \mu\text{m} \times 1\ \mu\text{m}$. Microwave switch performance was characterized up to 50 GHz using an Agilent two-port network analyzer.

■ ASSOCIATED CONTENT

■ Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.7b04342.

MoS₂ materials characterizations; schematic of transfer processes; retention time of monolayer TMDs non-volatile switches; low-voltage “Read” operations; test crossbar device without TMD active layer; dependence of SET/RESET voltage on area; characterizations of few-layer MoS₂; DMA and switching *I*–*V* curves before and after bending; current sweep SET operation of monolayer MoS₂ crossbar device; RF switch simulation results; comparison with previous works (PDF)

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: deji@ece.utexas.edu.

ORCID

Ruijing Ge: 0000-0002-0768-3057

Sushant Sonde: 0000-0002-1957-3146

Yanfeng Zhang: 0000-0003-1319-3270

Author Contributions

#Equal contribution.

Author Contributions

R.G. performed CVD growth, materials transfer, characterization, and device fabrication. X.W. carried out DC electrical measurements of 2D nonvolatile resistance switching devices. M.K. conducted RF switch fabrication and measurements. J.S. performed CVD growth and characterizations of MoS₂ on gold foil. S.S. conducted high resolution TEM measurements. L.T. contributed to sample preparation and device fabrication. R.G., X.W., J.L., and D.A. analyzed the electrical data and characteristics. R.G., X.W., and D.A. initiated the research on cross-plane nonvolatile resistance switching in single-layer atomic sheets. All authors contributed to the article based on the draft written by R.G., X.W., and D.A. Y.Z., J.L., and D.A. coordinated and supervised the research.

Notes

The authors declare no competing financial interest.

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■ REFERENCES

- (1) Qian, X.; Liu, J.; Fu, L.; Li, J. *Science* **2014**, 346 (6215), 1344–1347.
- (2) Molle, A.; Goldberger, J.; Houssa, M.; Xu, Y.; Zhang, S.-C.; Akinwande, D. *Nat. Mater.* **2017**, 16, 163.
- (3) Rivera, P.; Schaibley, J. R.; Jones, A. M.; Ross, J. S.; Wu, S.; Aivazian, G.; Klement, P.; Seyler, K.; Clark, G.; Ghimire, N. J.; Yan, J.; Mandrus, D. G.; Yao, W.; Xu, X. *Nat. Commun.* **2015**, 6, 6242.
- (4) Akinwande, D.; Petrone, N.; Hone, J. *Nat. Commun.* **2014**, 5, 5678.
- (5) Chhowalla, M.; Shin, H. S.; Eda, G.; Li, L.-J.; Loh, K. P.; Zhang, H. *Nat. Chem.* **2013**, 5 (4), 263–275.
- (6) Wouters, D. J.; Waser, R.; Wuttig, M. *Proc. IEEE* **2015**, 103 (8), 1274–1288.
- (7) Wong, H.-S. P.; Lee, H.-Y.; Yu, S.; Chen, Y.-S.; Wu, Y.; Chen, P.-S.; Lee, B.; Chen, F. T.; Tsai, M.-J. *Proc. IEEE* **2012**, 100 (6), 1951–1970.
- (8) Valov, I.; Waser, R.; Jameson, J. R.; Kozicki, M. N. *Nanotechnology* **2011**, 22 (25), 254003.
- (9) Onofrio, N.; Guzman, D.; Strachan, A. *Nat. Mater.* **2015**, 14 (4), 440–446.
- (10) Zhao, L.; Zizhen, J.; Chen, H. Y.; Sohn, J.; Okabe, K.; Magyari-Köpe, B.; Wong, H. S. P.; Nishi, Y. Ultrathin (2nm) HfO_x as the fundamental resistive switching element: Thickness scaling limit, stack engineering, and 3D integration. *2014 IEEE International Electron Devices Meeting*; IEEE, December 15–17, 2014; pp 6.6.1–6.6.4.
- (11) Tan, C.; Liu, Z.; Huang, W.; Zhang, H. *Chem. Soc. Rev.* **2015**, 44 (9), 2615–2628.
- (12) Bessonov, A. A.; Kirikova, M. N.; Petukhov, D. I.; Allen, M.; Ryhänen, T.; Bailey, M. J. A. *Nat. Mater.* **2014**, 14 (2), 199–204.
- (13) Son, D.; Chae, S. I.; Kim, M.; Choi, M. K.; Yang, J.; Park, K.; Kale, V. S.; Koo, J. H.; Choi, C.; Lee, M.; Kim, J. H.; Hyeon, T.; Kim, D.-H. *Adv. Mater.* **2016**, 28 (42), 9326–9332.
- (14) Hao, C.; Wen, F.; Xiang, J.; Yuan, S.; Yang, B.; Li, L.; Wang, W.; Zeng, Z.; Wang, L.; Liu, Z.; Tian, Y. *Adv. Funct. Mater.* **2016**, 26 (12), 2016–2024.
- (15) Qian, K.; Tay, R. Y.; Nguyen, V. C.; Wang, J.; Cai, G.; Chen, T.; Teo, E. H. T.; Lee, P. S. *Adv. Funct. Mater.* **2016**, 26 (13), 2176–2184.
- (16) Pan, C.; Ji, Y.; Xiao, N.; Hui, F.; Tang, K.; Guo, Y.; Xie, X.; Puglisi, F. M.; Larcher, L.; Miranda, E.; Jiang, L.; Shi, Y.; Valov, I.; McIntyre, P. C.; Waser, R.; Lanza, M. *Adv. Funct. Mater.* **2017**, 27, 1604811.
- (17) Tan, C.; Zhang, H. *Chem. Soc. Rev.* **2015**, 44 (9), 2713–2731.
- (18) Sangwan, V. K.; Jariwala, D.; Kim, I. S.; Chen, K.-S.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C. *Nat. Nanotechnol.* **2015**, 10 (5), 403–406.
- (19) Choi, M. S.; Lee, G. H.; Yu, Y. J.; Lee, D. Y.; Kim, P.; Hone, J.; Yoo, W. J. *Nat. Commun.* **2013**, 4, 1624.
- (20) Bertolazzi, S.; Krasnozhan, D.; Kis, A. *ACS Nano* **2013**, 7 (4), 3246.
- (21) Torsi, A.; Zhao, Y.; Liu, H.; Tanzawa, T.; Goda, A.; Kalavade, P.; Parat, K. *IEEE Trans. Electron Devices* **2011**, 58 (1), 11.
- (22) Chang, H.-Y.; Yogeesh, M. N.; Ghosh, R.; Rai, A.; Sanne, A.; Yang, S.; Lu, N.; Banerjee, S. K.; Akinwande, D. *Adv. Mater.* **2016**, 28 (9), 1818–1823.
- (23) Kang, K.; Xie, S.; Huang, L.; Han, Y.; Huang, P. Y.; Mak, K. F.; Kim, C.-J.; Muller, D.; Park, J. *Nature* **2015**, 520 (7549), 656–660.
- (24) Yanagida, T.; Nagashima, K.; Oka, K.; Kanai, M.; Klamchuen, A.; Park, B. H.; Kawai, T. *Sci. Rep.* **2013**, 3, 1657.
- (25) Shi, J.; Ma, D.; Han, G.; Zhang, Y.; Ji, Q.; Gao, T.; et al. *ACS Nano* **2014**, 8, 10196.
- (26) Fu, D.; Zhou, J.; Tongay, S.; Liu, K.; Fan, W.; Liu, T.-J. K.; Wu, J. *Appl. Phys. Lett.* **2013**, 103 (18), 183105.

- (27) Puglisi, F. M.; Larcher, L.; Pan, C.; Xiao, N.; Shi, Y.; Hui, F.; Lanza, M. 2D h-BN based RRAM devices. *2016 IEEE International Electron Devices Meeting (IEDM)*; IEEE, December 3–7, 2016; pp 34.8.1–34.8.4.
- (28) Chiu, F.-C. *Adv. Mater. Sci. Eng.* **2014**, *2014*, 18.
- (29) Liu, H.-L.; Shen, C.-C.; Su, S.-H.; Hsu, C.-L.; Li, M.-Y.; Li, L.-J. *Appl. Phys. Lett.* **2014**, *105* (20), 201905.
- (30) Kwon, J.-Y.; Lee, J.-Y.; Yu, Y.-J.; Lee, C.-H.; Cui, X.; Hone, J.; Lee, G.-H. *Nanoscale* **2017**, *9*, 6151.
- (31) Zhong, H. X.; Quhe, R.; Wang, Y. Y.; Ni, Z.; Ye, M.; Song, Z. G.; Pan, Y. Y.; Yang, J.; Yang, L.; Lei, M.; Shi, J. J.; Lu, J. *Sci. Rep.* **2016**, *6*, 21786.
- (32) Yu, S.; Kuzum, D.; Wong, H. S. P. Design considerations of synaptic device for neuromorphic computing, *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*; IEEE, June 1–5, 2014; pp 1062–1065.
- (33) Santini, C. A.; Sebastian, A.; Marchiori, C.; Jonnalagadda, V. P.; Dellmann, L.; Koelmans, W. W.; Rossell, M. D.; Rossel, C. P.; Eleftheriou, E. *Nat. Commun.* **2015**, *6*, 8600.
- (34) Indiveri, G.; Liu, S. C. *Proc. IEEE* **2015**, *103* (8), 1379–1397.
- (35) Wang, M.; Rais-Zadeh, M. J. *Micromech. Microeng.* **2017**, *27* (1), 013001.
- (36) Moon, J. S.; Hwa-Chang, S.; Le, D.; Helen, F.; Schmitz, A.; Oh, T.; Kim, S.; Kyung-Ah, S.; Zehnder, D.; Baohua, Y. 11 THz figure-of-merit phase-change RF switches for reconfigurable wireless front-ends. *2015 IEEE MTT-S International Microwave Symposium*; IEEE, May 17–22, 2015; pp 1–4.