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Novel Outphasing Power Amplifiers Designed With an Analytic Generalized Doherty–Chireix Continuum Theory

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***Abstract*— An analytic theory for dual-input outphasing power amplifiers that incorporate in one unified treatment, the continuum of solutions for power combining including the Doherty and Chireix modes is presented. This unified theory developed at the current-source reference planes reveals the performance trade-off achieved by all of the possible power amplifier (PA) combiners within the continuum of solutions. Furthermore, it identifies a novel type of dual-input hybrid Chireix–Doherty PA that combines key features of the Doherty and Chireix operations such that the fundamental drain voltages applied to both the main and auxiliary transistors remain constant. This hybrid PA relies on an input outphasing angle varying with the input power level to obtain the correct load modulation behavior. A 2-GHz dual-input hybrid Chireix–Doherty PA is implemented using nonlinear embedding and experimentally evaluated to validate the theory. A drain efficiency of 61% at 9-dB backoff power and a maximum output power of about 43 dBm are obtained for continuous-wave (CW) measurements. The efficiency increases monotonously with output power unlike that of the Doherty PA used for comparison. When excited with a 20-MHz LTE signal with 9.5-dB peak-to-average power ratio (PAPR), the dual-input PA yields a 60.0% average drain efficiency and -48.1-dBc adjacent-channel power-leakage ratio (ACLR) after linearization.**

***Index Terms*— Doherty, Chireix, outphasing, dual-input power amplifiers, continuum, nonlinear embedding.**

I. Introduction

MODERN wireless communication systems using modulated signals with high peak-to-average power ratio (PAPR) demand power amplifier (PA) architectures capable of delivering a high average efficiency. The Doherty PA architecture has been widely adopted for base station applications due to its simple implementation and enhanced average efficiency [1]–[6]. More recently, dual-input Doherty PAs [7]–[9] have been investigated to further increase the performance of Doherty PAs. Darraji et al. propose a design for the dual-input Doherty PA, which significantly improves the power added efficiency by digitally controlling the phase alignment between the carrier PA and peaking PA [9]. An alternative dual-input PA architecture which has drawn attention from PA designers is the Chireix outphasing PA [10]–[18]. Compared with the single-input outphasing PAs mentioned in [19]–[23], the dual-input outphasing PAs reported in [24]–[26] have the advantage of having more flexibility to optimize both the efficiency and linearity.

An intriguing PA design methodology has been explored in [27]–[30] by mixing the Doherty and Chireix modes of operation to benefit from both of their characteristics. A conventional pure mode Chireix PA has higher efficiency at high power regime but lower efficiency at low power regime compared with the Doherty PA [30]. A Doherty-Outphasing PA (DOPA) with an extended backoff power range was proposed and validated in [29]. The PA operates as a Doherty in the high power regime by activating both the main and peaking amplifiers. In the low power regime, the two main amplifiers connected with two quarter-wave transmission lines form a Chireix combiner by turning off the two peaking amplifiers. However, this design involves four transistors, which increases the design complexity and cost. On the contrary, in [30], the auxiliary PA is biased in class-C. In the lower power regime, the auxiliary PA turns off hence the PA operates in the Doherty mode (class-AB). The load modulation takes place in the high power regime where the PA operates in the outphasing mode. However, the outphasing operation relies on the nonlinear input impedance variation due to the single input splitter, which limits the tuning range of outphasing angles and performance compared with that of dual-input PAs. To further explore the design space of dual-input PAs, an analytic Doherty-Chireix continuum theory is developed in this paper to investigate the design of generalized dual-input outphasing power amplifiers (OPAs) as shown in Fig. 1.

The Doherty-Chireix continuum has been studied recently in [28] and [27] based on the dual-input Doherty-outphasing PA topology. Andersson *et al.* investigate the Doherty-outphasing continuum using a combiner network at current-source reference plane consisting of two transmission lines with variable electrical length and characteristic impedances in [28]. A realistic output combiner incorporating the parasitics at the package reference plane is then selected

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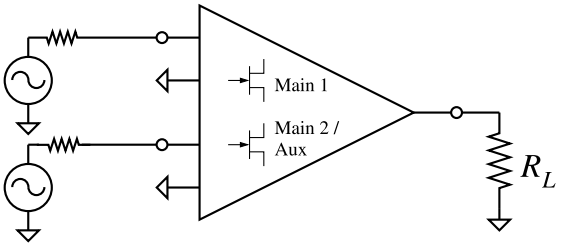

Fig. 1. Schematic of a dual-input outphasing PA (OPA).

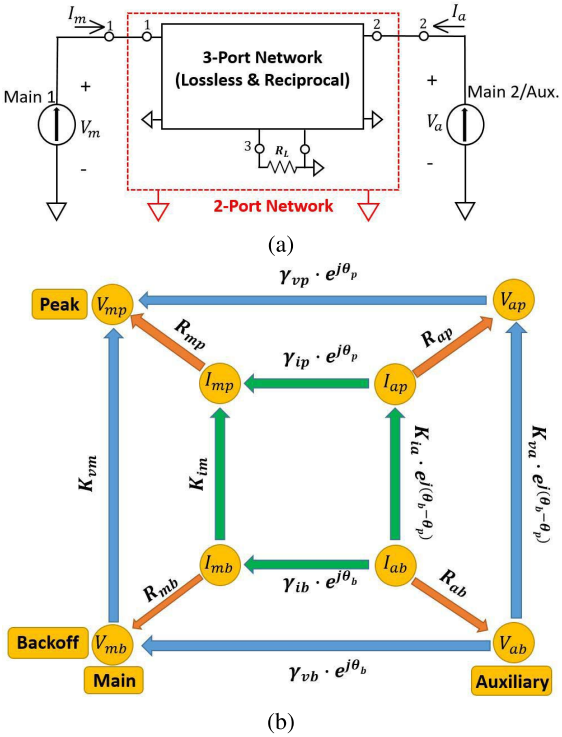

Fig. 2. (a) Dual-input OPA realized with a lossless and reciprocal three-port network (black solid-line box) terminated with a purely resistive load R_L at the current-source reference planes. (b) Mapping the connections between fundamental currents and voltages at the two-port output combiner for the main and auxiliary devices.

and optimized by using computer simulations to achieve a desired wideband performance. Differing from the method of Andersson *et al.*, in this paper we investigate the continuum in a more generalized and analytic way at the current-source reference planes by using the four current- and voltage-ratio factors: K_{vm}, K_{va}, K_{im} and K_{va},

$$|V_{mp}| = K_{vm}|V_{mb}|, \quad |V_{ap}| = K_{va}|V_{ab}|,$$
$$|I_{mp}| = K_{im}|I_{mb}|, \quad |I_{ap}| = K_{ia}|I_{ab}|.$$

which are also depicted in Fig. 2(b). The subscripts m and a refer to the main and auxiliary devices, respectively. The subscripts b and p refer to the backoff and peak power level, respectively. Meanwhile, the $V_{m/a}$ and $I_{m/a}$ refer to the fundamental voltages and currents of main and auxiliary devices, respectively. $\gamma_{v/i}$ are defined as the fundamental voltage and current ratios, respectively, between the main and auxiliary devices (Appendix I in [6]). The factors $K_{vm/a}$ and $K_{im/a}$ are referred to the peak-to-backoff power level voltage ratio (PBVR) and the peak-to-backoff power level current ratio (PBCR), respectively. The derivation of the continuum theory in this work is based on these four factors. The rationale for adopting these K factors as PA design parameters is explained in more detail below. Note that in the exceptional case of the Chireix PA the auxiliary device behaves like a secondary main device, and is thus labeled as the auxiliary/main 2 device as shown in Fig. 2(a). In this paper the main device is always on at backoff. In order to achieve a high efficiency at peak and backoff for the main PA, the fundamental peak and backoff drain voltages of the main device are set to be a) the same and b) approximately equal to the supply voltage ($|V_{mp}| = |V_{mb}| \simeq V_{DD,m}$). As a result the main PBVR K_{vm} is set to be equal to 1.

Assuming the impedances seen by the main and auxiliary devices at the current-source reference planes are real (B, F/F^{-1} or C), a two-dimensional (2D) continuum space described by K_{ia} and K_{va} covers a wide range of dual-input OPAs including Doherty and Chireix PAs. Moreover, as a byproduct of the theory presented in this paper, a new canonic dual-input Hybrid Chireix-Doherty (HCD) combiner network will be identified within the 2D Doherty-Chireix continuum. For this HCD PA the auxiliary PBVR K_{va} is also set to be equal to 1 to obtain a nearly constant fundamental drain voltage between the peak and backoff power in order to maintain a high efficiency for the auxiliary PA as well. An improved efficiency is obtained if the main PBCR K_{im} is kept small since the transconductance of the device reduces at low input RF voltages (Fig. 7(b) & 13 in [31]). Finally for the experimental verification of the theory, a HCD PA prototype will be designed at the current-source reference plane using the embedding IV device model introduced from [6] and [31]. The output combiner required at the device-package reference planes will then be readily provided by the nonlinear embedding technique introduced in [26], [32] and [35] before being implemented using physical circuits. The fabricated PA is found experimentally to exhibit an efficiency monotonously increasing with the output power in contrast to the usual double-hump efficiency of the Doherty PA.

This paper is organized as follows. In Section II, the generalized Doherty-Chireix continuum theory is introduced. The design details for the dual-input HCD PA prototype is described in Section III. Section IV presents the final implementation of the HCD PA circuit. The continuous-wave measurements and the dual-input digital pre-distortion with LTE signals are reported in Section V. Finally, the conclusions are drawn in Section VI.

II. Doherty-Chireix Continuum Theory

In this section, a generalized continuum theory for dual-input OPAs is proposed and discussed. A conceptual circuit for the lossless three-port combiner network and terminating load resistance R_L connecting the two transistors is shown in Fig. 2(a). This circuit holds only for the fundamental voltages and currents at the current-source reference planes. The Z-parameters of the two-port combiner network $\boldsymbol{Z}$ (dashed-line box), which is both reciprocal and lossy, is obtained by using the optimum fundamental currents and voltages from the main and auxiliary devices operating at both the backoff and peak power levels, respectively. The

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lossy two-port network $\boldsymbol{Z}$ is realized with a lossless three-port combiner network terminated with a resistive load R_L.

As shown in Fig. 2(a), port 1 of the two-port combiner network is connected to the main device and port 2 is connected to the auxiliary device. The two-port combiner network $\boldsymbol{Z}$ is directly derived by:

$$\boldsymbol{V} = \boldsymbol{Z}\boldsymbol{I}, \tag{1}$$

with

$$\boldsymbol{I} = \begin{bmatrix} I_{mp} & I_{mb} \\ I_{ap} & I_{ab} \end{bmatrix} \text{ and } \boldsymbol{V} = \begin{bmatrix} V_{mp} & V_{mb} \\ V_{ap} & V_{ab} \end{bmatrix}.$$

Solving (1), the Z-parameters of the two-port network $\boldsymbol{Z}$ are given by:

$$\boldsymbol{Z} = \frac{1}{\Delta} \begin{bmatrix} V_{mp}I_{ab} - V_{mb}I_{ap} & V_{mb}I_{mp} - V_{mp}I_{mb} \\ V_{ap}I_{ab} - V_{ab}I_{ap} & V_{ab}I_{mp} - V_{ap}I_{mb} \end{bmatrix}, \tag{2}$$

with

$$\Delta = I_{mp}I_{ab} - I_{mb}I_{ap}.$$

The subscript p refers to the peak power, e.g., I_{mp} is the fundamental current flowing through the main device at the peak power. Similarly, the subscript b refers to the backoff power, e.g., I_{mb} is the fundamental current flowing through the main device at the backoff power.

A. Reciprocity of the Two-Port Combiner Network

In Fig. 2(a), the two-port network is reciprocal: $Z_{12} = Z_{21}$. Based on (2), the following constrain equation is obtained:

$$V_{mb}I_{mp} - V_{mp}I_{mb} = V_{ap}I_{ab} - V_{ab}I_{ap}. \tag{3}$$

It is assumed that at the center frequency f_0, the load impedances seen by the main and auxiliary devices are both real, i.e., $Z_m = R_m$ and $Z_a = R_a$ as needed for class B, C or F operation. Therefore, the fundamental currents and voltages of the main device at peak and backoff power are given by:

$$I_{mp} = |I_{mp}|, \quad V_{mp} = |V_{mp}|, \tag{4}$$

$$I_{mb} = |I_{mb}|, \quad V_{mb} = |V_{mb}|. \tag{5}$$

In addition, the fundamental currents and voltages of the auxiliary device at peak and backoff power are given by:

$$I_{ap} = |I_{ap}|e^{-j\theta_p}, \quad V_{ap} = |V_{ap}|e^{-j\theta_p}, \tag{6}$$

$$I_{ab} = |I_{ab}|e^{-j\theta_b}, \quad V_{ab} = |V_{ab}|e^{-j\theta_b}. \tag{7}$$

where θ_b and θ_p are defined as the outphasing angles between the main and auxiliary devices at backoff and peak powers, respectively.

Plugging (4) and (7) into (3), the following identities are obtained:

$$\theta_p + \theta_b = \pi, \tag{8}$$

$$|V_{mb}||I_{mp}| - |V_{mp}||I_{mb}| = |V_{ab}||I_{ap}| - |V_{ap}||I_{ab}|. \tag{9}$$

Equ. (8) is a well-known criterion [25] which implies that the outphasing angle at peak power θ_p is determined once the outphasing angle at backoff θ_b is obtained and vice versa.

Based on (9), the asymmetry power ratio n between the auxiliary and main devices at peak power is derived as:

$$n = \frac{P_{ap}}{P_{mp}} = \frac{|V_{ap}||I_{ap}|}{|V_{mp}||I_{mp}|} = \frac{1}{\gamma_{vp}\gamma_{ip}} = \frac{1/K_{im} - 1}{1/K_{ia} - 1/K_{va}}. \tag{10}$$

Similarly, the power ratio m between the auxiliary and main devices at backoff power is also derived as:

$$m = \frac{P_{ab}}{P_{mb}} = \frac{|V_{ab}||I_{ab}|}{|V_{mb}||I_{mb}|} = \frac{1}{\gamma_{vb}\gamma_{ib}} = \frac{K_{im} - 1}{K_{ia} - K_{va}}. \tag{11}$$

Therefore, the overall peak ($P_{o,p}$) and backoff ($P_{o,b}$) RF powers delivered to the two-port network are equal to the summation of the peak and backoff powers at ports 1 and 2. Using (10) and (11), the overall peak and backoff output powers in terms of the peak and backoff output powers of the auxiliary or main devices are given by:

$$P_{o,p} = \begin{cases} P_{ap}\left(1 + \dfrac{1}{n}\right) \text{ with } P_{ap} = \dfrac{1}{2}|V_{ap}||I_{ap}| & \text{for } n \geqslant 1 \\ P_{mp}\,(1+n) \text{ with } P_{mp} = \dfrac{1}{2}|V_{mp}||I_{mp}| & \text{for } n < 1, \end{cases} \tag{12}$$

$$P_{o,b} = \begin{cases} P_{ab}\left(1 + \dfrac{1}{m}\right) \text{ with } P_{ab} = \dfrac{1}{2}|V_{ab}||I_{ab}| & \text{for } n \geqslant 1 \\ P_{mb}\,(1+m) \text{ with } P_{mb} = \dfrac{1}{2}|V_{mb}||I_{mb}| & \text{for } n < 1. \end{cases} \tag{13}$$

Given the peak and the backoff powers, the peak to backoff power ratio (PBPR) is calculated by:

$$\text{PBPR} = \frac{P_{o,p}}{P_{o,b}} = K_{va}K_{ia}\frac{1 + \frac{1}{n}}{1 + \frac{1}{m}}. \tag{14}$$

Based on this derivation, it is noted that the PBPR is related to the auxiliary PBVR K_{va}, auxiliary PBCR K_{ia}, n and m factors.

In a RFIC process the main and auxiliary transistors can be sized as desired and n gives the relative sizing of these devices. For the case where the two devices are of the same size as is often true for packaged devices, it is useful to introduce the following normalized output power for a figure of merit:

$$\overline{P}_{o,peak} = \frac{P_{o,peak}}{2\ P_{max}(n)} = \begin{cases} \dfrac{1}{2}\left(1 + \dfrac{1}{n}\right) & n \geqslant 1 \\ \dfrac{1}{2}\,(1+n) & n < 1. \end{cases} \tag{15}$$

where the single-device maximum output power is defined by $P_{max}(n) = |V_{ap}||I_{ap}|/2$ if $n \geqslant 1$, or $P_{max}(n) = |V_{mp}||I_{mp}|/2$ if $n < 1$. Thus $P_{max}(n)$ is the power of the devices (main or auxiliary) providing the most power when the dual-input OPA is operating at peak power. For equal size devices, $\overline{P}_{o,peak} = 1$ is the optimal value for this figure of merit. Note that in all design cases, selecting $\gamma_{vp} = 1$ is also usually desired for the main and auxiliary devices to operate with approximately the same fundamental maximum drain voltage $|V_{ap}| = |V_{mp}| \simeq V_{D,max}/2$ for maximum output power. An exception is for technologies for which trapping increases the IV knee voltage when the main device operates at high drain voltages. In such a case, it is best for the main transistor which is always on, to operate with a smaller peak drain voltage than that of the auxiliary device ($\gamma_{vp} > 1$).

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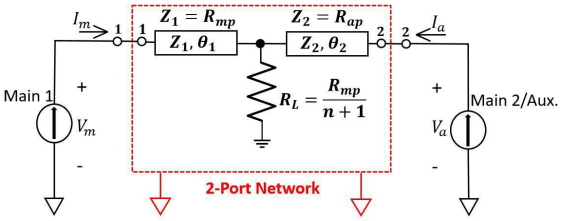

Fig. 3. Dual-input OPA prototype realized with two transmission lines connected with a resistive load. The characteristic impedance Z_1, Z_2, the electrical length θ_1, θ_2 and the resistive load R_L are provided by the continuum theory.

B. Losslessness of the Three-Port Combiner Network

The reciprocal lossy two-port combiner seen by the transistors of the OPA at their drain terminals consists of a three-port network terminated by a resistive load as shown in Fig. 2(a). Applying the condition for a lossless and reciprocal three-port network found in [3], [32] and [25], which is $\mathcal{R}^2\{Z_{12}\}=\mathcal{R}\{Z_{11}\}\mathcal{R}\{Z_{22}\}$, an analytic equation is obtained for the outphasing angle at backoff power:

$$\cos^2\theta_b = \frac{(K_{ia}-1)(K_{im}-K_{va})}{(K_{im}+1)(K_{ia}+K_{va})}. \tag{16}$$

This equation yields four possible analytic solutions for the outphasing angles at both the backoff and peak power levels:

$$\theta_b = \pm\cos^{-1}\left(\pm\sqrt{\frac{(K_{ia}-1)(K_{im}-K_{va})}{(K_{im}+1)(K_{ia}+K_{va})}}\right), \tag{17}$$

$$\theta_p = \pi - \theta_b. \tag{18}$$

However, one can verify that the sign does not affect the load modulation and the resulting efficiency [3]. In this paper, a positive sign is selected to calculate the outphasing angle at backoff power. It is found that given a fixed value for the PBVR and PBCR of both the main and auxiliary devices, the peak power, PBPR and outphasing angle can be obtained immediately. For example, in a Doherty combiner K_{ia} is equal to K_{im} due to the $\lambda/4$ inverter separating them. Therefore, in this case (17) and (18) yield: $\theta_b = \theta_p = 90°$, which matches the definition for the conventional Doherty combiner.

The impedances seen by the devices at peak and backoff powers are defined as $R_{mp} = V_{mp}/I_{mp}$ and $R_{mb} = V_{mb}/I_{mb}$ for the main and $R_{ap} = V_{ap}/I_{ap}$ and $R_{ab} = V_{ab}/I_{ab}$ for the auxiliary, respectively. Applying the condition of losslessness and reciprocity for the three-port combiner network to (2), the Z parameters reduces to:

$$\begin{aligned}
Z_{11} &= \frac{\cos\theta_b R_{mb}(1+K_{ia}) + j\sin\theta_b R_{mb}(K_{ia}-1)}{\cos\theta_b(K_{ia}+K_{im}) + j\sin\theta_b(K_{ia}-K_{im})},\\
Z_{12} &= \frac{K_{ia}(K_{im}-1)R_{ap}/\gamma_{vp}}{\cos\theta_b(K_{ia}+K_{im}) + j\sin\theta_b(K_{ia}-K_{im})},\\
Z_{22} &= \frac{\cos\theta_b R_{ab}(K_{im}+K_{va}) + j\sin\theta_b R_{ab}(K_{va}-K_{im})}{\cos\theta_b(K_{ia}+K_{im}) + j\sin\theta_b(K_{ia}-K_{im})}.
\end{aligned} \tag{19}$$

In the case where the main and auxiliary fundamental peak voltages are selected to be equal, which is $\gamma_{vp} = 1$ in (19), the general passive two-port combiner can be realized using a resistive load $R_L = R_{mp}/(n+1)$ and two transmission lines as shown in Fig. 3 with, respectively, characteristic impedances $Z_1 = R_{mp}$, $Z_2 = R_{ap}$, and electrical lengths θ_1 and θ_2 with:

$$\begin{aligned}
\tan\theta_1 &= \frac{K_{im}(K_{ia}-1)}{K_{ia}+K_{im}}\tan\theta_b,\\
\tan\theta_2 &= \frac{K_{ia}(K_{va}-K_{im})}{K_{va}(K_{ia}+K_{im})}\tan\theta_b.
\end{aligned}$$

By sweeping the three variables K_{im}, K_{ia} and K_{va} in (10), (11), and (15), there exists a three dimensional continuum that includes all possible solutions for the dual-input OPA combiners. In this paper we are interested in comparing PAs exhibiting the same PBPR to obtain a high average efficiency for signals with a large backoff output power range. Under such conditions, the PBPR becomes then an input parameter and (14) establishes a relationship between K_{im}, K_{ia} and K_{va}. For a given PBPR, the main PBCR K_{im} obtained from (14) is:

$$K_{im} = \frac{\text{PBPR}\,(1+K_{va}-K_{ia}) - K_{va}K_{ia}}{\text{PBPR} - K_{va}K_{ia} + K_{va} - K_{ia}}. \tag{20}$$

By only considering dual-input OPAs with the same PBPR and featuring a main PA always operating at high-efficiency ($K_{vm} = 1$), the design space for the dual-input OPA combiners is now reduced from a 3D to 2D continuum of possible solutions with K_{ia} and K_{va} the two independent variables. This 2D continuum of solutions covers a wide range of dual-input OPAs including the Doherty and Chireix PAs.

To visualize this 2D continuum, the outphasing angle given by (17) and the required main PBCR K_{im} given by (20) are plotted in Fig. 4(a) and (b) respectively for a PBPR of 9.54 dB and $K_{ia} \in [9, 100]$ and $K_{va} \in [1, 3]$. The corresponding normalized peak power $\overline{P}_{o,peak}(n)$ given by (15) and the asymmetry power ratio n given by (10) are also plotted in Fig. 4(c) and (d), respectively.

When $K_{ia} = \infty$ (or large enough to turn off the auxiliary at backoff, in this section $K_{ia} = 100$ is selected for numerical modeling) and $K_{va} = K_{im}$ (requires an $\lambda/4$ inverter) a Doherty PA mode is implemented. For $K_{ia} = 100$ and $K_{va} = K_{im} = 3$, a Doherty PA mode (Doherty label in Fig. 4) with an asymmetry power ratio of $n = 2$ (see Fig. 4 (d)) and a PBPR of 9 (9.54 dB) is realized. The outphasing angles at both peak and backoff are 90° as expected in Fig. 4(a). The main PBCR K_{im} is equal to $n + 1 = 3$ and the normalized peak power $\overline{P}_{o,peak}$ is 0.75 as shown in Fig.4(b) and (c), respectively.

When $K_{ia} = K_{im} = \text{PBPR}$ and $K_{va} = 1$ a Chireix PA mode is implemented. For $K_{ia} = K_{im} = 9$ (Chireix label in Fig. 4), a Chireix PA mode with a PBPR of 9 (9.54 dB) is realized. The required outphasing angle at backoff power is 36.9° as seen in Fig. 4(a). For all values of the PBPR, the Chireix PA exhibits symmetric power ratios ($n = m = 1$) and a normalized peak power $\overline{P}_{o,peak}$ equal to 1 as shown in Fig. 4(c). Note that a normalized peak power $\overline{P}_{o,peak} = 1$ is the maximum value possible in dual-input OPAs. Indeed the main and auxiliary transistors should be of equal size in a Chireix PA, so that the two devices can deliver the same output powers at peak and backoff.

A novel HCD PA mode is obtained by setting $K_{va} = 1$ and $K_{ia} = \infty$. For $K_{im} = 5$ a HCD PA (HCD label

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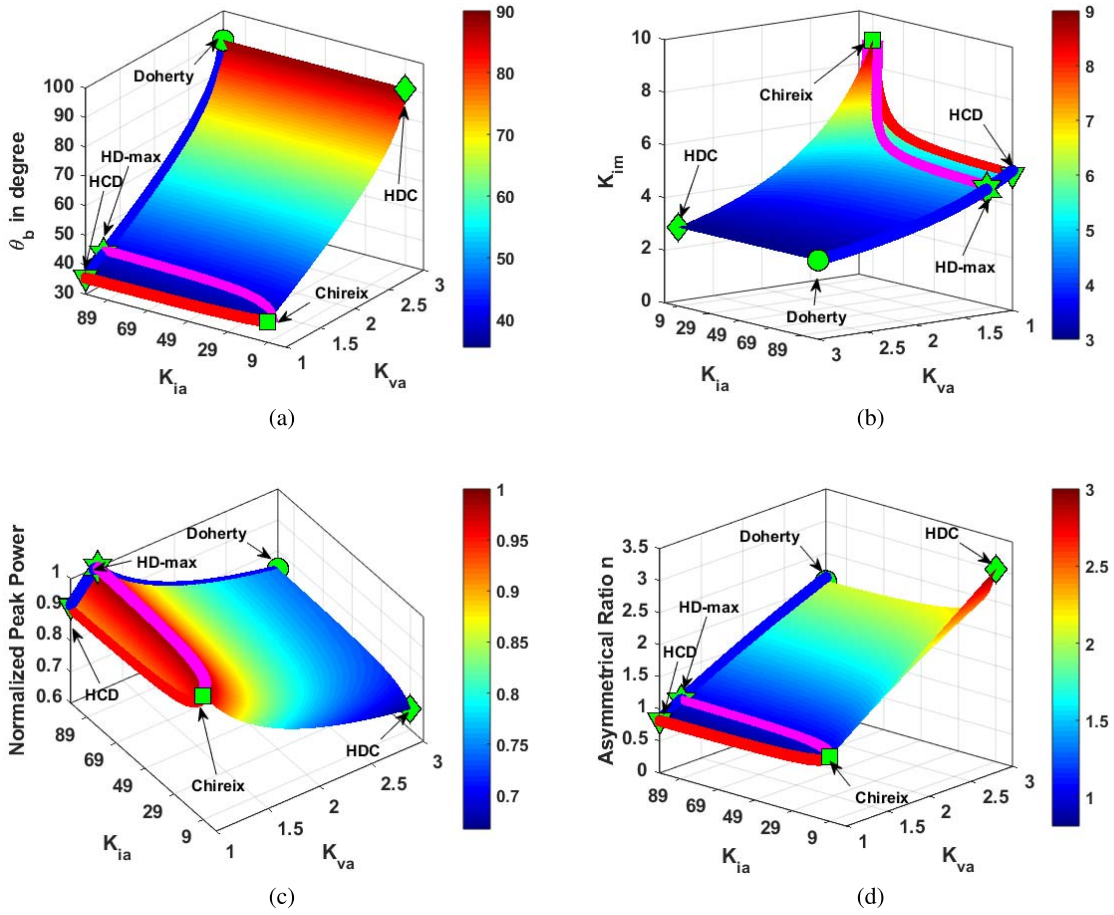

Fig. 4. Numerical modeling results based on the proposed continuum theory given PBPR=9.54 dB. (a) outphasing angle at backoff power θ_b, (b) PBCR of the main device K_{im}, (c) normalized peak power $\overline{P}_{o,peak}$, and (d) asymmetric power ratio n. The blue line shows the transition from Doherty to HCD, the red line shows the transition from Chireix to HCD and the purple line shows the transition from Chireix to HD-max.

in Fig. 4) with a PBPR of 9 is realized (see Fig. 4(b)). The required outphasing angle at backoff power is 35.3° as seen in Fig. 4(a). In this HCD PA, the fundamental drain voltages $|V_{ap}|$ and $|V_{ab}|$ presented to the auxiliary transistor at peak and backoff are kept the same by setting $K_{va} = 1$. As a result, the efficiency of the auxiliary PA is substantially increased between peak and backoff compared to the Doherty mode of operation where the inverter sets $K_{va} = K_{im} = 3$, leading to a reduced drain-voltage swing and efficiency near backoff. Also the main PBCR K_{im} of 5.5 for the HCD PA compared to 9 for the Chireix PA is known to improve the main efficiency at backoff (Fig. 7(b) & 13 in [31]). However, similarly to the Doherty mode of operation, the auxiliary PBCR K_{ia} is set to be sufficiently large (100 here) in the HCD PA to almost turn off the auxiliary device at backoff power. This differs from the conventional Chirex mode of operation which always keeps the same operation for the two devices by setting $K_{ia} = K_{im}$.

Note that another type of canonic Hybrid PA mode noted Hybrid Doherty-Chireix (HDC) is obtained for $K_{ia} = \text{PBPR}$ and $K_{va} = K_{im} = \sqrt{\text{PBPR}}$. This Hybrid PA is labeled as HDC in Fig. 4 in the 2D continuum. Like the Doherty mode, the HDC mode requires the same peak and backoff outphasing angle of 90° and use the same main PBCR of $K_{im} = 3$. Like the Chireix PA, the HDC model relies also on the same PBCR $K_{ia} = 9$ for the secondary main which remains partially on at backoff. The HDC mode is thus exhibiting a lower efficiency for the secondary main (auxiliary) at backoff, since it relies on a large auxiliary PBVR K_{va} of 3 while the auxiliary PBCR K_{ia} of 9 indicates the device is not fully off at backoff. A lower efficiency is thus expected at backoff for the alternative HDC mode compared to the HCD mode. Beside the HDC mode, it can be verified that all the modes between the Doherty and the HDC modes which verify $K_{va}^2 = K_{im}^2 = \text{PBPR}$, exhibit the same peak and backoff outphasing angle of 90° independently of the value of K_{ia}. Thus they can all be implemented as single-input PAs since $\theta_b = \theta_p$.

An example for a high PBPR of $B = 9 = 9.54$ dB is also given in Table I. The Doherty PAs exhibit the lowest normalized peak power $\overline{P}_{o,peak}$ compared with the Chireix PAs and HCD PAs when two transistors of equal size are used. Since the asymmetry power ratio verifies $n > 1$ for the Doherty combiner with 9.54 dB PBPR, the auxiliary device delivers the most power at peak power. On the contrary the asymmetry power ratio verifies $n < 1$ for the HCD combiner for the same PBPR, and the main device delivers the most power at peak power. The Chireix combiner always provides $n = 1$ for all PBPR values and thus the normalized peak power $\overline{P}_{o,peak}$ remains at its maximum value of 1. However this is not the only PA solution maximizing $\overline{P}_{o,peak}$. It is observed in Fig. 4 that there is a trajectory for K_{ia} versus K_{va} indicated

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TABLE I
COMPARISON OF CANONIC DUAL-INPUT POWER AMPLIFIERS

PA	K_{vm}	K_{im}	K_{va}	K_{ia}	$\overline{P}_{o,peak}$	PBPR	n	θ_b	R_{mp}	R_{mb}	R_{ap}	R_{ab}
Doherty	1	$\sqrt{B}$	$\sqrt{B}$	∞	$\frac{0.5\sqrt{B}}{\sqrt{B}-1}$	B	$\sqrt{B}-1$	$90°$	$\frac{\gamma_{vp}}{\gamma_{ip}}R_{opt}$	$\sqrt{B}\frac{\gamma_{vp}}{\gamma_{ip}}R_{opt}$	R_{opt}	∞
	1	3	3	∞	0.75	9	2	$90°$				
Chireix	1	B	1	B	1	B	1	$\cos^{-1}\left(\pm\frac{B-1}{B+1}\right)$	R_{opt}	BR_{opt}	R_{opt}	BR_{opt}
	1	9	1	9	1	9	1	$36.9°$				
Hybrid	1	$\frac{B+1}{2}$	1	∞	$\frac{B}{B+1}$	B	$\frac{(B-1)}{(B+1)}$	$\cos^{-1}\left(\pm\sqrt{\frac{B-1}{B+3}}\right)$	R_{opt}	$\frac{B+1}{2}R_{opt}$	$\frac{\gamma_{ip}}{\gamma_{vp}}R_{opt}$	∞
(HCD)	1	5	1	∞	9/10	9	8/10	$35.3°$				
Hybrid	1	$\sqrt{B}$	$\sqrt{B}$	B	$(0.5+\frac{0.5}{\sqrt{B}})$	B	$\sqrt{B}$	$90°$	$\frac{\gamma_{vp}}{\gamma_{ip}}R_{opt}$	$\sqrt{B}\frac{\gamma_{vp}}{\gamma_{ip}}R_{opt}$	R_{opt}	$\sqrt{B}R_{opt}$
(HDC)	1	3	3	9	2/3	9	3	$90°$				
HD-max	1	$\frac{B}{2}$	$\frac{B}{B-2}$	∞	1	B	1	$\cos^{-1}\left(\pm\sqrt{\frac{B^2-4B}{B^2-4}}\right)$	R_{opt}	$\frac{B}{2}R_{opt}$	R_{opt}	∞
	1	4.5	9/7	∞	1	9	1	$40.1°$				

by the purple line for which the asymmetry power ratio $n = 1$ such that the normalized peak power $\overline{P}_{o,peak}$ remains at its maximum value of 1. This trajectory connects to the Chireix mode for $K_{ia} =$ PBPR and the Doherty-HCD (blue line) for $K_{ia} = \infty$ (or large). The relation between K_{va} and K_{ia} for this trajectory is given by:

$$K_{va} = \frac{\text{PBPR}(K_{ia} - 1)}{\text{PBPR} + K_{ia}(\text{PBPR} - 2)}.$$

The type of OPA with $K_{ia} = \infty$ (or sufficiently large) and $n = 1$ is the preferred choice to maximize the output power when equal size devices are used. In this paper, it is referred as HD-max PA and labeled as HD-max in Fig. 4. This mode features a $K_{va} = 9/7$ close to the ideal $K_{va} = 1$ in the HCD mode and a favorably smaller K_{im} of 4.5 compared to 9 and 5 in the Chireix and HCD modes, respectively. These two features provide for an improved efficiency between peak and backoff for the auxiliary and main PAs, respectively. To highlight some of the key features of this Doherty-Chireix continuum theory, the design parameters and performance for the Doherty, Chireix, HCD, HDC and HD-max combiners are summarized in Table I.

The initial design-space for the continuum theory starts with ten parameters, namely the eight amplitudes ($|V_{mp}|$, $|V_{mb}|$, $|V_{ap}|$, $|V_{ab}|$, $|I_{mp}|$, $|I_{mb}|$, $|I_{ap}|$, and $|I_{ab}|$) of the voltages and currents for the main and auxiliary devices at peak and backoff and the two outphasing angles (θ_p and θ_b). The reciprocity and losslessness of the output combiner introduce three constraints based on (8), (9), and (17). The maximum device drain voltage $V_{D,max}$ and current $I_{D,max}$ introduce two more constraints. Keeping the main device operating at high efficiency with $K_{vm} = 1$ introduces one constraint. The main-to-auxiliary peak-voltage ratio γ_{vp} selected by the designer introduces one constraint. Furthermore targeting an OPA with a specific PBPR sets another constraint defining K_{im} in (20). It results that the design space for high-efficiency OPAs has now reduced to 2D with K_{va} and K_{ia} the two independent variables. Analytic formula for a) the outphasing angles θ_p and θ_b, b) the asymmetry factor n, c) the output power $P_{o,peak}$, and d) the main PBCR K_{im} were derived in terms of K_{va}, K_{ia} and PBPR in this section. With K_{im} and n available, all the remaining eight amplitudes $|V_{mp}|$, $|V_{mb}|$, $|V_{ap}|$, $|V_{ab}|$, $|I_{mp}|$, $|I_{mb}|$, $|I_{ap}|$, and $|I_{ab}|$ at the current-source reference planes are then analytically provided by this Doherty-Chireix continuum theory using the design parameters, K_{va}, K_{ia}, PBPR, $V_{D,max}$, $I_{D,max}$ and γ_{vp} selected by the PA designer. The Z-parameters of the combiner circuit are then given by (19). In the next section, the efficiency of the dual-input OPAs within the Doherty-Chireix continuum is investigated in more detail to provide backup for the above theoretical analysis.

C. Numerical Modeling for the Efficiency Behaviors of Dual-Input OPAs Based on the Doherty-Chireix Continuum

In this section numerical calculations of the drain efficiency at the current-source reference planes are presented for a simple transistor IV model, in order to substantiate the design guidelines introduced in the previous section, for optimizing the drain efficiency and maximum output power within the Doherty-Chireix continuum. For these simulations, the transistor is modeled using the following piece-wise linear IV characteristics with a constant transconductance and a non-zero knee voltage:

$$I_{DS}(v_{GS}, v_{DS}) = g_m \cdot \max[0, v_{GS} - V_{th}] \cdot \min\left[\frac{v_{DS}}{V_{on}}, 1\right]. \tag{21}$$

where v_{GS} refers to the instantaneous gate voltage and v_{DS} refers to instantaneous drain voltage. In (21), g_m, V_{th} and V_{on} refer to the device transconductance, the threshold voltage and the knee voltage of the IV model, respectively. In this example, V_{th} is set to be -3 V and V_{on} to be 2 V. The drain efficiencies obtained for various PAs inside of the Doherty-Chireix Continuum are numerically computed and plotted versus output power in Fig. 5. This analysis is under the assumption that the main device is operated in class-B and the auxiliary device in class-B/C depending on mode of the dual-input OPAs. The gate bias of the auxiliary device is determined by the conduction angle at backoff (Appendix II in [6]). Thus for these modeling, the auxiliary device for the dual-input OPA is biased in class-B for the Chireix mode and in class-C for the Doherty or HCD modes. The outphasing angles at peak θ_p, backoff θ_b and the output combiner network can be easily determined by (17), (18) and (19), respectively. The auxiliary device is assumed to verify $I_{D,max}/2 \simeq |I_{ap}| = 1$ A, $V_{D,max}/2 = |V_{ap}| = 30$ V and the input coupling ratio is $\gamma_{ip} = \gamma_{vp}/n = 1$. Note that the outphasing angle is linearly increased with the input RF voltage drive from backoff to peak, to implement a mixed-mode outphasing operation at

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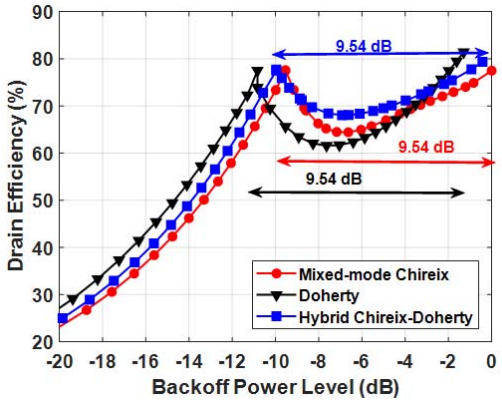
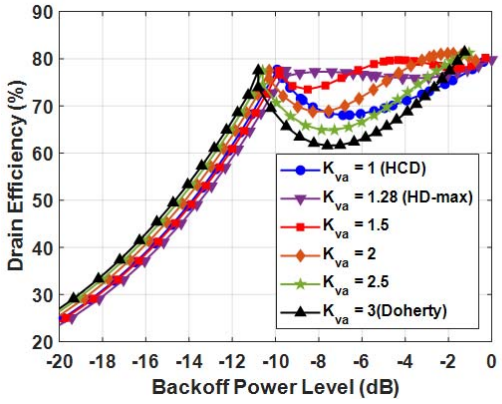


(a)



(b)

Fig. 5. Drain efficiency results based on the piece-wise linear IV model. (a) Drain efficiency versus backoff power range for the mixed-mode Chireix, Doherty, and HCD PAs. (b) Drain efficiency versus backoff power range for various K_{va} given the same 9.54 dB PBPR and $K_{ia} = 100$.

the current-source reference planes. The drain efficiency is calculated using:

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{\mathcal{R}\{V_m I_m^*\}/2 + \mathcal{R}\{V_a I_a^*\}/2}{V_{DC,m} I_{DC,m} + V_{DC,a} I_{DC,a}}, \tag{22}$$

where V_m, V_a, I_m and I_a refer to the RF fundamental drain voltages and currents for the main and auxiliary PA, respectively. $V_{DC,m}$, $V_{DC,a}$, $I_{DC,m}$ and $I_{DC,a}$ refer to the DC drain voltages and currents for the main and auxiliary PA, respectively. The currents $I_{DC,m}$ and $I_{DC,a}$ are numerically calculated using harmonic balance.

Fig. 5(a) compares the drain efficiency versus output power for three types of PAs: HCD, mixed-mode Chireix, and Doherty PAs. The three PAs are modeled with the same PBPR of 9.54 dB. As suggested by Table I for the same PBPR (B), the Chireix PA achieves the highest maximum output power while the Doherty PA achieves the lowest. Furthermore, compared to the Doherty PA, both of the Chireix and HCD PAs exhibit a flat efficiency dependence on the output power at high power, which is expected to result in higher average efficiency for modulated input signals. Even though the efficiency response versus output powers of the HCD and Chireix PAs are similar for the same PBPR of 9.54 dB, the corresponding PBCR K_{im} of the main transistor is equal to 5 in the HCD PA compared to 9 in the Chireix PA. Thus when the HCD PA is at backoff, the main PA transistor does not operate near the threshold region, where the device transconductance is in practice substantially reduced compared to that of the constant-transconductance model used here.

To further investigate the efficiency performance versus output power within the Doherty-Chireix continuum, Fig. 5 (b) shows the efficiency versus power of the dual-input OPA as the operation is shifted from Doherty PA to HCD PA while keeping the auxiliary PA almost turned off ($K_{ia} = 100$). It is observed that the efficiency drop between backoff and peak output powers is gradually suppressed as the auxiliary PBVR K_{va} decreases from 3 (Doherty) to 1 (HCD), while keeping the PBPR at 9.54 dB. The peak power in Fig. 5(b) increases by 0.84 dB as the PA design shifts from Doherty to HCD with a maximum increase reaching 1.29 dB (33%) at the HD-max mode (Table I). To simplify the numerical modeling process, in Fig. 5 the main device operates in class-B and the auxiliary device operates in class-C. The same harmonic terminations are applied for all the modes shown in Fig. 5(a) and (b).

In summary, the variation of the efficiency versus output power is numerically evaluated for various modes in the Doherty-Chireix continuum theory using a simple constant g_m piece-wise linear model. As expected, the HCD PA exhibits the advantage of a higher drain efficiency in the high power regime between the backoff and peak powers compared to the Doherty PA. This feature will be experimentally investigated in section V. In addition, the HCD PA is seen to be theoretically able to deliver a higher peak power given the same peak-to-backoff power ratio of 9.54 dB. In the next section, the design and simulation of an ideal HCD PA prototype will be pursued using a realistic transistor device model.

III. Design of Dual-Input Hybrid Chireix-Doherty Prototype

In the Doherty-Chireix continuum theory presented in the previous sections, a new type of dual-input HCD PA mode has been proposed at the current-source reference planes. In this section, the dual-input HCD PA prototype is designed and simulated using the Angelov embedding device model reported in [31] and [6]. This embedding device model provides realistic Angelov IV characteristics for the intrinsic simulations at the current-source reference planes while at the same time calculating the voltages and currents at the package reference planes which sustain that intrinsic mode of operation. Note that the design of PAs using nonlinear embedding [33] and [31] accounts for the linear parasitics, the nonlinear capacitances and current sources in the device model. The projected voltages and currents obtained at the package reference planes provide then the two-port Z-parameters of the combiner as well as the fundamental and harmonic impedances of the source and load termination networks.

A. Design Methodology

The prototype HCD PA to be designed with the embedding device model is shown in Fig. 6(b). An operation frequency of 2 GHz is selected. The overall peak output power for the prototype HCD PA $P_{o,p}$ is selected to be 43.5 dBm.

For this design K_{ia} is set to 50, together with $K_{vm} = 1$ and $K_{va} = 1$ as needed for implementing an HCD mode.

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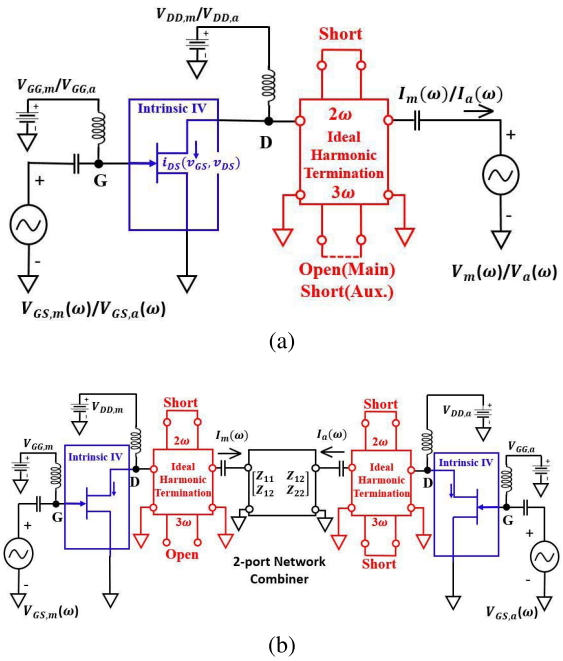

Fig. 6. Schematic of (a) a single transistor PA terminated with an RF voltage source and (b) HCD PA prototype applied with an ideal two-port output combiner network. The embedding device model at the current-source reference plane is used (in the blue boxes).

$K_{im} = 6.5$ is selected using (20) as it yields on a PBPR close to 10 dB. Using (10) and (11) the asymmetric power ratios n of 0.863 and m of 0.112 are obtained at peak and backoff powers, respectively. Based on (14) and (17), the exact PBPR is 10.37 dB and the backoff outphasing angle θ_b is $\pm 33°$. In this demonstration, the positive solution of the outphasing angle is selected. The design of the main and auxiliary amplifiers is presented next. The main and auxiliary peak and backoff output powers P_{mp}, P_{ap}, P_{mb} and P_{ab} are given by (12) and (13), respectively.

In the first step, the main PA is designed. As shown in Fig. 6(a), the main transistor is operated in ideal class F at the current-source reference planes. The second and the third harmonic currents are terminated by short and open harmonic terminations, respectively, using an ideal triplexer. The gate bias is equal to the device model threshold voltage V_{th}. The transistor is driven by a gate voltage source $V_{GS,m} = -|V_{GS,m}|$ and a drain voltage source $V_{DS,m} = |V_m| = |V_{mp}| = |V_{mb}|$ at the fundamental frequency. A 2D parametric sweep is performed with the input RF voltage drive $|V_{GS,m}|$ swept from 0.5 V to 4.5 V and the drain voltage source $|V_m|$ swept from 21 V to 31 V to select the optimal large-signal operating point at peak and backoff. The resulting drain efficiency of the main PA at the package reference planes calculated by the embedding device model is plotted in Fig. 7(a) versus the output power for the different $|V_{GS,m}|$ and $|V_m|$. Multiple design choices are possible based on the results shown in Fig. 7(a). The green circles indicate the maximum output power which is obtained for $|V_{GS,m}| = 4.5$ V. The green stars indicate the corresponding main PA efficiency at the backoff power P_{mb} given by (13). If the output power is to be maximized, a fundamental drain voltage $|V_m|$ of 31 V can be selected as it yields the highest main peak

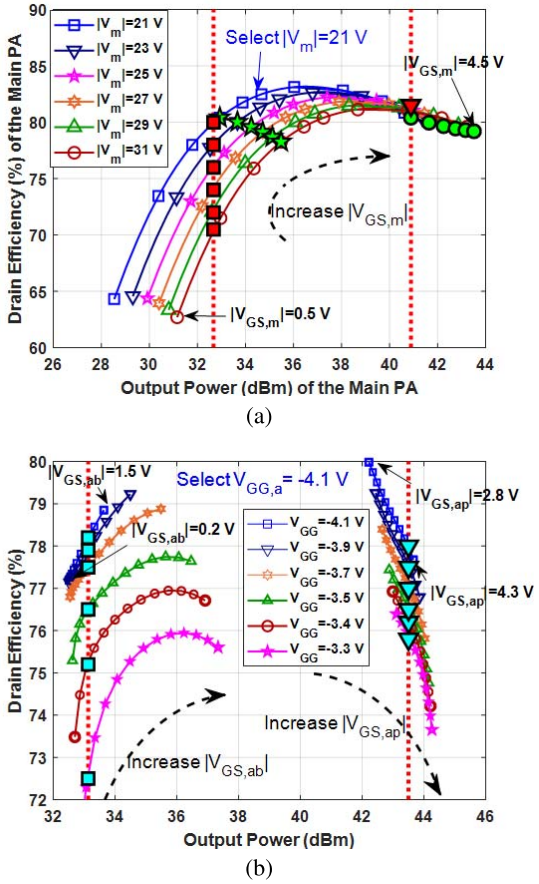

Fig. 7. (a) Simulated efficiency of the main PA versus RF input voltage drive $|V_{GS,m}|$ for different drain voltage drive $|V_m|$ and (b) simulated overall PA efficiency versus the gate voltage drive $|V_{GS,a}|$ for different DC gate bias V_{GG} of the auxiliary PA. The simulations are performed using the schematic shown in Fig. 6 (a). The intrinsic embedding device model is used in the blue box to calculate the efficiency at the package reference planes.

power P_{mp} with an acceptable backoff efficiency. If a specific output power is targeted, an alternative approach is to select the peak power and determine the fundamental drain voltage maximizing the backoff drain efficiency. The drain efficiencies associated with fixed peak and backoff powers are depicted by the vertical red triangular and rectangular markers as shown in Fig. 7(a). In this paper, the latter approach is adopted. Thereby a fundamental drain voltage $|V_m| = 21$ V and the drain bias $V_{DD,m} = 18$ V are selected as it yields a high efficiency at both backoff and peak powers. The peak and backoff fundamental currents for the main transistor $|I_{mp}| = 2P_{mp}/|V_{mp}|$ and $|I_{mb}| = |I_{mp}|/K_{im}$ are calculated (Table II) and the corresponding amplitude of the input RF voltage drives $|V_{GS,mp}|$ and $|V_{GS,mb}|$ at peak and backoff respectively are interpolated accordingly. It is noted that the corresponding maximum instantaneous current $I_{D,max}$ is about 2 A for the main transistor at peak power.

In the second step, the auxiliary PA is designed. As indicated in Fig. 6(a), the auxiliary transistor is operated in class-C (harmonics shorted) at the current-source reference planes using a voltage source $|V_a| = |V_{ab}| = |V_{ap}|$ for the fundamental drain voltage. The fundamental drain voltage $|V_a|$ is set to 23.5 V. The drain bias $V_{DD,a}$ is set to 25 V assuming a knee voltage of 1.5 V. The backoff fundamental current is

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TABLE II
DESIGN PARAMETERS FOR THE PROTOTYPE HCD PA

$\|V_m\|$	$\|I_{mp}\|$	$\|I_{mb}\|$	$\|V_{GS,mp}\|$	$\|V_{GS,mb}\|$	R_{mp}	R_{mb}
21.0 V	1.11 A	0.18 A	4.08 V	0.94 V	18.40 Ω	119.30 Ω
$\|V_a\|$	$\|I_{ap}\|$	$\|I_{ab}\|$	$\|V_{GS,ap}\|$	$\|V_{GS,ab}\|$	R_{ap}	R_{ab}
23.5 V	0.88 A	0.02 A	4.00 V	1.16 V	21.01 Ω	1.31 kΩ
m	n	γ_{vp}	γ_{ip}	θ_b	θ_p	PBPR
0.11	0.86	1.26	0.89	33°	147°	10.37 dB

found by $|I_{ab}| = |I_{ap}|/K_{ia}$ (Table II). A 2D parametric sweep is performed with the gate voltage bias $V_{GG,a}$ swept from -4.1 V to -3.3 V and the input RF gate voltage source $|V_{GS,a}|$ swept from 0.2 V to 1.5 V at backoff and 2.8 V to 4.3 V at peak power. The peak and backoff fundamental current for the auxiliary amplifier $|I_{ap}| = 2P_{ap}/|V_{ap}|$ and $|I_{ab}| = |I_{ap}|/K_{ia}$ are calculated (Table II) and the input RF voltage drives $|V_{GS,ap}|$ and $|V_{GS,ab}|$ at peak and backoff respectively are interpolated accordingly.

The resulting combined drain efficiency from the two transistors at the package reference planes calculated by the embedding model is shown in Fig. 7(b) versus the overall peak power (right) $P_{o,p}$ and backoff power (left) $P_{o,b}$ for the different $V_{GG,a}$ and $|V_{GS,a}|$. Since the overall peak power $P_{o,p}$ and backoff power $P_{o,b}$ have already been determined, the DC gate bias of -4.1 V for the auxiliary PA is selected in Fig. 7 (b) to maximize the overall PA efficiency as indicated by the cyan triangular (backoff) and cyan rectangular (peak) markers.

In the third step, the two-port output combiner network design at the current-source reference plane is calculated. Based on (2) and the HCD PA design parameters summarized in Table II, the intrinsic Z-parameters of the two-port combiner network $\boldsymbol{Z_{intr}}$ connected to the current-source device model as shown in Fig. 6(b) are given by:

$$\boldsymbol{Z_{intr}} = \begin{bmatrix} 113.0 + j10.7 & 110.4 - j55.0 \\ 110.4 - j55.0 & 108.0 - j137.7 \end{bmatrix}. \quad (23)$$

B. Simulation Results and Discussions

In this section, the simulated results obtained using the embedding device model from the last section are presented and discussed. For this simulation, the outphasing angle at backoff power θ_b is selected to be 33° and the outphasing angle at peak power θ_p is equal to 147° according to (17) and (18). Fig. 6(b) shows the schematic for the ideal HCD PA prototype using the embedding device model. The harmonic currents for the main and auxiliary intrinsic transistors are terminated by ideal triplexers. The simulated drain efficiency versus output power is shown in Fig. 8(a). A drain efficiency of 75% at about 33.1 dBm output power is achieved in this simulation. The drain efficiency is affected by the outphasing angles between these two input drives. By linearly sweeping the outphasing angle from θ_b to θ_p as the input RF voltage increases from backoff to peak, one can obtain the optimal drain efficiency envelope versus output power which is plotted in Fig. 8(a) indicated by blue hollow circles. The theoretical outphasing angles applied to achieve the optimal drain efficiency are indicated by black hollow rectangles. The intrinsic fundamental drain currents and voltages of the main and auxiliary transistors plotted versus output power are shown in Fig. 8(b). This figure shows

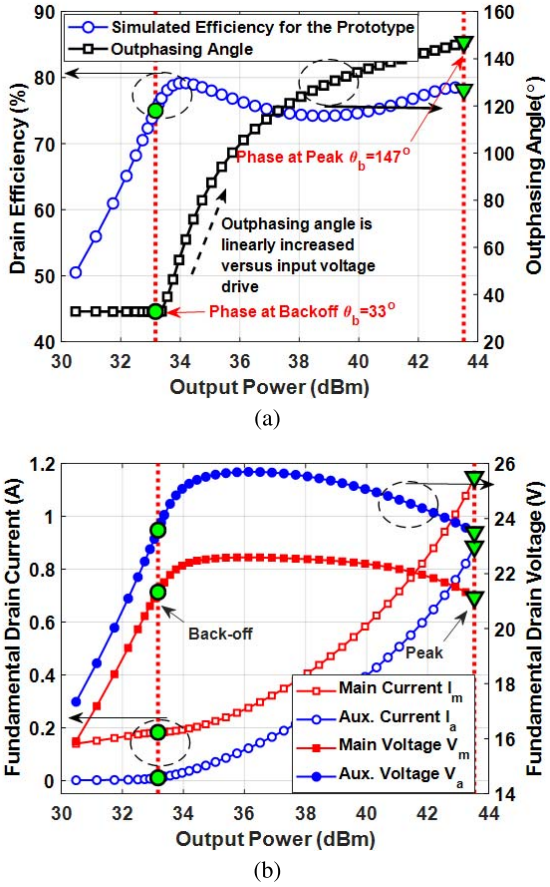

Fig. 8. Simulated (a) optimal drain efficiency and outphasing angle versus output power and (b) amplitudes of the intrinsic fundamental currents and voltages versus output power at 2 GHz.

that the fundamental drain current of the main device (marked by red hollow rectangles) is higher than that of the auxiliary device (marked by blue hollow circles). Below the backoff power level, the auxiliary transistor almost turns off. Fig. 8(b) also shows that the fundamental drain voltages of the two devices (indicated by the solid markers) remain the same at peak and backoff as is expected from the theory. The goal of which is to maintain a high efficiency while fully utilizing the capability of both the main and auxiliary transistors.

The trajectories of the impedances presented to the transistors under load modulation as obtained in the simulation are presented in Fig. 9. It is noted that the fundamental impedances seen by main and auxiliary transistors at the current-source reference plane are purely real at both backoff and peak powers. However, the modulated fundamental load impedances in between are complex, because the outphasing angle that increases between backoff and peak introduces a reactive component to the modulated load impedances. In addition, the fundamental and harmonic loads seen by the main and auxiliary transistors at the package reference planes marked in red are presented in Fig. 9. Due to the linear and nonlinear parasitic contribution at microwave frequencies, the load impedances are shifted and rotated when projected from the current-source to the package reference planes [6] and [26]. The projected loads at the package reference planes

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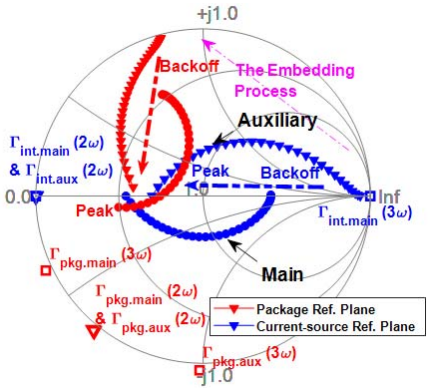

Fig. 9. Simulated load modulation trajectories including the intrinsic impedance $\Gamma_{int.main/aux}(n\omega)$ (blue) presented to the main and auxiliary device and the corresponding impedance at the device package reference plane $\Gamma_{pkg.main/aux}(n\omega)$ (red).

are used to design the physical output combiner and harmonic termination circuits as explained in the next section.

IV. Circuits Design and Implementation of an Hybrid Chireix-Doherty Power Amplifier

A 2 GHz 20-W HCD PA circuit demonstrator is designed and simulated using two device models at the package reference plane. As discussed in the previous section, an ideal HCD PA prototype was first designed and simulated using two embedding device models at the current-source reference planes. The embedding device model predicts the required output load and source reflection coefficients at the package reference planes, which sustains the desired device operation at the current-source reference plane without performing muti-harmonic loadpull simulations or measurements [32] and [35].

The required output combiner at the package reference plane is designed using the Z-parameters of the two-port combiner network $\boldsymbol{Z_{pkg}}$, which is calculated from the optimal fundamental voltages and currents predicted by the embedding device model at peak and backoff at the package reference planes. It is also noted that the physical $\boldsymbol{Z_{pkg}}$ must incorporate not only the fundamental matching circuits but also the harmonic matching circuits.

The embedding device model also predicts the required harmonic impedances at the package reference plane. As shown in Fig. 10(a) the output harmonic termination circuits are implemented using open stubs with electrical length of $\lambda/4$ at $2f_0$ and $3f_0$. Transmission lines are used to transform the harmonic reflection coefficients to meet the targeted harmonic impedance design goals. The contribution at the fundamental frequency of the harmonic termination circuits is then de-embedded from the two-port network combiner circuit $\boldsymbol{Z_{pkg}}$ as shown in Fig. 10(a) to facilitate the design of the two-port output combiner [3], [4], [32] and [25].

Using the above procedure, the de-embedded Z parameters $\boldsymbol{Z'_{pkg}}$ for the fundamental two-port combiner accounting for the harmonic termination circuits are then obtained. In [3], Özen *et al.* proposed a systematic method to synthesize two-port output combiner networks. The methodology is adopted here to synthesize the output combiner for the HCD PA. For a single-frequency PA combiner, it is a

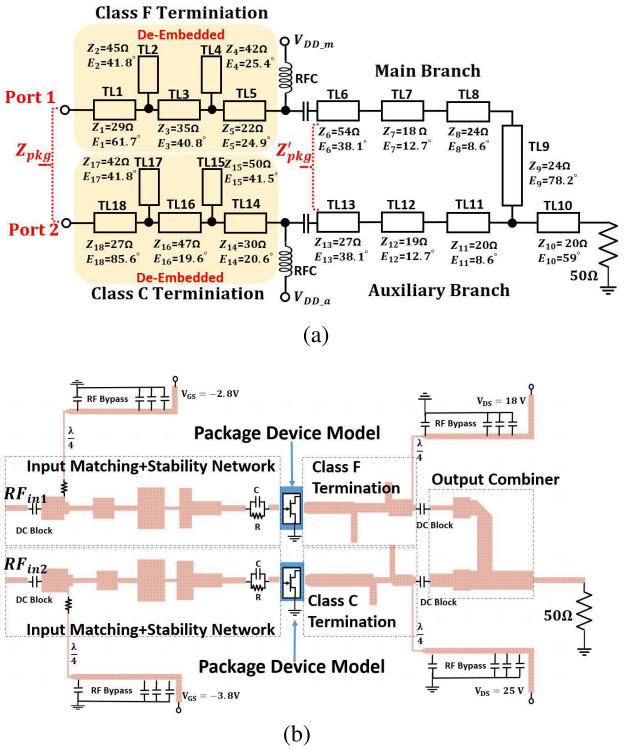

Fig. 10. (a) The synthesized output combiner circuits using transmission lines and (b) complete cut-ready layout of the HCD PA.

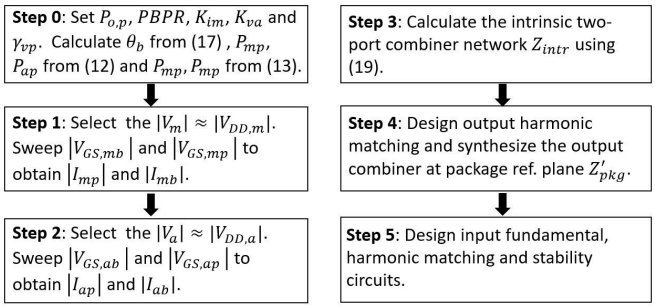

Fig. 11. Design flowchart for the HCD PA.

relatively straightforward design task. The combiner synthesis is performed with the help of computer aided design tools such as the ones provided by the optimization tools in the Keysight Advanced Design System (ADS). The HCD PA output combiner circuit which is synthesized and implemented using microstrip lines at 2 GHz yields the following 2-port impedance $\boldsymbol{Z'_{pkg}}$ including the output load R_L:

$$Z'_{pkg} = \begin{bmatrix} 3.135 + j2.166 & -8.044 + j19.922 \\ -8.044 + j19.922 & 23.263 + j20.042 \end{bmatrix}. \quad (24)$$

Input matching networks are also designed and optimized for the main and auxiliary branches. A stepped-impedance matching topology is applied to perform the conjugate matching at the fundamental frequency and filter out the higher order input harmonics simultaneously. RC networks consisting of a 30Ω resistor and a 3.9 pF capacitor in parallel are used to stabilize the PA. The design procedures for the HCD PA are summarized and presented in Fig. 11. The HCD PA operating at 2GHz is fabricated using a Duroid 5880 substrate with a relative dielectric constant of 2.2 and thickness of 31 mil.

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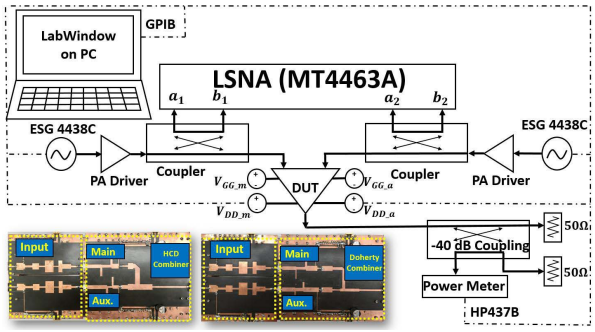


Fig. 12. Schematic of the LSNA testbed used for the CW measurements, the fabricated HCD PA (left), and reference Doherty PA (right).

Two Wolfspeed CGH27015 15-W transistors are used for this implementation. Fig. 10(b) presents complete cut-ready layout of the HCD PA and Fig. 12 shows the fabricated HCD PA.

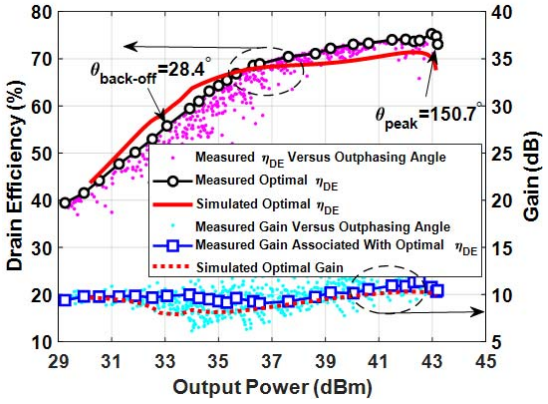
V. Measurement Results

A. Continuous Wave (CW) Measurements

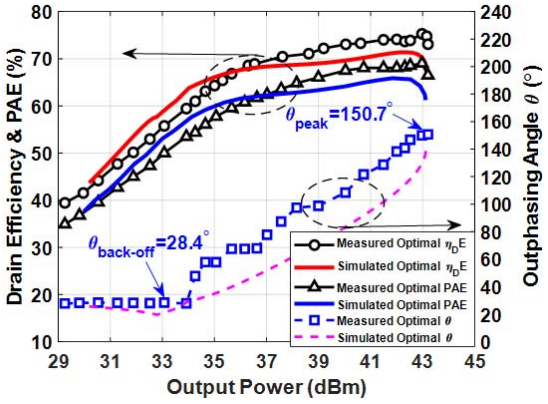
The main amplifier is biased at 18 V for the drain and 58 mA DC quiescent current. The auxiliary amplifier is biased at −3.8 V for the gate and 25 V for the drain. It is noticed that the gate bias of the auxiliary amplifier had to be slightly adjusted from the −4.1 V value used in the simulations in order to compensate for the discrepancy between the package Angelov embedding device model and the actual transistor device.

The CW measurements are performed using a large-signal network analyzer (LSNA) as shown in Fig. 12. The dual-input RF ports are driven by two phase-locked signal-source generators (Keysight ESG 4438C). The incident powers and reflected powers of the main and auxiliary PAs are measured at ports 2 and 1 of the LSNA using two external directional couplers, respectively. The output power is recorded with a power meter (HP437B) and the DC drain currents are captured by the DC drain power supplies. The incident powers and outphasing sweep range used at the input of the HCD PA are obtained at the input ports of the simulated cut-ready PA circuits. Fig. 13(a) compares the ADS simulations with the CW measurements. The simulated results based on the schematic shown in Fig. 10(b) are performed using the EM Co-Simulation built-in the ADS software. As seen from the Fig. 13(a), a close agreement between the simulations and the measurements is observed at 2 GHz. A 61% measured drain efficiency is achieved at 9-dB backoff power with a peak power of about 43 dBm and a measured saturation gain of about 10 dB. It is worth mentioning that the dual-input PA gain (in dB) is defined as the difference between the output power (in dBm) and the sum of the input powers (in dBm) at the two RF input ports. The outphasing behavior is also observed in Fig. 13(a) indicated by the purple and cyan dots.

The outphasing angles at the gate current-source reference plane is theoretically calculated using (17) and (18) to be 33° at backoff and 147° at peak power. After non-linear embedding of the transistor parasitics and linear embedding of the input matching (based on EM Co-simulation) it is found that the outphasing angles have shifted to 23° at backoff and



(a)



(b)

Fig. 13. (a) Drain efficiency and the associated gain. (b) The optimal efficiency and associated outphasing angle for the HCD PA at 2 GHz.

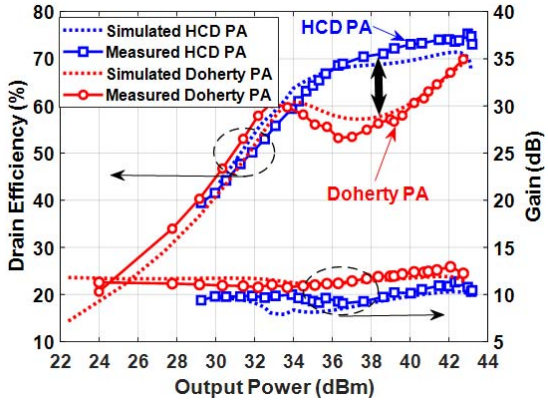


Fig. 14. The 2 GHz large signal simulations and measurements for the HCD and Doherty PA, respectively.

135° at peak power. The optimal outphasing angles based on the measured optimal drain efficiency have slightly deviated from the original values and are found to be around 28° at backoff and 150° at peak as shown in Fig. 13(b). This discrepancy could originate from the difference in (1) the simulated and fabricated output combiner (Fig. 15(b)) and (2) the input impedance between the Angelov package device model and the actual transistors used in this design, especially for the auxiliary transistor biased in class-C. It is also noted that in Fig. 13(b) the EM-simulated outphasing angle (purple dashed line) used between backoff and peak is the one predicted by embedding assuming the intrinsic gate voltage

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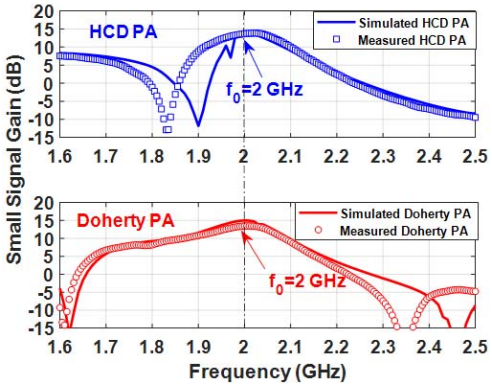
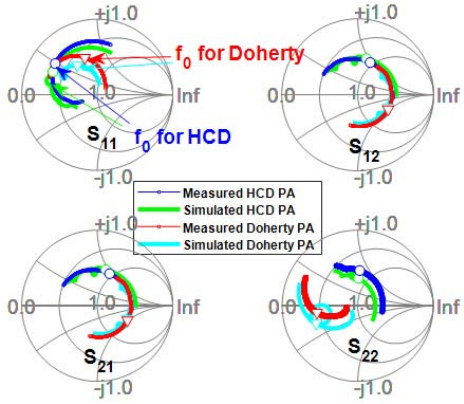
TABLE III
MODULATED SIGNAL MEASUREMENT AT 2 GHZ

	Signal	Output PAPR (dB)	$P_{inc,avg.}$ (dBm)	$P_{out,avg.}$ (dBm)	$P_{out,peak}$ (dBm)	$\eta_{DE,avg.}/PAE_{avg.}$ (%)	$ACLR_{L,H}$ (dBc)	NMSE (dB)
Before DPD	10 MHz LTE	8.4	22.7, 21.7	34.4	42.8	63.0/55.4	−30.7, −30.0	−15.2
After DPD	10 MHz LTE	9.6	21.2, 20.3	33.3	42.9	60.3/53.4	−53.2, −51.2	−35.4
Before DPD	20 MHz LTE	8.5	22.7, 21.7	34.4	42.9	62.3/54.9	−31.7, −30.5	−15.8
After DPD	20 MHz LTE	9.4	21.5, 20.5	33.4	42.8	60.0/52.9	−48.1, −47.7	−32.5



(a)



(b)

Fig. 15. Small-signal evaluations for the HCD and Doherty PAs. (a) Small-signal gains for the HCD and Doherty PAs. (b) S-parameters of the HCD and Doherty combiners.

drive is varying linearly with output power. The dashed blue line with square in Fig. 13(b) corresponds to the optimal value obtained from the LSNA measurements. Below the backoff power, the choice of the outphasing angle does not affect the performance since the auxiliary transistor is turned off.

B. Comparison Between the Hybrid Chireix-Doherty and Doherty PAs

In order to verify that HCD PA exhibits higher drain efficiencies in the higher power regime compared to the Doherty PA, a 2 GHz dual-input asymmetric Doherty PA as shown in Fig. 12 with a 9-dB PBPR was also designed as a reference PA for the sake of comparison with the HCD PA. For a fair comparison, the same transistors were used in both PAs to eliminate any variation in devices. Furthermore, to minimize any variation in the drain efficiency due to different input second harmonic design, the same input matching networks are used for both PAs. For demonstration purpose, the simulations and measurements in Fig. 14 are obtained by

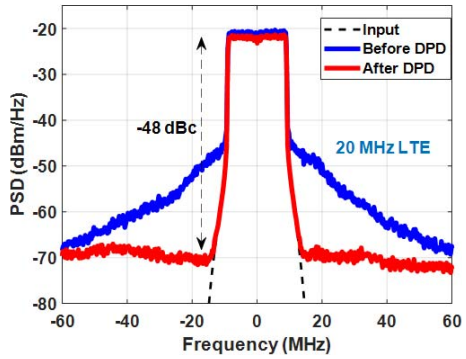


Fig. 16. Spectral density before (blue) and after DPD (red) 20 MHz LTE signals centered at 2 GHz.

using the same input matching networks and only swapping the two different output combiners. It is noted that in the lower power regime, both PAs exhibit similar drain efficiencies since both of the main devices operate in class-F with the auxiliary device turned off. However, in the higher power regime, the HCD PA achieves a higher and flatter drain efficiency response than that of the Doherty PA as shown in Fig. 14. To evaluate the designs of the two PAs, the simulated and measured small-signal gains versus frequency are compared in Fig. 15(a). The simulated and measured S-parameters of the HCD and Doherty combiners after TRL calibration are also presented versus frequency in Fig. 15(b), respectively.

C. Digital Pre-Distortion (DPD) With LTE Signals

The dynamic response of the HCD PA is verified with both 10 MHz and 20 MHz input LTE signals exhibiting 9.6 dB and 9.5 dB PAPR, respectively. The same linearization technique as reported in [18] is used. First a look-up table is created based on the CW simulation-guided measurement results which determined the PA output power as a function of the outphasing angle and input power. Next an inverse PA model is extracted using the generalized memory cubic-spline basis [37], [18] and applied to generate the pre-distorted waveforms. The same waveforms were used for both the inverse model extraction and linearization for demonstration purpose. With 10 MHz LTE signal, 60.3% of average drain efficiency and around -53.2 dBc adjacent channel leakage ratio (ACLR) are achieved at an average output power of 33.3 dBm after applying DPD. With 20 MHz LTE signal, 60.0% of average drain efficiency and around -48.1 dBc adjacent channel leakage ratio (ACLR) are achieved at an average output power of 33.3 dBm after applying DPD. The spectral density before (blue) and after DPD (red) 20 MHz LTE signals are shown in Fig. 16. The modulated signal measurements are summarized in Table III. It is noted that after DPD, the PAPR of the output signals from the HCD PA increases and becomes

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TABLE IV
COMPARISON OF THE RECENT STATE-OF-THE-ART PAS

Device Technology	Architecture	Signal	f_0 (GHz)	Drain Bias (Main/Aux.) (V)	BW (MHz)	PAPR (dB)	$P_{out,avg.}$ (dBm)	$\eta_{DE,avg.}/PAE_{avg.}$ (%)	ACLR (dBc)	Ref
GaN	Doherty	LTE	1.95	28/28	20	9	35.16	55/50	-49	[3]
GaN	Doherty-Outphasing	W-CDMA	2.3	30/30	3.84	6.7	35.3	−/40	-57,-59	[28]
GaN	Asymmetric Doherty	LTE	2.0	14.3/28	10	8.85	33.55	51.9/−	-51.5	[6]
LDMOS	Chireix-Doherty	-	2.17	28/21	3.84	7.5	43.9	45.8/45.4	-50.2,-50.2	[30]
GaN	4-way outphasing	W-CDMA	2.14	20/20	3.84	9.15	41.49	55.6/−	−33*	[20]
GaN	Hybrid Chireix-Doherty	LTE	2.0	18/25	20	9.5	33.3	60.0/52.9	-48.1,-47.7	**This work**

* No DPD was performed.

the same as the PAPR of the input LTE signals. In Table IV, the performance of the HCD PA in this paper is compared with other works found in recent literatures.

VI. CONCLUSION

An analytic generalized Doherty-Chireix continuum theory was proposed and discussed. The analysis was performed at the current-source reference planes. Class-B, $\mathrm{F}/\mathrm{F}^{-1}$ or C operation for the auxiliary and main transistors was assumed at peak and backoff, such that the impedances seen by the transistor current sources at peak and backoff are both real. We further limited the analysis to OPAs with the same fundamental drain voltages at peak and backoff ($K_{vm} = 1$) for the main transistor. A 3D Doherty-Chireix continuum of modes was then defined for dual-input OPAs in terms of the auxiliary PBVR K_{va} and PBCR K_{ia} and the main PBCR K_{im}. When limiting the analysis to dual-input OPAs with the same PBPR, the continuum of modes then reduces to 2D with the auxiliary PBVR K_{va} and PBCR K_{ia} the independent variables. This 2D continuum covers all of the possible modes of dual-input OPAs operation including Doherty and Chireix PAs. A new type of OPA operation, the HCD mode, which optimally combines features of both the Doherty and Chireix modes was singled out within this continuum. In the low power regime, the auxiliary PA turns off similarly to the conventional Doherty operation. Between backoff and peak powers, the HCD PA maintains a nearly constant drain voltage for both of the main and auxiliary transistors, as in the mixed-mode Chireix outphasing PA. This Hybrid mode of operation requires dynamically adjusting the outphasing angle at the dual-input with the incident power. The efficiency drop between back and peak powers typically observed in the conventional Doherty PAs is reduced or cancelled (HD-max mode). Hence the average efficiency of the Hybrid Chireix-Doherty PA under modulated-signal measurement is enhanced compared to the Doherty PA. To further validate the continuum theory, a Hybrid Chireix-Doherty PA operating at 2 GHz was implemented with a packaged transistor device and transmission lines, and the expected distinctive performance was experimentally achieved for both CW and modulated signals.

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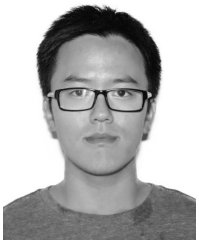

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