New Mixed-Mode Design Methodology for High-Efficiency Outphasing Chireix Amplifiers

Hsiu-Chen Chang, *Student Member, IEEE*, Yunsik Hahn, *Student Member, IEEE*, Patrick Roblin, *Senior Member, IEEE*, and Taylor Wallis Barton, *Member, IEEE*

***Abstract*— A new design methodology providing optimal mixed-mode operation for dual-input class-F outphasing Chireix amplifiers is presented. The design starts with single-transistor class-F simulations at the intrinsic *I–V* reference planes to directly select the optimal peak and backoff resistive loads $R_{\min}$ and $R_{\max}$ and input RF gate drives yielding the best combination of efficiencies and output powers without needing to perform a load pull simulation or measurement. New analytic equations expressed only in terms of $R_{\min}$ and $R_{\max}$ are given for designing the Chireix combiner at the current source reference planes. Nonlinear embedding is then used to predict the incident power and multi-harmonic source and load impedances required at the package reference planes to physically implement the power amplifier (PA). An analytic formula solely expressed in terms of $R_{\min}$ and $R_{\max}$ is reported for the peak and backoff outphasing angles required at the PA input reference planes. A Chireix outphasing PA is designed using two 15-W GaN HEMTs. A Chireix outphasing PA exhibits a peak efficiency of 72.58% with peak power of 43.97 dBm and a 8-dB backoff efficiency of 75.22% at 1.9 GHz. Measurements with 10-MHz LTE signals with 9.6-dB PAPR yield 59.4% average drain efficiency at 1.9 GHz while satisfying the 3GPP linearity requirements.**

***Index Terms*— Chireix, combiner, embedding, GaN, high efficiency, outphasing.**

I. Introduction

THE rapidly rising demand for high data-rate in wireless communication has resulted in the use of communication protocal with signals exhibiting high peak-to-average power-ratio (PAPR). For such communication signals with high PAPR, the reduction of the energy consumption and operating cost calls for the use of power amplifier (PA) architectures such as the Doherty PA architecture [1]–[6] which provides a high average power efficiency. Beside the mainstream Doherty amplifier architecture, the Chireix outphasing amplifier architecture provides an alternative approach which is being investigated for designing high efficiency PAs [7]–[32].

The Chireix outphasing architecture has been successfully realized in a variety of device process technologies such as GaN [14]–[26], LDMOS [27], CMOS [28], [29], and CMOS-GaN [30]–[32]. The conventional Chireix outphasing architecture consists of two amplifiers and one lossless combiner, typically implemented using a single quarter-wave transmission line and a stub (or lumped passive capacitor and inductor) in each path. Conventional analysis of the Chireix PA assumes constant-amplitude drive of the two branch PAs, with output power controlled through the outphasing angle. In this conventional mode of operation, the transistors are operated in deep saturation. In mixed-mode operation, both the phase and amplitude of the branch PA drives are modulated [14], [15], [18]. It has been verified that this can provide a higher efficiency at backoff power compared to the conventional mode. Indeed in the mixed mode, while the relative phase controls the load impedance, the power drive is typically adjusted to maintain saturation without over-driving the PAs. Below a pre-determined outphasing operating regime, the phase (and therefore load impedance) is held fixed and amplitude modulation is used to extend the dynamic range down to zero output power. Therefore, mixed-mode operation is critical for optimizing the performance over a wide dynamic range.

In either operating mode, both branch PAs in the Chireix architecture are kept in saturation over the entire outphasing range. This is in contrast to Doherty PAs, where at most one PA is in an efficient saturated mode. In addition, Chireix outphasing offers the advantage of symmetric operation of the two branches, allowing identical PAs to be used. Nonetheless, Doherty PAs have seen significantly greater commercial success, attributable to its single RF input and to the existence of clear analysis methodologies. In this work, we address the design methodology of mixed-mode Chireix outphasing to provide a direct synthesis approach. The new analytic design equations reported in this paper for the Chireix combiner prototype are developed to obtain optimal drain efficiency at both peak and backoff powers under mixed-mode outphasing operation.

The design procedures for the Chireix outphasing combiner typically follow two different stages. The conventional

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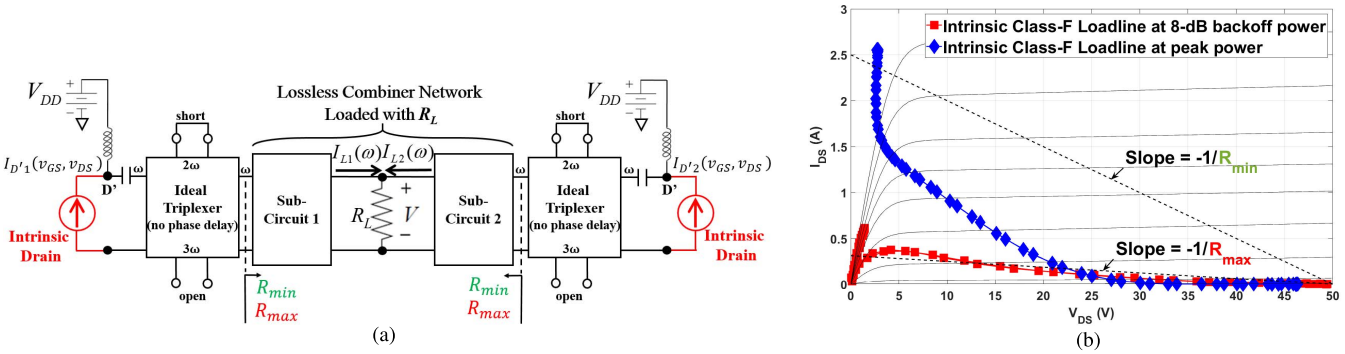


Fig. 1. (a) Prototype combining-network of a two-way current-source based Chireix outphasing amplifier to be used with the embedding device model for the fundamental frequency component. The ideal triplexer is used for obtaining class-F multi-harmonic loads with zero phase delay (b) Intrinsic Class-F PA loadlines at 8 dB backoff power and peak power.

combiner theory is first introduced by using ideal voltage sources for the transistors at the package drain reference planes, and thus neglects the linear and nonlinear device parasitics between the intrinsic current source reference planes (CSRPs) and the package reference planes (PRPs) of both transistors [8], [15], [17], [24]–[26]. Load-pull and source-pull measurements or simulations with the de-embedding device models are then used to search for the optimal multi-harmonic load and source impedances at the package drain reference planes in order to account for the linear and nonlinear device parasitics [9], [10], [16], [18], [30].

Unlike the outphasing combiner theory directly developed at the device PRPs, new mixed-mode analytic design equations for the Chireix outphasing combiner at the CSRPs of the FET device model will be introduced in this paper. To practically realize this optimal operation at the CSRPs, a model-based embedding FET device model is then required to project the voltage and current waveforms to the PRPs [33], [34]. With the embedding FET device model, the desired intrinsic drain fundamental and multi-harmonic loads can be realized simultaneously without using time-consuming multi-harmonic load-pull and source-pull searches at the PRPs using simulations or measurement techniques. It is sufficient to directly connect the new outphasing combiner and an ideal triplexer for harmonic terminations to the CSRPs for the embedding model to automatically define the multiharmonic and fundamental combiner networks required at the PRPs. The embedding device model designing technique has been successfully applied to multiple different PA architectures and classes such as Doherty PA [3], outphasing PA [22], single broadband continuous class B/J PA [35], and single continuous class-F PA [36].

It is to be noted that the proposed mixed-mode outphasing combiner design equations presented in this paper are fundamentally different from the constant-envelope outphasing theory reported previously [21], [22], [37] for several reasons. First, in contrast to the constant-envelope outphasing analysis, the new mixed-mode outphasing analysis permits a more flexible selection of the best efficiency at both peak and backoff power. Furthermore, the method previously reported in [21] and [22] was based on an approximate calculation using an estimate of the knee voltage (V_{on}) and the maximum drain voltage $V_{D,max}$ for dual-transistor simulations, which did not permit the designer to accurately set the peak-to-backoff power ratio (PBPR). On the contrary, single-transistor simulations are used in this paper to search for the required resistive fundamental intrinsic drain loads at peak power and backoff power, and the input fundamental RF gate drives at peak and backoff power. The desired PBPR can then be precisely controlled based on these variables. In addition to this new single-transistor design technique, which significantly simplifies the design flow and accelerates the design, (1) the new analytic outphasing combiner as well as (2) the analytic outphasing angles required are now solely decided by the resistive intrinsic fundamental loads at peak and backoff power.

This paper is organized as follow. First, the analytic theory for the design of mixed-mode Chireix outphasing PAs using the embedding device model is introduced in Section II. The low-pass filter based harmonic termination and combiner synthesis are introduced in Section III. Large-signal CW measurement results and digital linearization results using modulated signals are reported in Sections IV and V, respectively. A summary of the new contributions is presented in the conclusion in Section VI.

II. Analytic Outphasing Theory for Mixed-Mode Operation

Fig. 1(a) shows the circuit topology of the prototype outphasing combining network to be used with the embedding FET device model. As shown in Fig. 1(a), the left and right current sources represent the intrinsic drain current $I_{D'}(v_{GS}, v_{DS})$ (IV characteristics) at the CSRPs of each transistor. The new outphasing combiner is implemented with two lossless two-port sub-circuits connected to a common load R_L. Two ideal triplexers (multi-harmonic terminations with zero phase delay) are implemented in order to define the PA's class of operation and establish device dynamic loadlines providing high efficiency. In this work, a class-F implementation will be pursued as it can provide a higher efficiency compared to class B/J and class E at high frequencies [30]. Fig. 1(b) shows the class-F intrinsic loadlines with resistive fundamental intrinsic drain loads R_{min} and R_{max} at peak (P) and backoff (B) power, respectively. Based on the mixed-mode outphasing operation, the two transistors operate with the same R_{min} and R_{max}, and the same input fundamental RF gate

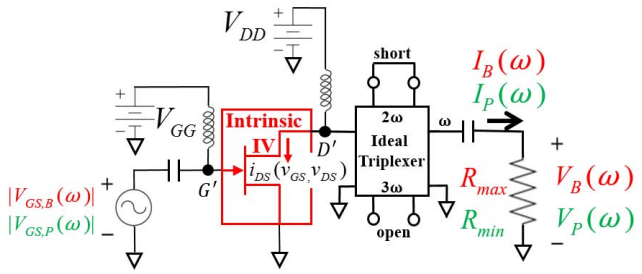


Fig. 2. Single-transistor circuit used at the current-source reference planes (CSRPs) with the embedding model for determining the operation at (a) backoff power $(P_{o,back})$ using the load R_{max} and (b) peak power $(P_{o,peak})$ using the load R_{min}, respectively. This schematic is also used to define the intrinsic fundamental voltages and currents at peak and backoff to be used in the analytic Chireix design theory.

drives $|V_{GS,P/B}(\omega)|$ at peak and backoff power, respectively. This important feature allows the designer to rely on single-transistor simulations to search for the best combination of R_{min}, R_{max} and $|V_{GS,P/B}(\omega)|$, providing the optimal output power P_o, efficiency, and peak-to-backoff power ratio (PBPR).

A. Single Transistor Optimization at the Current Source Reference Planes

Using the intrinsic I-V characteristics, the optimal incident powers and load impedances which will yield the best Chireix PA performance can be determined from single transistor simulations before starting the design of the two-transistor outphasing combiner circuit. A single-transistor simulation is sufficient in the first design stage because both transistors have the same loadline at peak and backoff powers.

Class-F operation is selected for the operation of the transistors at both peak and backoff. While using the embedding device-model, ideal open and short harmonic terminations can then be used at the CSRPs for the even and odd harmonics, respectively, as shown in Fig. 2. The design of a class-F PA with optimal performance at peak (P) and backoff (B) therefore simply requires the selection of the R_{min} and R_{max} and the corresponding amplitude of fundamental gate voltages $V_{GS,P}(\omega)$ and $V_{GS,B}(\omega)$.

To select the appropriate input RF gate drives $|V_{GS,P/B}(\omega)|$, and resistive fundamental intrinsic drain loads R_{min} and R_{max} at the CSRPs, the following four performance parameters are monitored: 1) the peak output power $P_{o,peak}$, 2) the backoff output power $P_{o,back}$, 3) the drain efficiency $\eta_{DE,peak}$ at peak and 4) the drain efficiency $\eta_{DE,back}$ at backoff. Note that the backoff power $P_{o,back}$ is targeted such that the peak to backoff power ratio (PBPR) given by $P_{o,peak}\big|_{\text{dBm}} - P_{o,back}\big|_{\text{dBm}}$ approaches the signal peak to average power ratio (PAPR). Furthermore, unlike in the empirical approach in [30], the peak and backoff levels can be assumed resistive because they are found at the CSRPs.

Unlike the conventional constant-envelope operation for the outphasing PA, the mixed-mode operation was selected here in order to obtain a high efficiency in the medium-to-high power backoff region while obtaining the targeted output power. Fig. 3(a) and Fig. 3(b) show the simulation results obtained with a single transistor under peak and backoff power operations, respectively, as a function of resistive fundamental intrinsic drain loads R_{min} or R_{max} and the fundamental component of the RF gate voltages $V_{GS,P}(\omega)$ or $V_{GS,B}(\omega)$.

By sweeping $|V_{GS}(\omega)|$, R_{min}, and R_{max} at the CSRPs, the optimal $P_{o,peak}$ and $P_{o,back}$ at the PRPs can be then selected to achieve the desired power backoff (PBPR) while obtaining optimal efficiencies. Fig. 3(a) and Fig. 3(b) shows the backoff power and peak power design spaces, respectively. Each point in Fig. 3 indicates one possible combination of gate drive amplitude $|V_{GS}(\omega)|$ and R_{min} or R_{max}. As shown in Fig. 3, $R_{min} = 20\ \Omega$ and $R_{max} = 160\ \Omega$ are selected based on a 34.2 dBm backoff power and a 42.1 dBm peak power while maintaining nearly 80% drain efficiency and 8 dB backoff (PBPR) at the PRPs. The yellow triangles in Fig. 3 indicate the best combination of $|V_{GS}(\omega)|$ with R_{min} or R_{max} selected under these conservative performance considerations. Applying the best load and gate voltage combination selected in Fig. 3 into the single-transistor circuit schematic of Fig. 2, the precise PBPR obtained at the CSRPs can be calculated from these simulations using:

$$\text{PBPR} = \frac{P_{o,peak}}{P_{o,back}} = \frac{\frac{1}{2}\mathcal{R}\{I_P(\omega)V_P^*(\omega)\}}{\frac{1}{2}\mathcal{R}\{I_B(\omega)V_B^*(\omega)\}}. \tag{1}$$

B. Outphasing Combiner for Mixed-Mode Operation at the Current Source Reference Planes

After selecting the best mixed-mode class-F performance that one could possibly achieve from the single-transistor simulations, a prototype outphasing combiner network needs to be developed at the CSRPs. The desired Chireix operation at both the CSRPs and the PRPs can thus be realized with embedding device model.

The prototype Chireix outphasing network used with the embedding device model at the CSRPs is shown in Fig. 4. The four intrinsic reference planes introduced in Fig. 4 are successively: 1) Plane G' the intrinsic gate reference plane for the memoryless IV characteristics, 2) Plane D' the intrinsic drain current-source reference plane, 3) Plane C' the plane at the combiner's port 1 and port 2, and 4) Plane L' the common load R_L reference plane. Note that at this prototype stage where the Chireix PA design is first verified using the embedding model, planes D' and C' are the same for the fundamental frequency, as the ideal multiplexer used for class-F harmonic termination acts as an ideal through at the fundamental frequency. Once the harmonic termination circuit is implemented at the PRPs with real circuits, the frequency-dependent phase shift between the extrinsic plane D and plane C will need to be accounted for.

The outphasing analysis begins at the common load R_L (plane L') with the targeted mixed-mode Chireix operation:

$$\begin{aligned} I_{L1}(|V_{GS}(\omega)|, \theta_L) &= |I_{L1}(|V_{GS}(\omega)|)| \exp(+j\theta_L/2), \\ I_{L2}(|V_{GS}(\omega)|, \theta_L) &= |I_{L2}(|V_{GS}(\omega)|)| \exp(-j\theta_L/2), \\ I_L(|V_{GS}(\omega)|, \theta_L) &= I_{L1} + I_{L2}, \end{aligned} \tag{2}$$

where θ_L is the outphasing angle at the common load R_L. I_{L1} and I_{L2} are now both function of $|V_{GS}(\omega)|$ because of the

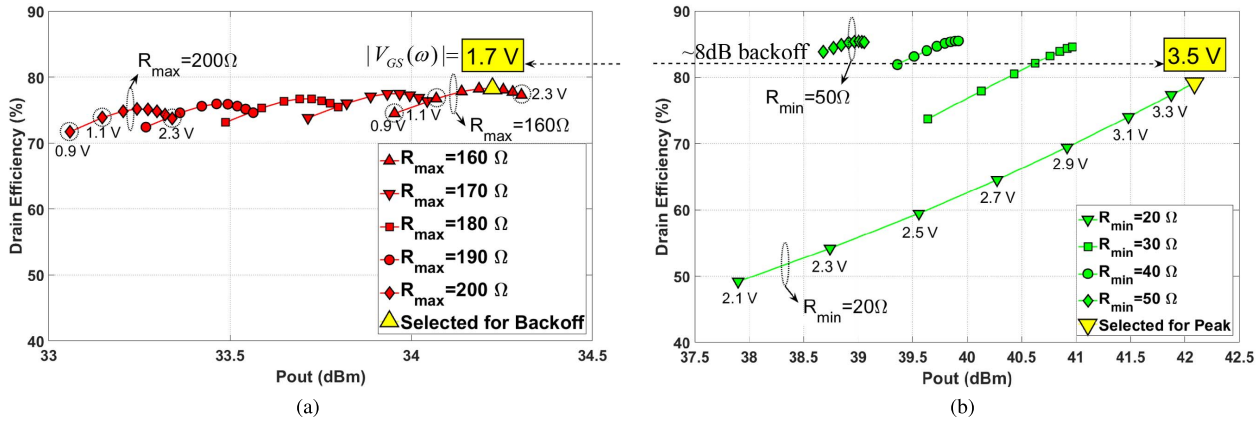


Fig. 3. Efficiency versus output power simulated at the package reference planes (PRPs) with excitations at the current-source reference planes (CSRPs) using the embedding model and the single-transistor circuits as shown in Fig. 2, operating respectively at (a) backoff power $(P_{o,back})$ and (b) peak power $(P_{o,peak})$.

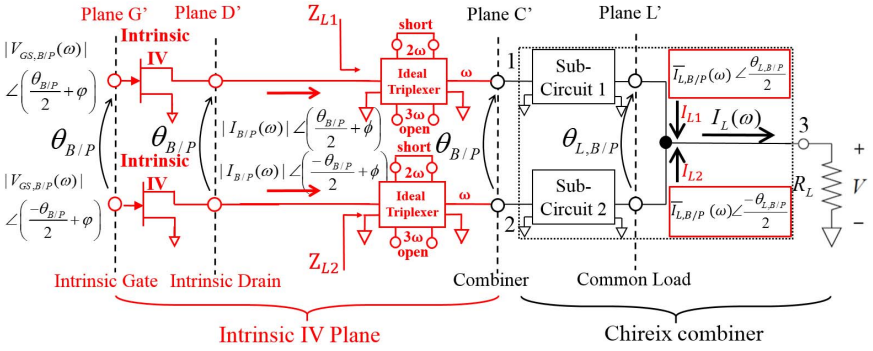


Fig. 4. Prototype circuit of the mixed-mode Chireix outphasing PA realized with the embedding model at the CSRPs. Plane G': Intrinsic gate reference planes. Plane D': Intrinsic drain current-source reference planes. Plane C': Combiner reference planes. Plane L': Common load reference planes.

mixed-mode operation. Note that both $|V_{GS}(\omega)|$ and θ_L are a function of the targeted output power P_o.

At peak power ($\theta_{L,P} = 0°$) both transistors operate identically ($|I_{L1,P}| = |I_{L2,P}| = \overline{I_{L,P}}$) and we have:

$$I_L\left(|V_{GS,P}(\omega)|, \theta_{L,P}\right) = 2\overline{I_{L,P}}. \tag{3}$$

At backoff power ($\theta_{L,B} = \theta_L$) both transistors operate identically ($|I_{L1,B}| = |I_{L2,B}| = \overline{I_{L,B}}$) and we have:

$$I_L\left(|V_{GS,B}(\omega)|, \theta_{L,B}\right) = 2\overline{I_{L,B}}\cos(\theta_{L,B}). \tag{4}$$

The peak to backoff power ratio (PBPR) with mixed-mode operation at the common load R_L is then:

$$\text{PBPR} = \frac{\left|I_L\left(|V_{GS,P}(\omega)|, \theta_{L,P}\right)\right|^2}{\left|I_L\left(|V_{GS,B}(\omega)|, \theta_{L,B}\right)\right|^2} = \frac{\overline{I_{L,P}}^2}{\overline{I_{L,B}}^2\cos^2(\theta_{L,B})}. \tag{5}$$

Note that for the constant-envelope case, (5) reduces to the classical equation PBPR $= \cos^{-2}(\theta_{L,B})$ (see [7], [21], [22]).

Given the targeted mixed-mode outphasing behavior at the common load (plane L'), the ideal lossless and reciprocal outphasing combiner network connected to the plane D' in Fig. 4 needs now to be designed so that the combiner presents the impedance R_{max} at backoff and R_{min} at peak as determined in the single transistor simulations. Two two-port impedance matrices are used as shown in Fig. 5 to represent the sub-circuit 1 and 2 of the outphasing combiner in Fig. 4, to facilitate the synthesis of the required combiner. The procedure used to calculate the drain voltage V_1 and drain current I_1 at plane D' starting from the load voltage $I_L R_L$ and currents I_{L1} at the plane L' (see Fig. 4 and Fig. 5) is presented in Appendix A.

It can be found using the results in Appendix A that the pure-imaginary Z-parameters ($Z_{ij} = jX_{ij}$) of the lossless and reciprocal outphasing combiner can be solely expressed in terms of the load R_L of the intrinsic prototype PA and the targeted intrinsic peak R_{min} and backoff R_{max} loads as:

$$X_{11}^{\text{sub}} = -\sqrt{\frac{R_{min}^3}{R_{max}}}, \tag{6}$$

$$X_{12}^{\text{sub}} = \sqrt{2R_L R_{min}\left[\frac{R_{min}}{R_{max}} + 1\right]}, \tag{7}$$

$$X_{22}^{\text{sub}} = -2R_L\sqrt{\frac{R_{min}}{R_{max}}}. \tag{8}$$

Note that the load R_L used in the intrinsic prototype is arbitrary and does not affect the transistors' operation. 50 Ω is selected for R_L in this paper.

Using the Z-parameters $Z_{ij}^{\text{sub}} = jX_{ij}^{\text{sub}}$ for the two sub-circuits 1 and 2 shown in Fig. 5, the two selected resistive loads R_{min} and R_{max} for the peak and backoff power, respectively,

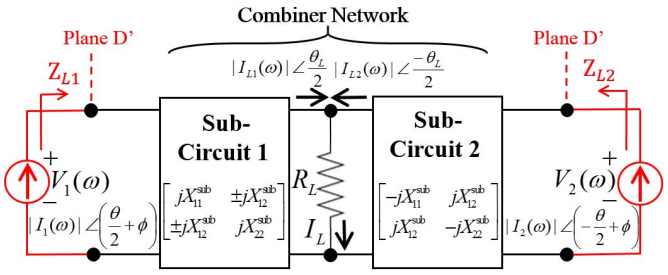


Fig. 5. Circuit implementation of the Chireix outphasing combiner. $|I_1(\omega)|$ and $|I_2(\omega)|$ are the amplitudes of the fundamental *drain* currents contributed by sub-circuits 1 and 2. $i_{D1}(t)$ and $i_{D2}(t)$, respectively. $|I_{L1}(\omega)|$ and $|I_{L2}(\omega)|$ are the amplitudes of the fundamental *load* currents contributed by sub-circuits 1 and 2.

are now provided by the combiner at the plane D'. The required backoff outphasing angle $\theta_{L,B}$ at the common load (plane L') is derived in Appendix A in terms of R_{min} and R_{max} as:

$$\theta_{L,B} = \pm 2\tan^{-1}\left(\sqrt{\frac{R_{max}}{R_{min}}} - \sqrt{\frac{R_{min}}{R_{max}}}\right). \tag{9}$$

Two different solutions are found for the *backoff* outphasing angle $\theta_{L,B}$ at the common load (plane L' in Fig. 4 and 5). The *peak* outphasing angle at the common load is $\theta_{L,P} = 0$. In the next section we shall derive an analytic expression for the peak and backoff outphasing angles θ_P and θ_B required at the gate (Plane G') and drain current-source (Plane D') of the Chireix prototype to sustain this desired mixed-mode Chireix operation at the load R_L.

C. Peak and Backoff Outphasing Angles at PA Input

We need next to find the complex fundamental RF gate voltages $V_{GS,1}(\omega)$ and $V_{GS,2}(\omega)$ to be applied to the Plane G' for simulating the mixed-mode operation of the Chireix amplifier in Fig. 4 with the embedding model. The amplitude of these voltages $|V_{GS,i}(\omega)|$ has already been determined in the single transistor design in the previous section. Only the outphasing angle θ between the two branches needs to be calculated at the plane D' as shown in Fig. 4. Note that at peak and backoff, the same outphasing angle θ is to be applied to the plane G' to sustain the outphasing angle θ at the planes D'. Although the equations in Appendix A provide the means to calculate θ numerically, a compact analytic solution for the outphasing angle θ at plane D' in terms of R_{min} and R_{max} is highly desirable. We outline below the complete derivation found in Appendix B.

The linear lossless three-port outphasing combiner circuit loaded with the common load R_L can be represented by a lossy two-port network $\boldsymbol{Z}$ [16], [37]. At peak and backoff we have:

$$\boldsymbol{V_{D'}} = \boldsymbol{Z}\boldsymbol{I_{D'}} = \boldsymbol{I_{D'}}\begin{bmatrix} R_{max} & 0 \\ 0 & R_{min}\end{bmatrix}, \text{ with} \tag{10}$$

$$\boldsymbol{I_{D'}} = \begin{bmatrix} I_{1,B} & I_{1,P} \\ I_{2,B} & I_{2,P}\end{bmatrix} \text{ and } \boldsymbol{V_{D'}} = \begin{bmatrix} V_{1,B} & V_{1,P} \\ V_{2,B} & V_{2,P}\end{bmatrix}.$$

Note that this forms an eigenvalue problem with eigenvalues R_{min} and R_{max} and eigenvectors:

$$\boldsymbol{I_{D',B/P}} = \begin{bmatrix} |I_{1,B/P}|\exp\left(+j\theta_{B/P}/2\right) \\ |I_{2,B/P}|\exp\left(-j\theta_{B/P}/2\right)\end{bmatrix}, \tag{11}$$

where $\theta_{B/P}$ are the backoff and peak outphasing angles at plane D' as well as plane G'. At peak and backoff, both transistors operate similarly such that we have for $\theta = \theta_P$, the same peak current amplitude $|I_{1,P}| = |I_{2,P}| = |I_P|$, and for $\theta = \theta_B$, the same backoff current amplitude $|I_{1,B}| = |I_{2,B}| = |I_B|$.

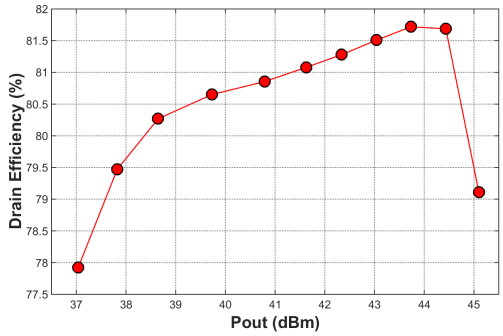
Applying the three-port combiner lossless ($\mathcal{R}^2[Z_{12}] = \mathcal{R}[Z_{11}]\mathcal{R}[Z_{22}]$) and reciprocity ($Z_{12} = Z_{21}$) conditions on the 2-port impedance matrix $\boldsymbol{Z}$ of the combiner loaded with R_L ([16], see [37] for a detailed derivation), simple analytic equations expressed in terms of R_{min} and R_{max} are derived in Appendix B for the combiner impedance $\boldsymbol{Z}$ and outphasing angles θ_B at backoff and θ_P at peak both measured at the gate and drain current-source reference plane D' and G':

$$\theta_B = \pm\cos^{-1}\left(\pm\frac{R_{max} - R_{min}}{R_{max} + R_{min}}\right), \tag{12}$$

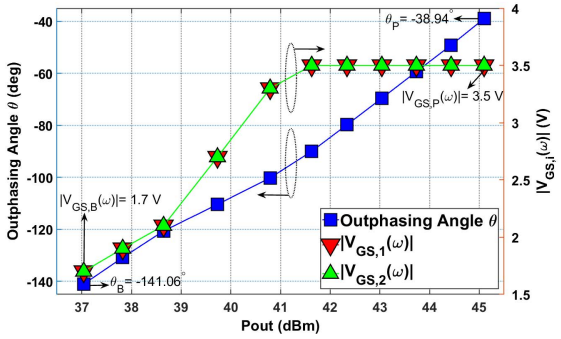
$$\theta_P = \pi - \theta_B. \tag{13}$$

Using $R_{min} = 20\ \Omega$ and $R_{max} = 160\ \Omega$, the analytic solution of (12) yields four possible outphasing angles: $\pm 38.94°$ and $\pm 141.06°$ for backoff power at plane D' as well as plane G'. The solution $-141.06°$ is associated with the positive sign ($+X_{12}^{sub}$) in sub-circuit 1 for the combiner. The solution $-38.94°$ is associated with the negative sign ($-X_{12}^{sub}$) in sub-circuit 1 for the combiner. The other two solutions $141.06°$ and $38.94°$ are simply obtained by exchanging the sub-circuits 1 and 2 of the combiner. Thus, the outphasing angle between peak and backoff power is varying within the range $-141.06° \le \theta \le -38.94°$ or the range $38.94° \le \theta \le 141.06°$ depending on which combiner topology is selected. Fig. 5 summarizes the resulting two choices for the left (top) and right (bottom) 2-port impedance matrices used in the prototype combiner.

It is worth emphasizing that the method previously reported in [21] to select the R_{min} and R_{max} was based on an approximate calculation using an estimate of the knee voltage (V_{on}) and the maximum drain voltage ($V_{D,max}$). Thus the R_{min} and R_{max} values were not well-controlled, and not accurately achieved in circuit simulations. Due to the assumption of constant-envelope operation, the calculation of the outphasing angle was not consistent with the mixed-mode Chireix outphasing operating targeted and the peak and backoff efficiences were not optimized. As a results the PBPR, output power, and efficiencies obtained in harmonic balance simulations all departed from their theoretrical values. On the contrary, we will verify in the next section using harmonic balance simulations on the two-transistor Chireix PA, that the new design procedure relying on the design equations reported for the first time in this paper for both the outphasing angle equations (12)-(13) and for the combiner equations (6)-(8), all a function of the R_{min} and R_{max} of the initial one-transistor simulations, precisely yield the targeted



(a)



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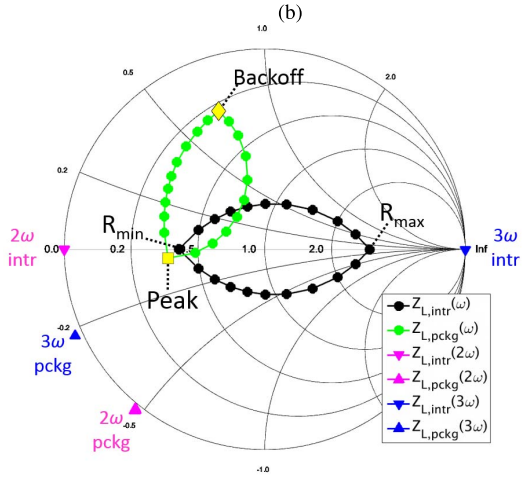


(c)

Fig. 6. Simulation results for a mixed-mode outphasing PA using embedding device model at a single frequency 1.95 GHz with $V_{DD} = 24.6$ V and $V_{GG} = -2.9$ V. (a) Output power versus optimal drain efficiency at the PRPs. (b) $|V_{GS}(\omega)|$ at plane G' and Outphasing angle at plane D' versus output power. (c) $Z_{L,intr}(\omega, 2\omega, 3\omega)$ and $Z_{L,pckg}(\omega, 2\omega, 3\omega)$.

output powers, efficiencies, PBPR (backoff) and loads R_{min} and R_{max} at peak and backoff.

Beside bypassing the need for multi-harmonic sourcepull and loadpull, one further advantage of working at the CSRPs with the embedding device model is that this enables us to derive a fully analytic expression for the outphasing angles θ_B and θ_P using R_{min} and R_{max} as design parameters. Further as we shall verify in the next section using harmonic balance simulations, the analytic formulae for the outphasing angles at the CSRPs and PRPs, provides a very accurate estimate of the

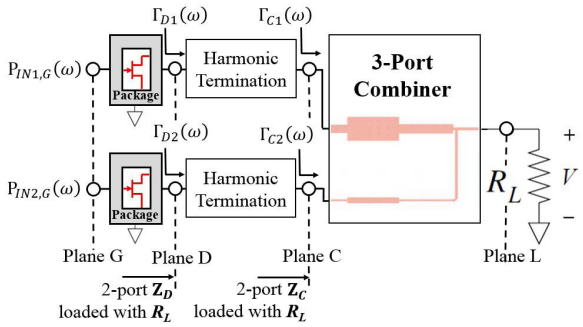


Fig. 7. Dual-input outphasing PA circuit realized at the PRPs after the nonlinear embedding process. Plane G: Package gate reference planes. Plane D: Package drain reference planes. Plane C: Physical combiner reference planes.

outphasing angles numerically calculated from the projected peak and backoff loads at the PRPs [30].

D. Verification of the Outphasing Combiner Theory at Both the Intrinsic and Package Reference Planes

We proceed now to the verification of the operation of the class-F outphasing PA prototype using the embedding device model and the ideal lossless and reciprocal outphasing combiner network derived in the previous section. Fig. 6 shows the results obtained from backoff to peak power. The trajectories of the intrinsic drain loads Z_{L1} (top) and Z_{L2} (bottom) in Fig. 4 noted as $Z_{L,intr}(\omega)$ are plotted (black dots) in the Smith chart in Fig. 6(c)) as the outphasing angle varies from backoff to peak. These intrinsic load trajectories clearly achieve two pure real loads right on the real axis at peak and backoff, indicating that the loads R_{min} and R_{max} have been successfully generated by the combiner at plane D'. The trajectories of the fundamental drain load at the PRPs $Z_{L,pckg}(\omega)$ are projected by the embedding device model and plotted (green dots) in the Smith chart in Fig. 6(c). The yellow symbols in Fig. 6(c) shows the package drain load impedances at backoff and peak operation. Since both transistors are operated identically at the peak and backoff power, the package drain impedances overlap. The reflection coefficients of the second (2ω) and third (3ω) harmonics are also plotted before (lower triangles) and after (upper triangles) embedding. A two-port harmonic termination will be designed and connected to plane D as shown in Fig. 7 based on the projected $Z_{L,pckg}(\omega, 2\omega, 3\omega)$. For the purpose of clarity, the projected $Z_{L,pckg}$ at plane D will be represented as Z_D in the rest of the paper.

Fig. 7 shows the final outphasing PA circuit after the nonlinear embedding or projecting process. In the projecting process performed by the embedding model from the CSRPs to PRPs, the transistor drain voltages V_D and currents I_D at the package drain reference plane D are generated for the top and bottom branches. Given the projected voltages and currents at the drain package reference plane D, the two-port $\boldsymbol{Z_D}$ or $\boldsymbol{Y_D}$ matrix can be extracted with the combiner connected to a common load R_L. The technique in Appendix C is then used to extract a reciprocal $\boldsymbol{Z_D}$ matrix and to verify the

TABLE I

COMPARISON OF THE OUTPHASING ANGLES θ_B AND THE LOADS R_{min} AND R_{max} USING THE THEORY, HARMONIC BALANCE SIMULATIONS AND THE TECHNIQUE REPORTED BY ÖZEN *et al.* [30]

R_{min} (Ω)	R_{max} (Ω)	$\theta_{B,intr}$ (deg)	$\theta_{B,pckg}$ (deg)	θ_L (deg)	
20	160	± 38.94 ± 141.06	$= \theta_{B,intr}$	$+136.00$ -136.00	Theory
20 20	160.04 160.04	-39.01 -140.98	-38.98 -141.07	$+135.99$ -135.98	Simulation
NA NA	NA NA	NA NA	± 37.78 ± 142.22	NA NA	[30]

lossless criteria $\mathcal{R}^2(Z_{12})=\mathcal{R}(Z_{11})\mathcal{R}(Z_{22})$ as reported in [16] and [37]. Alternatively, the mixed analytical and numerical technique reported in [30, eqs. (8)–(10)] which relies only on the projected impedances Z_D at peak and backoff, can be used to verify the accuracy of the method presented in Appendix C as is investigated next.

The comparison of the results obtained from 1) the analytic theory, 2) harmonic balance simulations using the proposed theory and 3) the numerical technique reported by Özen *et al.* [30] are presented in Table I. Note that the numerical technique in [30] is applied on the load impedances Z_D obtained at peak and backoff power levels from the embedding process. Table I shows that the four outphasing angles $\pm 38.94°$ and $\pm 141.06°$ predicted by the analytic equation (12) at the PRPs are nearly the same as the four analytic solutions obtained from the harmonic balance simulation and in close agreement with the numerical technique reported in [30].

In conclusion, the four outphasing angle solutions at the intrinsic drain match well with the outphasing angle solutions calculated by Özen *et al.* at the transistors' PRPs. Unlike the approach used in [30] and elsewhere which requires the use of multi-harmonic loadpull measurements, simulations, and a numerical search to find the outphasing angle for a given backoff factor γ, an analytic solution is provided by the compact equation (12) based only on the optimal R_{min} and R_{max} selected from the simple single-transistor initial class-F design (see Fig 3). Further, once the R_{min}, R_{max}, and $|V_{GS}(\omega)|$ have been selected based on the desired output power, efficiencies, and PBPR, all the information required to design the lossless and reciprocal outphasing PA at the PRPs is available based upon a single simulation with the embedding model at both the peak and backoff powers.

Fig. 8 summarizes the complete design flow from the single transistor simulation to the realization of the harmonic termination and outphasing combiner to be discussed in Sec. III.

III. CLASS-F HARMONIC TERMINATION AND OUTPHASING COMBINER SYNTHESIS

As verified in Fig. 6(c), the intrinsic fundamental load $Z_{L,intr}(\omega)$ (black circles on the real axis) are pure real at both peak and backoff powers at the operating frequency. With the $Z_{L,packg}(\omega, 2\omega, 3\omega)$ projected by the nonlinear embedding process, a realizable two-port $\boldsymbol{Z_D(\omega)}$ matrix of combiner loaded with R_L can be extracted using Appendix C as shown

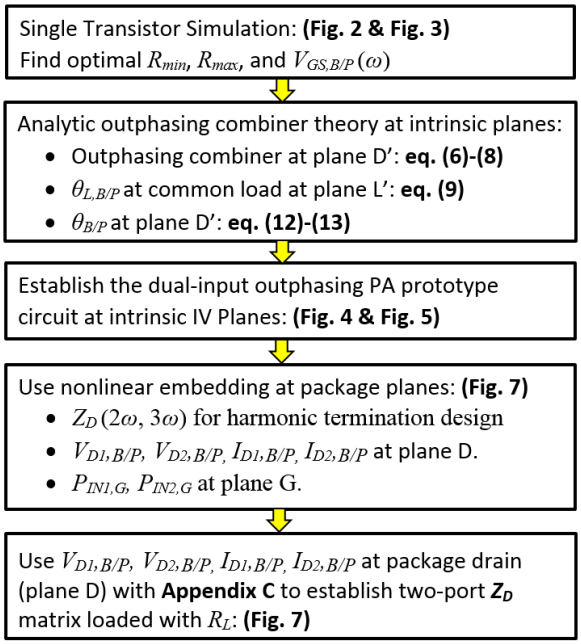


Fig. 8. Design flow of the outphasing PA with the new design equations.

below.

$$\boldsymbol{Z_D(\omega)} = \begin{bmatrix} 0.29 + j14.19 & 2.96 - j23.45 \\ 2.96 - j23.45 & 30.29 + j17.64 \end{bmatrix}. \quad (14)$$

To realize the above 2-port $\boldsymbol{Z_D(\omega)}$, some researchers have relied on a combined circuit design technique including both fundamental and multi-harmonic control. This approach is usually used for wideband design to ensure a good fundamental control while selectively sacrificing the high-order harmonics control [4], [30]. On the other hand, separately designing the harmonic termination and combiner allows for a more precise control of the high-order harmonics while minimizing the impact on the fundamental response at the center frequency. Although the proposed analytic outphasing combiner theory in this paper is not developed for a wideband design, it can be noted that with the careful design of the harmonic termination circuit, an acceptable bandwidth larger than 100 MHz can be achieved.

A. Class-F Harmonic Termination Design and Synthesis

In order to obtain a class-F behavior at the center frequency with an acceptable bandwidth, a stepped-impedance low-pass filter has been designed to implement the second and third harmonic termination networks. This filter provides the $\Gamma_D(n\omega)$ reflection coefficiencts generated by the embedded mode. In addition, the transmission coefficient phase of this low-pass harmonic termination (HT) filter was constrained to verify $\angle S_{21}^{(\mathrm{HT})} = 0°$ or $180°$ so as to facilitate the subsequent design of the combiner at the fundamental frequency using the synthesis technique of Appendix C. Under this condition, the combiner matrix $\boldsymbol{Z_C}$ at plane C is nearly equal to $\boldsymbol{Z_D}$ at plane D for the center frequency.

The amplitudes of the S-parameters $S_{ij}^{(\mathrm{HT})}$ versus frequency of the stepped-impedance harmonic filter designed for the

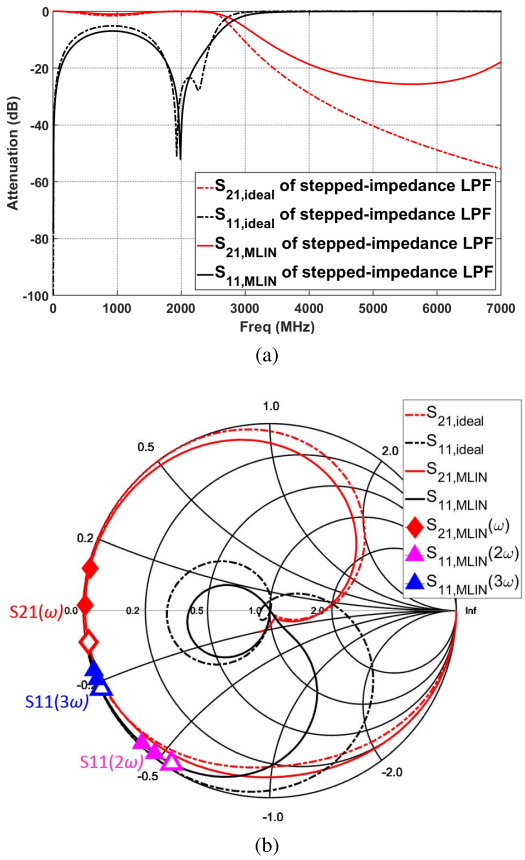


Fig. 9. Simulated results of ideal and microstrip-line based stepped-impedance low-pass filter (harmonic termination). (a) Frequency response of $|S_{11}^{(\mathrm{HT})}(\omega)|$ and $|S_{21}^{(\mathrm{HT})}(\omega)|$. (b) Frequency trajectory of S_{11} and S_{21} on the Smith chart.

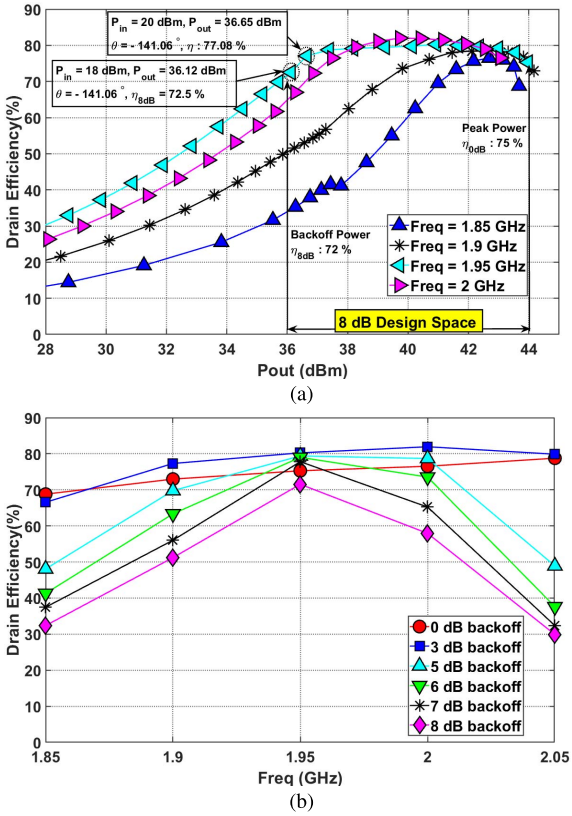


Fig. 10. (a) Simulated drain efficiency versus output power for different frequencies and (b) drain efficiency versus versus frequency for different backoffs. The outphasing angle θ is fixed to $-141.06°$ below the backoff power for each frequency.

harmonic termination are shown in Fig. 9(a). The angle $\angle S_{21}^{(\mathrm{HT})}(\omega_c)$ of the filter was set to be approximately 180° at the center frequency of 1.95 GHz as shown in Fig. 9(b). The phase dispersion of the transmission coefficient $\angle S_{21}^{(\mathrm{HT})}(\omega)$ is allowing the critical impedance $Z_{L,intr}(2\omega)$ but also $Z_{L,intr}(3\omega)$ to remain as close as possible to the ideal values established by the embedding model within an acceptable bandwidth of 150 MHz. The phase change of $S_{21}^{(\mathrm{HT})}(\omega)$ at the fundamental is seen to be maintained within the range of 190° to 166° within a bandwidth of 150 MHz.

B. Outphasing Combiner Synthesis With Designed Harmonic Termination

Once the harmonic circuit design is completed, an ABCD matrix of the harmonic termination circuit can be used to calculate the new voltages and currents at plane C in Fig. 7. Appendix C can be used with the new voltage and current to create a new 2-port $\boldsymbol{Z_C(\omega)}$ for the combiner loaded with R_L at the plane C. The combiner at plane C is then designed using stepped-impedance microstrip lines. The 2-port $Z_C(\omega)$ matrix of the coupler is converted into S-parameters which define the optimizing targets for the 3-port lossless coupler terminated with the load (R_L). The combiner circuit consists of two branches as shown in Fig. 7. Each branch is realized using asymmetric stepped-impedance microstrip-lines. 3 and 4 sections are used for the top and bottom branches respectively. The length and width of the sections are optimized till the circuit approaches the targeted amplitudes and phases of $S_{11}^{Comb}(\omega)$, $S_{12}^{Comb}(\omega)$, $S_{22}^{Comb}(\omega)$ for the coupler.

Fig. 10 shows (a) the simulated drain efficiencies versus output power and (b) the simulated drain efficiencies versus frequency obtained for the cut-ready PA circuit including the stepped-impedance-based output harmonic termination, outphasing combiner circuits, and the input stabilizing and biasing circuits. At center frequency 1.95 GHz, the drain efficiency is 75% and 72% at peak power (44 dBm) and 8 dB backoff power (36 dBm), respectively. Even though the proposed theory is only developed for single frequency, the 8dB backoff drain efficiency is seen in Fig. 10(b) to be higher than 50% within a bandwidth of at least 100 MHz (1.9 GHz to 2GHz).

IV. CW Measurements Using Large Signal Network Analyzer

Fig. 11(a) shows the complete outphasing PA circuit schematic diagram and Fig. 11(b) a picture of the fabricated PA. The circuit is build on a Rogers RT/duroid 5880 substrate with 31 mils thickness and 2.2 relative dielectric constant. Two RF signal generators (ESG 4438C) are connected to both RF inputs of the outphasing PA (DUT) via two ultra-low-loss directional couplers (RTT0812H) interfacing with

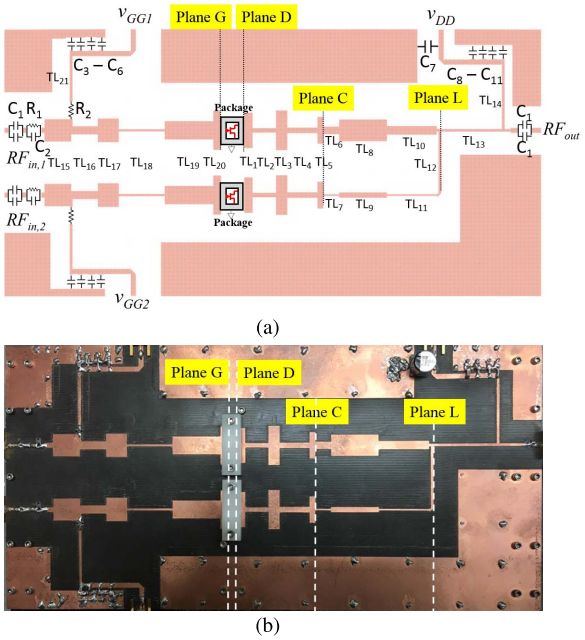


Fig. 11. Complete (a) layout and (b) picture of the Chireix outphasing amplifier.

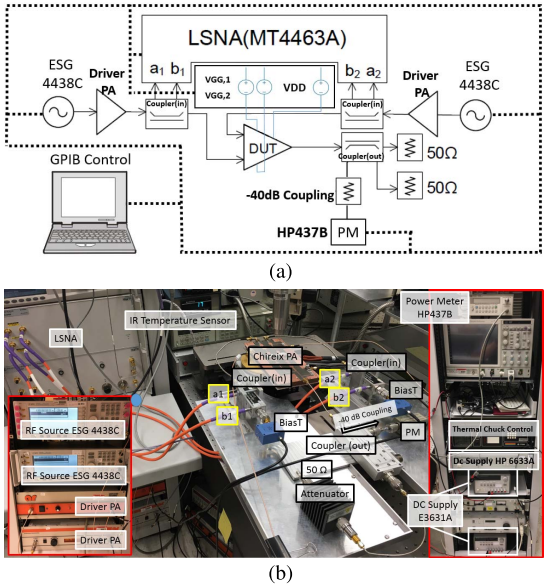


Fig. 12. (a) Schematic and (b) picture of the large signal network analyzer (LSNA) testbed used for the CW measurements.

the large signal network analyzer (LSNA, MT4463A). The LSNA is used for CW measurement as shown in Fig. 12. The output of the outphasing circuit is connected to the power meter (HP437B) through a 20 dB directional coupler (ZGDC20-33HP+) and a 20 dB attenuator. The output port of the coupler is terminated by a 50 Ω power load.

The complete CW drain efficiency, PAE, and gain obtained from the LSNA measurements at 1900 MHz are shown in Fig. 13. Two different mixed-mode operations are highlighted: (1) the optimum-efficiency and (2) the constant-gain modes.

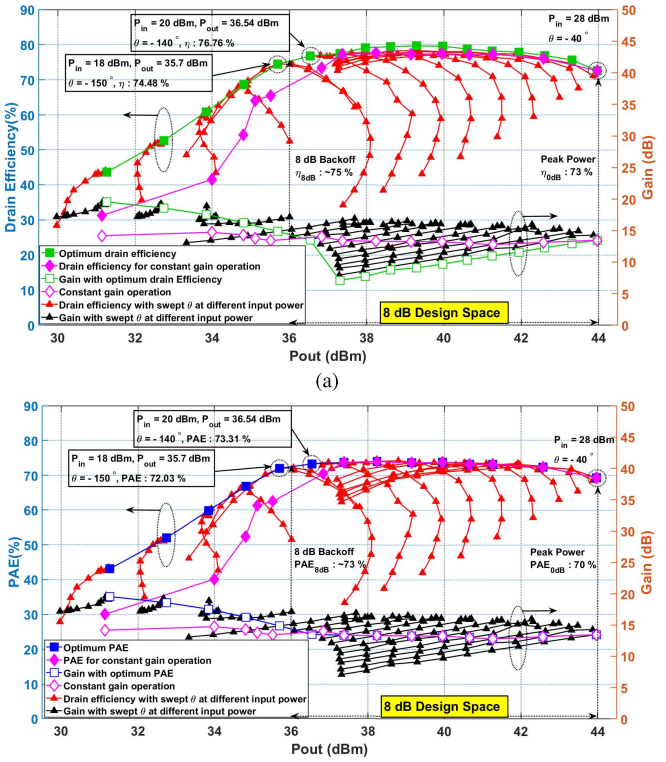


Fig. 13. LSNA measurements of (a) the CW drain efficiency and gain versus the outphasing angle θ for 15 different input power levels at 1900 MHz and (b) the CW PAE and gain versus the outphasing angle θ for 15 different input power levels at 1900 MHz.

The optimum drain-efficiency and PAE modes are shown in Fig. 13(a) and Fig. 13(b), respectively. Each red triangle curve represents different P_{in} levels used. The same incident power $P_{in,1} = P_{in,2} = P_{in}$ are used for the entire P_{in} range from 10 to 28 dBm. For the low power region from 10 to 18 dBm, the P_{in} step size is set to be 2 dB while sweeping the outphasing angle from $-200°$ to $-100°$ with $10°$ step size. For the medium-to-high power region from 19 to 28 dBm, the P_{in} step size is set to be 1 dB while sweeping the outphasing angle from $-140°$ to $-40°$ with $10°$ step size. The top green and blue solid circles represent the optimum drain efficiencies and optimum PAEs. The bottom green and blue hollow circles show the corresponding power gains associated with optimum drain efficiency and optimum PAE.

The constant gain mode is shown in both Fig. 13(a) and 13(b). The top magenta solid circles represent the drain efficiency and PAE with constant gain operation. The bottom magenta hollow circles show the corresponding power gains with constant gain operation. In this case, the incident power $P_{in,1} = P_{in,2} = P_{in}(P_o)$ projected by embedding are only used within 8 dB PAPR design space (36 to 44 dBm). Below the 8 dB PAPR design space around 36 dBm, $P_{in,1}$, $P_{in,2}$, and θ are selected to achieve constant gain operation.

For the optimum drain efficiency mode, the PA enters the constant envelope mode earlier at 37.5 dBm, which leads to a non-linear gain drop as shown in the green hollow circles

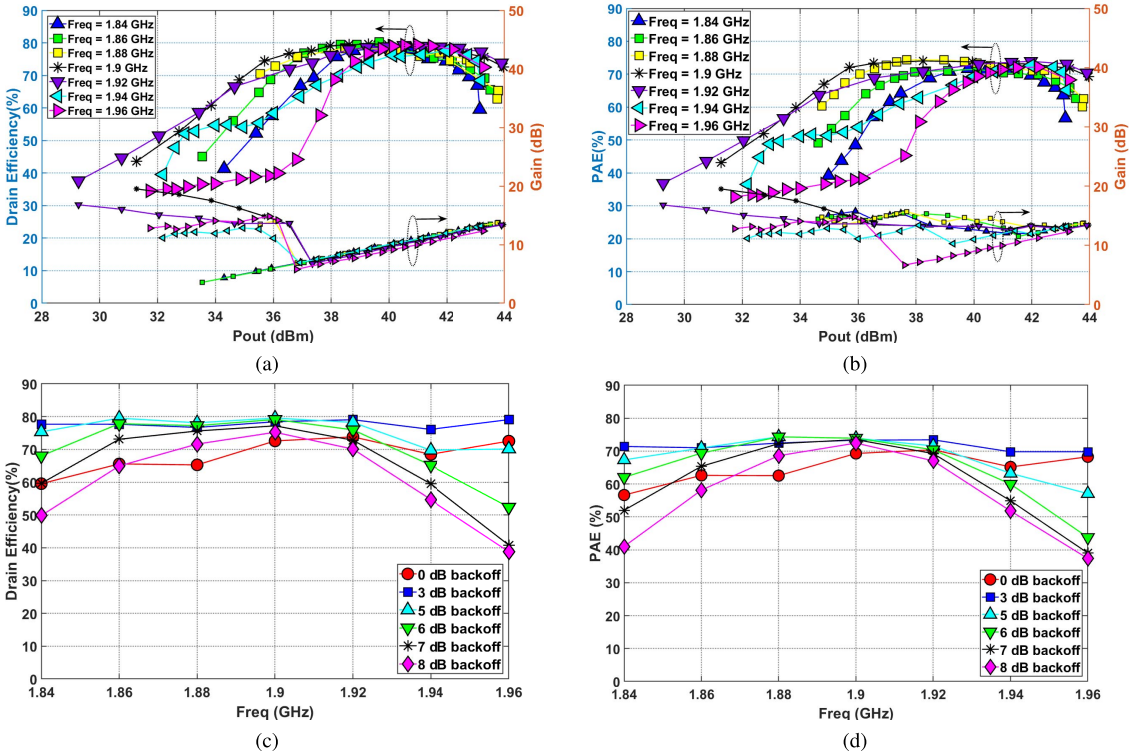


Fig. 14. (a) Measured optimum drain efficiency and output power results from 1.84 GHz to 1.96 GHz (b) Measured optimum PAE and output power results from 1.84 GHz to 1.96 GHz (c)Measured drain efficiency results versus frequency from 1.84 GHz to 1.96 GHz. (d) Measured PAE results versus frequency from 1.84 GHz to 1.96 GHz.

in Fig. 13(a). On the other hand, constant gain mode offers a more stable gain by selectively sacrificing the drain efficiency in the low power region. A look-up table (LUT) for the incident power levels, outphasing angles, and output power levels is created to sustain the constant-gain mode of operation. This constant gain based LUT will be used for the linearization in Section V.

Fig. 14(a) and (b) shows the measured optimal drain efficiency and PAE envelope at each frequency, respectively. Due to the device variation and circuit fabrication error, a 50 MHz frequency shift can be observed compared to the simulations in Fig. 10. Around the frequency range from 1.84 to 1.96 GHz, the mixed-mode operation is seen to yield higher efficiencies with lower input powers especially in the medium-to-high backoff operation range. For the center frequency range from 1.88 GHz to 1.92 GHz, the PAE nearly maintains a constant value (flat curve) within a 8 dB backoff range down to 36 dBm. The best performance is around 1.9 GHz that yields 75.22% drain efficiency and 73% PAE at 35.97 dBm with 8 dB backoff. The slightly higher measured performance at back-off than in simulation is due to additional tuning of the outphasing angle, which was held fixed at $\theta = -141.06°$ in the original simulation. It is worth noting that the 10 dB backoff PAE can be maintained above 60% at 1.9 GHz. Overall with 5 dB and 8 dB backoff, the drain efficiency can be larger than 70% and 50%, respectively, within 100 MHz bandwidth as shown in Fig. 14(c).

Finally, the CW measurement results of the state-of-the-art modulated outphasing PAs were summarized in table II. The 8-dB backoff drain efficiency and PAE results at the center frequency obtained in this paper is seen to be highly competitive when compared to the cutting edge outphasing PA research. These results convincingly validate the completeness and effectiveness of the proposed outphasing PA design methodology.

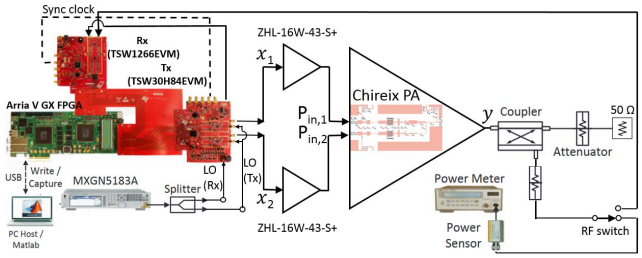


Fig. 15. Digital pre-distortion testbed.

V. Modulated Signal Measurements and Linearization

To characterize its dynamic response, the Chireix PA was tested with modulated signals. A 3.84 MHz WCDMA signal with PAPR of 9.5 dB and a 10 MHz LTE signal with PAPR of 9.6 dB were selected for testing.

A. Digital Control for the Dual-Input PA

The dual-input-single-output (DISO) digital front end FPGA testbed with two RF transmitters and one RF receiver shown in Fig. 15 is used for modulated measurements. The FPGA

TABLE II

COMPARISON OF THE CW PERFORMANCE WITH STATE-OF-THE ART LOAD MODULATED PAS

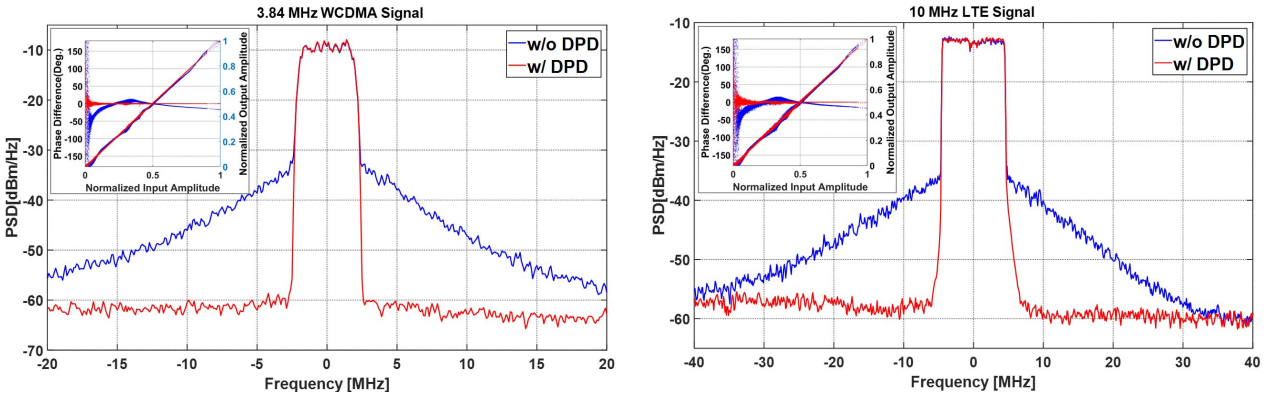
Technology	Architecture	f_0 (GHz)	$P_{o,peak}$ (W)	$\eta_{DE,peak}/PAE_{,peak}$ (%)	$\eta_{DE,8dB}/PAE_{,8dB}$ (%)	Ref.
GaN	Class-B outphasing	2.14	90	$72^*/70^*$	$46^*/42^*$	[14]
GaN	4-Way outphasing	2.14	60	$72/-$	$55/-$	[15]
GaN	4-Way outphasing	2.14	105	$52/-$	$55/-$	[17]
GaN	Class-E outphasing	2.3	70	$70/68^{**}$	$55/48^{**}$	[20]
GaN	Load-pull Based	2.1	29.2	$-/65$	$-/49$	[16]
GaN	Doherty-outphasing	2.14	112	$66/-$	$60/-$	[23]
LDMOS	RF-input Doherty-outphasing	2.17	138	$56/-$	$50/-$	[27]
65 nm CMOS-GaN	Cont. Class-E outphasing	0.9	> 24	$79/75^{**}$	$80/60^{**}$	[30]
CMOS-GaN	Class-E outphasing	1.95	19	$70/-$	$70/-$	[31]
GaN	Class-J outphasing	0.9	28.18	83/76	65/58	[18]
GaN	Class-AB outphasing	1.7	20	$-/50$	$-/23^*$	[26]
GaN	Class-F outphasing	1.9	25.1	73/70	75/73	**This work**

* Graphically estimated.
** Line-up efficiency.

TABLE III

AVERAGE EFFICIENCY BEFORE AND AFTER LINEARIZATION

	f_o (GHz)	Signal	PAPR (dB)	$P_{inc,avg}$ (dBm)	$P_{o,avg}$ (dBm)	Gain (dB)	$\eta_{DE,avg}$ (%)	ACLR_1 (dBc)	NMSE (dB)
Before DPD	1.9	3.84 MHz WCDMA	9.57	17.17, 19.14	34.46	13.18	59.5	$-27.7, -27.51$	-18.88
After DPD	1.9	3.84 MHz WCDMA	9.51	17.6, 19.3	34.5	12.95	59.5	$-50.96, -51.48$	-38.53
Before DPD	1.9	10 MHz LTE	9.64	17.01, 18.09	34.43	13.33	59.32	$-27.69, -29.42$	-18.82
After DPD	1.9	10 MHz LTE	9.6	17.44, 19.3	34.46	13	59.4	$-45.33, -46.4$	-33.92



(a) (b)

Fig. 16. Power spectral density, AM/AM, and AM/PM results before DPD (blue) and after DPD (red) at 1.9 GHz implemented with (a) 3.84 MHz WCDMA signal. (b) 10 MHz LTE signal. Both transistors are operated with $V_{DD} = 25$V and $I_{DD} = 5$mA.

board is used as a pattern generator along with a data capture card using Texas Instruments' DAC (TSW30H84EVM) and ADC (TSW1266EVM) boards. The entire digital signal processing including DPD coefficient calculation is processed in a PC with MATLAB. Two Mini-Circuits' ZHL-16W-43-S+ are used as driver amplifiers for both channels. Phase and power calibration are implemented in order to accurately obtain the desired mixed-mode outphasing control for dual-input operation. As mentioned in Section IV, the constant-gain mixed-mode operation shown in Fig. 13(a) is used for generating a look-up table (LUT) including the incident power ($P_{in,1/2}$), outphasing angles (θ) at plane G, and the output power (P_o) at 1.9 GHz. Representing the modulated RF input signal in discrete-time form as $x(n) = |x(n)| \exp[j\phi_x(n)]$, the two inputs of the PA were controlled by complex predistorted modulated signals $x_1(n)$ and $x_2(n)$, defined respectively as:

$$x_1(n) = \sqrt{P_{in,1}\left[P_o(n)\right]} \exp j \left\{\phi_x(n) + \frac{1}{2}\theta\left[P_o(n)\right]\right\}, \quad (15)$$

$$x_2(n) = \sqrt{P_{in,2}\left[P_o(n)\right]} \exp j \left\{\phi_x(n) - \frac{1}{2}\theta\left[P_o(n)\right]\right\}, \quad (16)$$

where $P_{in,1/2}[P_o(n)]$ are the incident powers at ports 1 and 2 and $\theta[P_o(n)]$ is the outphasing phase difference, both of them a function of the targeted output power $P_o(n) = P_{o,peak} \times |x(n)|^2$. The use of the LUT to control the dual-input PA enables one to implement a preliminary linearization (constant gain amplitude) which solely relies on the quasi-static characteristics established by the CW LSNA measurements.

TABLE IV
COMPARISON OF MODULATED SIGNAL MEASUREMENTS WITH STATE-OF-THE ART OUTPHASING PAS

Technology	Arch.	Signal	f_0 (GHz)	BW (MHz)	PAPR (dB)	$P_{o,peak}$ (W)	$\eta_{DE,avg}$ (%)	ACLR $_1$ (dBc)	Ref
GaN	Class B outphasing	W-CDMA	2.14	3.84	9.6	90	50.5	-47	[14]
CMOS-GaN	Class E outphasing	W-CDMA	2.25	3.84	9.6	70.6	53.5	-49	[20]
LDMOS	Doherty-outphasing	-	2.17	3.84	7.5	138	45.8	-50.2	[27]
GaN	4-input 4-way outphasing	W-CDMA	2.14	3.84	9.15	110	55.6	-33^*	[24]
GaN	Class-AB outphasing	LTE	2.25	10	4	19.95	28.5	-30	[26]
GaN	Class-F outphasing	LTE	1.9	10	9.6	25.46	59.4	$-45.33, -46.4$	**This work**
GaN	Class-F outphasing	WCDMA	1.9	3.84	9.51	25.12	59.32	$-50.96, -51.48$	**This work**

* No DPD was used.

B. Digital Predistortion Results

The Chireix PA was linearized by predistorting the input signal $x(n)$ using the technique of indirect learning. The input data $x(n)$ were modeled in terms of the output data $y(n)$ using a generalized memory gain-functions G_p^m with memory depth M of 3 and cross term depth P of 3:

$$x(n) = \sum_{m=0}^{M-1} \sum_{p=0}^{P-1} G_p^m \left(|y(n-m-p)|^2 \right) y(n-m). \quad (17)$$

The memory gain functions $G_p^m(|y|)$ are implemented using a cubic spline basis with 30 segments [38].

The measurement results before and after linearization are summarized in Table III. Fig. 16(a) and (b) show the output spectra of the PA, AM/AM, and AM/PM performance with and without DPD when using 3.84 MHz WCDMA signal and 10 MHz LTE signal as a benchmark [14], [20], [24], [26], and [27]. The adjacent channel leakage power ratio (ACLR) after linearization is -50.96 dBc for the WCDMA case and -45.33 dBc for the LTE case, which means the PA satisfies the linearity requirements of 3GPP TS 36.141 for both the WCDMA and LTE cases when DPD was applied. It can be seen in Table IV that the average efficiencies above 59% obtained with this PA for both WCDMA and LTE compares favorably to other published works.

VI. CONCLUSION

A new design procedure for a Chireix outphasing PA operating in mixed mode was presented and experimentally verified in this paper. The design procedure is significantly simplified as compared to conventional methods through its use of the embedding model. Only single-transistor operation needs to be considered initially to determine the operating points at peak and backoff power, due to the identical operation of the two outphasing transistors at these two power levels. Furthermore, the load impedances at these power levels are constrained to be pure real because the design is performed at the intrinsic plane instead of the device plane of the transistor. Simulation of the single-transistor operation furthermore yields the fundamental RF gate drives at peak and backoff power for mixed-mode operation, which substantially improves efficiency at backoff.

Once the required resistive fundamental intrinsic drain loads and the amplitude of fundamental RF gate drives at peak and backoff power are found, a fully analytic theory enables implementation of a mixed-mode Chireix outphasing PA. This theory provides the prototype combiner at the intrinsic drain current-source reference planes, and the outphasing angles at peak and backoff powers. Simulation of the two-way mixed-mode outphasing PA with an embedding model then yields (1) the two-port impedance matrix of the combiner, and (2) the required multi-harmonic loads at the drain side of the package reference planes. Comparing the results to those based solely on the package reference plane impedances [30] shows a close agreement.

The theory is validated with a hardware demonstration with a center frequency of 1.9 GHz, with peak drain efficiency of 72.58% and efficiency of 75.22% at 8 dB backoff. A constant-gain LUT based on CW LSNA measurement data is used at the center frequency to generate the modulated outphasing signals for driving the dual-input Chireix PA before DPD is applied. With DPD, the PA satisfies the linearity requirements of 3GPP TS 36.141 for both 3.84 MHz WCDMA and 10 MHz LTE signals, with average efficiencies of 59.5% and 59.4% respectively.

APPENDIX A
DESIGN OF THE PROTOTYPE COMBINER AT THE INTRINSIC CURRENT-SOURCE REFERENCE PLANE

The normalized currents at the common load side of the current-source Chireix prototype combiner can be written as:

$$I_{L1n} = \frac{I_{L1}}{\overline{I_L}(|V_{GS}(\omega)|)} = \exp\left(+j\frac{\theta_L}{2}\right) = \exp\left(j\theta_{L,1}\right),$$
$$I_{L2n} = \frac{I_{L2}}{\overline{I_L}(|V_{GS}(\omega)|)} = \exp\left(-j\frac{\theta_L}{2}\right) = \exp\left(j\theta_{L,2}\right),$$
$$I_{Ln} = \frac{I_L}{\overline{I_L}(|V_{GS}(\omega)|)} = 2\cos\left(\frac{\theta_L}{2}\right).$$

The voltages and currents at the drain current-source reference plane of transistor 1 (left side) of the Chireix combiner prototype can be expressed as:

$$V_{1n} = \beta I_{Ln} + j\alpha I_{L1n},$$
$$I_{1n} = jbI_{Ln} + aI_{L1n},$$

where $V_{Ln} = R_L I_{Ln}$, β/R_L, $j\alpha$, jb/R_L and a are the ABCD parameters of the lossless reciprocal ($a\beta + b\alpha = R_L$) 2-port network connecting the load R_L to the left transistor 1.

Separating the real and imaginary parts we get:

$$V_{1n} = [2\beta\cos\theta_{L1} - \alpha\sin\theta_{L1}] + j\alpha\cos\theta_{L1},$$
$$I_{1n} = a\cos\theta_{L1} + j\left[a\sin\theta_{L1} + 2b\cos\theta_{L1}\right].$$

The voltage V_{1n} and current I_{1n} must be in phase so that the peak and backoff load impedances at the CSRPs are both pure real. This leads to the following required identity:

$$(4b\beta - a\alpha)\cos^2\theta_{L1,B} + 2\,(a\beta - b\alpha)\cos\theta_{L1,B}\sin\theta_{L1,B} = \alpha a \sin^2\theta_{L1,B}. \quad (18)$$

When $\theta = 0$ at peak power, the first term multiplying $\cos^2\theta$ must vanish:

$$\frac{a}{4b} = \frac{\beta}{\alpha} = r.$$

At backoff the remaining terms in (18) must vanish as well for the outphasing angle $\theta_{L,B}$:

$$\tan\theta_{L1,B} = \tan\frac{\theta_{L,B}}{2} = \frac{2\,(a\beta - b\alpha)}{a\alpha} = \frac{r}{2} - \frac{2}{r}.$$

With the conditions above, the two pure real loads, R_{min} at peak for $\theta_L = 0$ and R_{max} at backoff for $\theta_{L,B}$ are then given by;

$$R_{min} = \frac{V_{1n,P}}{I_{1n,P}} = \frac{j\alpha I_{1n,P} + \beta I_{Ln,P}}{aI_{1n,P} + jbI_{Ln,P}} = \frac{2\beta + j\alpha}{a + j2b} = \frac{\alpha}{2b},$$
$$R_{max} = \frac{V_{1n,B}}{I_{1n,B}} = \frac{j\alpha I_{1n,B} + \beta I_{Ln,B}}{aI_{1n,B} + jbI_{Ln,B}} = \frac{4R_{min}}{r^2}. \quad (19)$$

Using (19) the outphasing angle $\theta_{L,B}$ is obtained from:

$$\tan\left(\frac{\theta_{L,B}}{2}\right) = \frac{r}{2} - \frac{2}{r} = \pm\left(\sqrt{\frac{R_{min}}{R_{max}}} - \sqrt{\frac{R_{max}}{R_{min}}}\right).$$

Appendix B
Outphasing Angle at the Drain Current-Source Reference Plane

The 2-port matrix of the combiner-plus-load is obtained from (10) using:

$$\boldsymbol{Z_{D'}} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{12} & Z_{22} \end{bmatrix} = \boldsymbol{I_{D'}} \begin{bmatrix} R_{max} & 0 \\ 0 & R_{min} \end{bmatrix} \boldsymbol{I_{D'}}^{-1}.$$

To simplify the derivation we use here $I_1 = \exp(j\theta)I_2$ and $I_2 = |I_2|$ for evaluating $\boldsymbol{Z_{D'}}$:

$$\begin{aligned}
\left|\boldsymbol{I_{D'}}\right| Z_{11} &= R_{max} I_{1,B} I_{2,P} - R_{min} I_{1,P} I_{2,B} \\
&= |I_P||I_B| \left(R_{max} e^{j\theta_B} - R_{min} e^{j\theta_P}\right), \\
\left|\boldsymbol{I_{D'}}\right| Z_{12} &= I_{1,P} I_{1,B} (R_{min} - R_{max}) \\
&= |I_P||I_B| e^{j\theta_P} e^{j\theta_B} (R_{min} - R_{max}), \\
\left|\boldsymbol{I_{D'}}\right| Z_{21} &= I_{2,P} I_{2,B} (R_{max} - R_{min}) \\
&= |I_P||I_B| (R_{max} - R_{min}), \\
\left|\boldsymbol{I_{D'}}\right| Z_{22} &= R_{min} I_{1,B} I_{2,P} - R_{max} I_{1,P} I_{2,B} \\
&= |I_P||I_B| \left(R_{min} e^{j\theta_B} - R_{max} e^{j\theta_P}\right). \quad (20)
\end{aligned}$$

Enforcing reciprocity ($Z_{12} = Z_{21}$) leads to:

$$\exp(j\theta_P)\exp(j\theta_B) = -1.$$

Thus we have $\theta_B + \theta_P = \pi$ and the determinant of $\boldsymbol{I_{D'}}$ is real:

$$\begin{aligned}
\left|\boldsymbol{I_{D'}}\right| &= |I_P||I_{2,B}| \left[\exp(j\theta_B) - \exp(j\theta_P)\right] \\
&= 2|I_P||I_B|\cos\theta_B.
\end{aligned}$$

Using the real part of $\mathcal{R}[Z_{ij}]$:

$$\mathcal{R}[Z_{11}] = \mathcal{R}[Z_{22}] = 1/2\ (R_{max} + R_{min}),$$
$$\mathcal{R}[Z_{12}] = \mathcal{R}[Z_{21}] = \frac{(R_{max} - R_{min})}{2\cos\theta_B},$$

and enforcing the combiner lossless condition leads then to:

$$\cos^2\theta_B = \frac{(R_{max} - R_{min})^2}{(R_{max} + R_{min})^2}.$$

Appendix C
Package Combiner Plus Load Impedance Matrix

After embedding to the package reference planes, the combiner plus load network can be synthesized using the following 2-port $\boldsymbol{Y}$ matrix.

$$\begin{aligned}
\boldsymbol{M_1} &= \begin{bmatrix} V_{1,P} & V_{2,P} \\ V_{1,B} & V_{2,B} \end{bmatrix}, \\
\boldsymbol{Y_1} &= \begin{bmatrix} Y_{11} \\ Y'_{12} \end{bmatrix} = \boldsymbol{M_1^{-1}} \begin{bmatrix} I_{1,P} \\ I_{1,B} \end{bmatrix}, \\
\boldsymbol{Y_2} &= \begin{bmatrix} Y'_{21} \\ Y_{22} \end{bmatrix} = \boldsymbol{M_1^{-1}} \begin{bmatrix} I_{2,P} \\ I_{2,B} \end{bmatrix}, \\
G_{12} &= \text{sign}\left(\mathcal{R}\{Y_{11}\}\right)\sqrt{|\mathcal{R}\{Y_{11}\}\mathcal{R}\{Y_{22}\}|}, \\
B_{12} &= \text{sign}\left(\mathcal{I}\left\{Y'_{12}\right\}\right)\sqrt{\left|\mathcal{I}\{Y'_{12}\}\mathcal{I}\{Y'_{21}\}\right|}, \\
Y_{21} &= Y_{12} = G_{12} + jB_{12}.
\end{aligned}$$

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