Chireix Amplifier with Enhanced Bandwidth Using Active Load

(Invited Paper)
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***Abstract*—The use of an active load has been recently proposed for the realization of power-efficient broadband balanced amplifiers. The application of an active load to a dual-input Chireix amplifier is investigated in this paper for the purpose of increasing their bandwidth. An embedding device model is used to established the optimal non-Foster loads required for both the transistors to remain operating in class F as the operating frequency deviates from the center frequency. Given the transistors must operate with a constant voltage swing between backoff and peak, it is found necessary for the two transistors to operate with different load impedances as the frequency varies. The required load impedance and outphasing angles for the Chireix operation are obtained using a generalized eigenvalue problem using the Y-matrix of the Chireix combiner loaded with the active load. It is verified that using an active load, it is possible to maintain a high efficiency not only at peak power but also under various backoff power levels over a bandwidth of 1 GHz. Within a 200 MHz bandwidth, the PA is predicted to be able to maintain an efficiency larger than 79% for 6 dB backoff. Further work is required to experimentally validate the proposed technique.**

***Index Terms*—Chireix amplifier, Power amplifier, Embedding device model**

I. Introduction

With the increasing demand for high data-rate communication, power amplifiers (PA) must operate with wider bandwidth while maintaining a high average power efficiency for signals exhibiting a high peak to average power ratio (PAPR).

The design of single-transistor power amplifiers with high efficiency at peak power requires to establish a mode of operation where the power dissipated by the transistor is minimized while providing the desired output RF power. This is traditionally pursued with the help of time-consuming multi-harmonic load and source pull measurements or simulations. Given the power dissipation in the transistor is mostly taking place at the current-source (IV) reference planes, an alternative approach is to first set the desired operating mode at the current-source (IV) reference planes and use an embedding model to predict in a single simulation, the required RF drive and impedance terminations at the package reference planes. Various examples of such designs for class-AB, 2-way Doherty, broadband class-J amplifiers and 2-way Chireix power amplifiers have been demonstrated experimentally [1]-[5].

In the case of the design of broadband amplifiers, the embedding device model facilitates the determination of the non-Foster load which must be approached to operate the PA over a wide range of frequencies [4]. Recently the use of an active load as been proposed to realize the required non-Foster load over a broad bandwidth. The active load was implemented using a balanced amplifier topology realized with two broadband 90 degree hybrid couplers. This yields a multi-input single-output (MISO) power amplifier. It will be verified in this abstract that the output load, typically 50 ohm must be a broadband load for the balanced operation to be sustained. In such a case, a circulator may be used instead to realize the active load without using a balanced topology as is the common practice in active loadpull testbeds.

Combined with envelope tracking, the active-load approach should facilitate the implementation of a MISO PA maintaining an high efficiency over a wide range of backoff powers. However given supply modulation is difficult to implement for a wide bandwidth and high-power operation, it would be desirable to implement the non-Foster active load with the Doherty or Chireix architecture. This approach is theoretically investigated in this paper for the case of a dual input 2-way Chireix power amplifier [7]. Given the design space is increased by four more dimensions for a dual-input Chireix PA with active load, it becomes desirable to make use of the embedding model to streamline the design process and facilitate the determination of the optimal outphasing angle, dual-input power levels and complex active load required for each output power level and frequency to achieve an optimal efficiency over a wide range of frequencies and power.

In the first section of this paper we briefly review the embedding device model and its application to the design a class B amplifier. In the second section we present the non-Foster impedance variation required from the Chireix coupler for broadband operation. In the third section we present the proposed active-load architecture and theoretically investigate its application to a dual-input Chireix amplifier.

II. Embedding Device Model

Device models for field effect transistors usually feature a current source to generate the intrinsic IV characteristics. This current source is embedded in the linear and nonlinear parasitic network of the complete device as shown in Fig. 1. The embedding device model provides direct access to this

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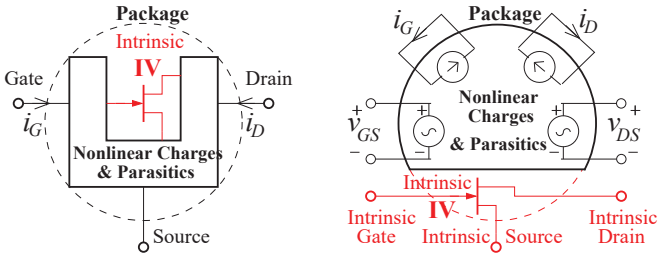
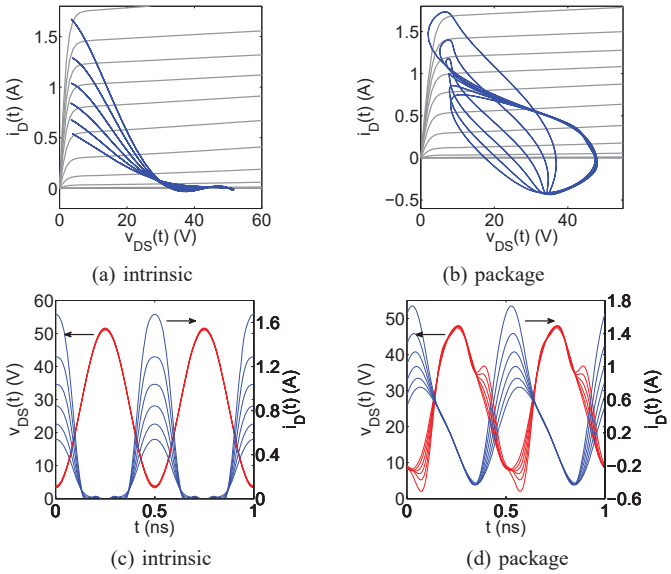


(a) FET model (b) Embedding FET model

Fig. 1: Conventional embedding device model.



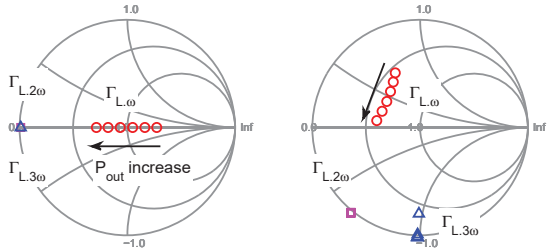
(a) intrinsic (b) package

(c) intrinsic (d) package

Fig. 2: Simulated load lines (a) and (b) and waveforms (c) and (d) at the current-source reference planes and package reference planes, respectively [2].

IV characteristics at the current-source reference planes for use in a circuit simulator. The transistor IV of the embedding device model can then be used to implement any type of mode of operation such as class F. While doing so the required voltage and current waveforms at the package reference planes are simultaneously calculated by the embedding model. The required input-power drive and multi-harmonic impedance terminations required to sustain the desired intrinsic mode of operation are then established. The harmonic source and load impedance terminations are usually slightly active and their reflection coefficients must be renormalized to the edge of Smith Chart for practical implementation. This usually results in a small degradation in performance compared to the ideal case where active loads are used.

Let us consider a transistor operating in class B (second and third harmonic shorted) for different fundamental loads $Z_{L,1}$ and input power drives. Fig. 2 (a) and (c) shows the selected intrinsic class B load lines and waveforms obtained in simulation using the embedding device model. The intrinsic DC-IV curves are shown for reference.



(a) intrinsic (b) package

Fig. 3: The simulated intrinsic load reflection coefficients shown in (a) at the current-source reference planes are mapped using the *embedding device model* to the package reference planes in (b) [2].

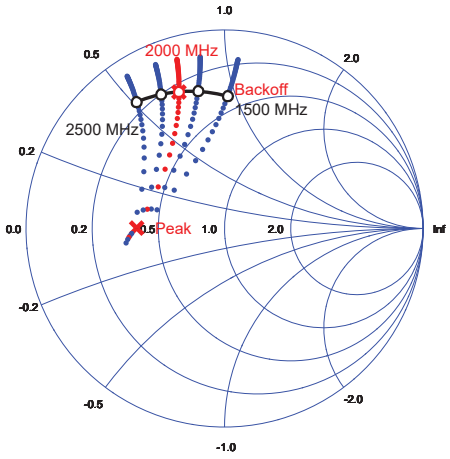


Fig. 4: Optimal device impedance from backoff to peak for five different frequencies from 1500 MHz to 2500 MHz.

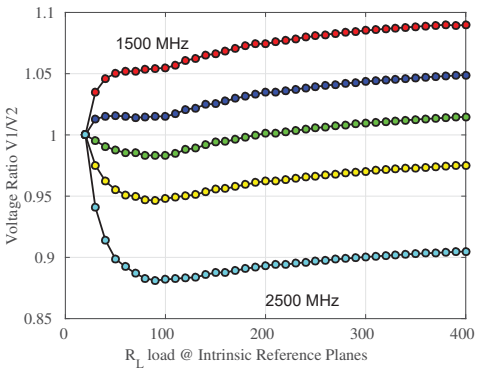


Fig. 5: Ratio for fundamental drain voltage from peak to backoff using the peak reference voltage as reference.

III. Frequency Dependence of the Load for Sustained Class F Operation

We investigate now the frequency dependence of the complex load required to sustain class-F operation. The complex load is obtained using the embedding model while sweeping the real load R_L seen by the intrinsic IV characterics from

400 Ω to 20 Ω from backoff to peak operation. The resulting complex load Z_L at the package reference planes are plotted in Fig. 4 for 1500, 1800, 2000, 2200 and 2500 MHz. It is seen in Fig. 4 that the required complex load Z_L is moving anti-clock wise as the frequency is increased from 1500 MHz to 2500 MHz. This indicates that a non-Foster load is required and thus cannot be realized using a passive circuit.

To optimize the packaged efficiency for each load R_L at the intrinsic reference planes, the intrinsic voltage V_{GS} was swept and the optimal incident fundamental RF power at the packaged reference planes was determined. It is interesting to inspect the resulting fundamental drain voltage at the package reference planes as the load impedance R_L is swept. For each frequency of operation it is found that the drain voltage remains about constant as indicated by the voltage amplitude ratio between the drain voltage V_2 for an intrinsic load R_L and the drain voltage V_1 at peak power. Since the optimal intrinsic drain voltage is approximately the DC drain voltage, it is not surprising that the drain voltage at the package reference planes be also approximately constant as the optimal complex impedance Z_L varies. This will place an important constraint on the class-F operation of a dual-input Chireix PA as the operating frequency deviates from the center frequency.

IV. Broadband PA Archictures Using an Active Load

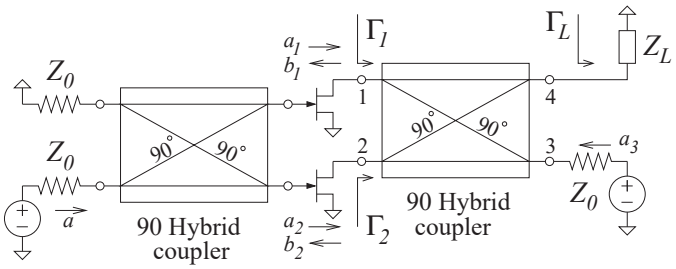


Fig. 6: Balanced amplifier topology proposed in [6] for implementing an active load.

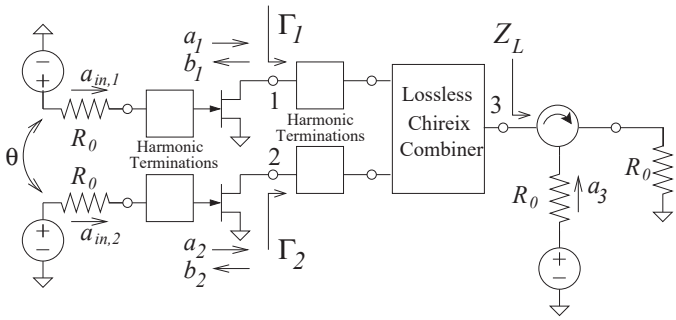


Fig. 7: Chireix power amplifier with an active load implemented using a circulator.

As described in the previous section a non-Foster load must be implemented if class F is to be sustained for broadband operation. The same is also found for class J operation [4]. The use of an active load has been proposed to effectively realize a non-Foster load which rotates anti-clockwise as the frequency is increased. The power efficiency of the amplifier can still be maintained if the power dissipated by the active load remains a small fraction of the output power. The balanced amplifier topology shown Fig. 6 has been proposed in [6] to implement the active load. The reflection coefficients seen by the top and bottom transistors in Fig. 6 are given by:

$$\Gamma_1 = \gamma_{inj}\frac{a_3}{a} + \Gamma_L \quad \text{and} \quad \Gamma_2 = \gamma_{inj}\frac{a_3}{a} - \Gamma_L.$$

Note that the same reflection coefficient correction (same γ_{inj} coefficient) is provided by the signal injected a_3 at port 3 used to tune the load reflection coefficients Γ_1 and Γ_2 seen by the top (1) and bottom (2) transistors respectively. However any mismatch Γ_L presented by the load at the balanced PA output will lead to the two transistor being subjected to opposite reflection contributions coming from Γ_L. Thus it is not possible to use the active load to simultaneously cancel for both transistors, the mismatch introduced by the complex load Z_L as it departs from 50 Ω. In the case of two-way Doherty and Chireix amplifiers the lossless combiner provides to the top and bottom branches, a varying load impedance due the load-pulling between the transistors and a constant load impedance is thus purposely not maintained. We are then forced to look into alternative schemes if we are to use an active load with a Doherty or a Chireix amplifier.

Fig. 7 shows a possible scheme using a circulator to inject the control signal a_3 for tuning the complex load Z_L provided at the output of the Chireix combiner. An example of lossless Chireix combiner circuit is shown in Fig. 8. The Chireix combiner is developed with a 50 Ω impedance termination at port 3 but is terminated by a complex load under active loading when the frequency deviates from the center frequency.

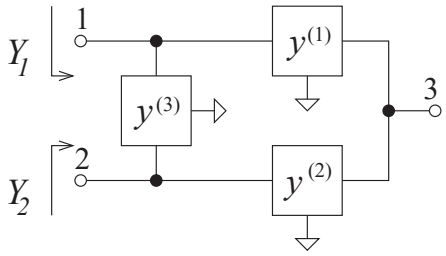


Fig. 8: Model of the lossless Chireix combiner.

The outphasing angle θ required to drive the 2-way Chireix PA can then be obtained from the generalized eigenvectors V_1 and V_2 of the 2-port admittance $\mathbf{Y}_{in}$ defined at port 1 and 2 of the loaded 2-port Chireix combiner in Fig 8:

$$\begin{aligned}\mathbf{I} &= \mathbf{Y}_{in}\mathbf{V} = Y_L\mathbf{R}\mathbf{V} \\ &= \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{12} & Y_{22} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = Y_L\begin{bmatrix} 1 & 0 \\ 0 & r \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}\end{aligned}$$

The generalized eigenvalues of the 2-port admittance $\mathbf{Y}_{in}$ provides the load admittances Y_1 and $Y_2 = r \times Y_1$ for the

$$Z_L(Y_1,Y_2)=\frac{Y_1Y_2-Y_2\left(y_{11}^{(1)}+y_{11}^{(3)}\right)-Y_1\left(y_{22}^{(2)}+y_{22}^{(3)}\right)+\left(y_{11}^{(1)}+y_{11}^{(3)}\right)\left(y_{22}^{(2)}+y_{22}^{(3)}\right)-y_{12}^{(3)2}}{y_{13}^{(1)2}\left(y_{22}^{(2)}+y_{22}^{(3)}\right)+y_{23}^{(2)2}\left(y_{11}^{(1)}+y_{11}^{(3)}\right)-Y_2y_{13}^{(1)2}-Y_1y_{23}^{(2)2}-2y_{13}^{(1)}y_{23}^{(2)}y_{12}^{(3)}} \tag{2}$$

top and bottom transistors when the combiner is driven by the voltages V_1 and V_2 at port 1 and 2 respectively. It is possible to inverse this eigenvalue problem and derive the analytic expression (2) for the complex impedance $Z_L(Y_1,Y_2)$ providing the desired Y_1 and Y_2 load admittances.

At the center frequency we have $Z_L = 50\ \Omega$ ($a_3 = 0$) and the two transistors of the Chireix PA operate at peak and backoff with the same load admittance $Y_1 = Y_2$ and the same drain voltage magnitude $|V_1| = |V_2|$. For this to occur the transistors must be driven with an outphasing phase shift given by $\theta = \angle V_1/V_2$. As Z_L deviates from 50 Ω it is no longer possible to obtain the same load $Y_1 = Y_2$ if we use the same voltage magnitude $|V_1| = |V_2|$. However one can maintain class-F operation if the load admittances Y_1 and Y_2 and corresponding Γ_1 and Γ_2 are located on the load loci specified in Fig. 4 for each of the frequency from 1500 MHz to 2500 MHz. At the same time the voltage amplitude ratio the $|V_1|/|V_2|$ provided by the combiner must match the voltage amplitude ratio obtained from the optimal class F PA operation at the admittances Y_1 and Y_2 respectively (see Fig. 5). The motivation for this strategy is that if the two transistors operate with about the same drain efficiency η, the overall drain efficiency of the Chireix PA is also η even if the two transistors provide different output power contributions.

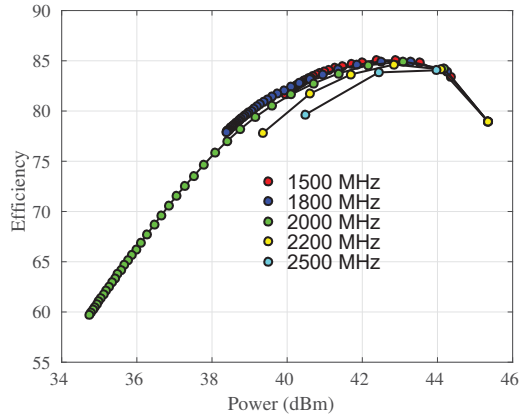


Fig. 9: Efficiency obtained with an active load for five different frequencies from 1500 MHz to 2500 MHz.

The overall drain efficiency η_{tot} of the Chireix PA operated with an active load can be verified to be given by:

$$\eta_{tot}=\frac{P_L}{P_{DC}+P_{inj}}=\frac{\eta_{chir}}{1+\frac{\eta_{chir}}{\eta_{inj}}|\Gamma_L|^2}$$

where Γ_L is the reflection coefficient of the complex active load and where η_{inj} is the drain efficiency of the power amplifier providing the injected power $P_{inj} = |a_3|^2/2$. Fig. 9 shows the overall drain efficiency η_{tot} obtained for $\eta_{inj} \simeq \eta_{chir}$ when a solution can be obtained with an active load. From Fig. 9 it is seen that within a 200 MHz bandwidth the PA is able to maintain an efficiency larger than 79% for 6 dB backoff.

V. Conclusion

In conclusion the design of a 2-way Chireix amplifier using an active load was investigated to generate the required non-Foster impedances under broadband operation. An embedding device model was used to determine the load impedance keeping both transistors operating in Class F mode. However to maintain the same drain voltage at the intrinsic node, it was found necessary to allow for different load impedances for the top and bottom transistors resulting in an unwanted decrease in the peak to backoff power ratio. As a consequence only a moderate bandwidth increase could be obtained. Further the active load connected at the output of the Chireix combiner is not always able to track the required non-Foster load as the operating frequency departs from the center design frequency. Still within a 200 MHz bandwidth the PA is predicted to be able to maintain an efficiency larger than 79% for 6 dB backoff. Note that these simulation predictions are for an ideal lossless combiner circuit implementation. It was further assumed that the harmonics impedance were kept tuned to maintain Class F operation. Further work is required to investigate the application of the active load concept to the design of a Chireix PA operating in class J as this should increase the design space.

Acknowledgment

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