Electrical Characterization of Process Induced Effects on Non-Silicon Devices

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***Abstract*—The influence of the fabrication process on the electrical performance of ZnO and MoS_2 devices are evaluated due to their promise for future internet of things technology applications beyond silicon. Low temperature processing of gate dielectrics introduce new challenges in obtaining optimal device performance. HfO_2 and Al_2O_3 gate dielectrics on ZnO or MoS_2 semiconducting layers are electrically characterized to gain understanding of the influence process-induced effects have on transistor performance.**

Keywords—ZnO; MoS_2; high-k; transistor; TMD, thin-film transistor

I. Introduction

Devices for future Internet of Things (IoT) needs may require non-silicon-based devices for large-area/flexible electronics and Si replacement for continued scaling. These technologies will most likely need a reduced thermal budget compared to conventional CMOS manufacturing, which introduces new challenges in understanding the device materials and fabrication in relation to the electrical performance and reliability. Two key semiconductor materials under substantial investigation are transition metal dichalcogenides (TMDs) and zinc oxide-based low dimensional (i.e., ultra-thin) films. With these materials, field effect transistors are generally the most investigated device architecture. Exploratory devices are configured in a bottom or top gate configuration. We explore the results of the effects of processing on MoS_2 (a TMD semiconductor) and ZnO transistors due to their promise to supplant Si in certain areas of IoT in the future.

II. Experimental

A. ZnO-based Thin-Film Transistor Fabrication

TFTs were fabricated in a bottom-gate, top-contact configuration, (Fig. 1). The process utilizes a substrate consisting of Si with a thermally grown SiO_2 on top. To define the gate, 10/100 nm of Cr/Au is deposited and patterned. Next, different thickness values of HfO_2 or Al_2O_3 gate dielectrics are deposited by ALD at 100 °C. Pulsed laser deposition (PLD) was executed to deposit 50 nm of ZnO at 100 °C directly after and without patterning the dielectric. Then, to serve as a hard-mask and passivation layer, parylene-C (500 nm) is deposited on the ZnO. Source and drain contacts are exposed through the hard-mask to deposit aluminum source-drain contacts. Further details are provided in [1, 2]. Finally, a forming gas anneal at 150°C for 1 hr was done.

*Equal contributors to the work presented herein.

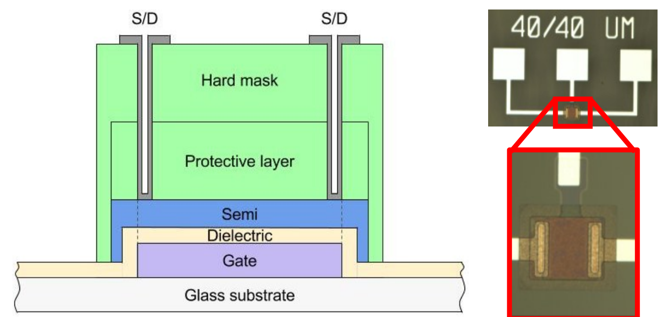

Fig. 1. Schematic cross section and planview image of ZnO TFT used in this work.

TABLE 1. EXPANDED FABRICATION DETAILS OF THE THIN-FILM TRANSISTORS.

Gate Metal	100nm of ITO	
Dielectric	15 nm Al_2O_3	15 nm HfO_2
Semiconductor	45 nm ZnO	
Semiconductor deposition conditions	**100°C**	
	30mTorr O_2	**20mTorr O_2**
Protection layer	250 nm Parylene	
Hard-Mask	250 nm Parylene	
S-D Contacts	150 nm Al	

B. MoS_2 Dual-Gated Field Effect Transistor Fabrication

Dual-gated, few-layer MoS_2 FETs were used as the device for electrical characterization, with the MoS_2 thickness values ranging from 5-10 layers (3-6 nm). Mechanically exfoliated MoS_2 flakes from a synthetic crystal were placed onto Si substrates with 270 nm SiO_2 or 27 nm of Al_2O_3. Using photolithography, a lift-off process was implemented for e-beam evaporation of Au/Ti (100/20 nm) source/drain (S/D) regions. An ultra-high vacuum anneal was performed to remove contaminants on MoS_2 surface [3]. Then, the MoS_2 surface was treated by UV-O_3 [4] and a 6 nm HfO_2/ 3 nm Al_2O_3 layer was deposited at 200˚C by atomic layer deposition (ALD) (Fig. 2). The gate was formed with Au/Cr (100/20nm) metal deposition followed by a lift-off procedure. A 400˚C forming gas (N_2/H_2=95/5) anneal was performed after device fabrication [3].

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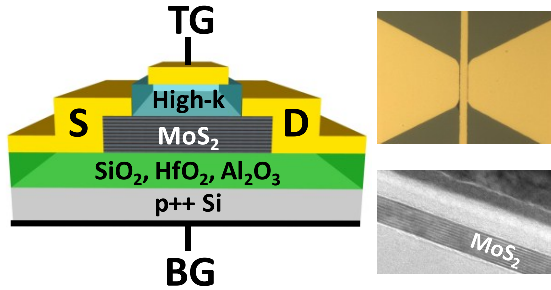

Fig. 2. Schematic and plan view image along with TEM cross section of MoS_2, dual-gated FETs used in this work.

TABLE II. ADDITIONAL MATERIAL DETAILS FOR THE FET STRUCTURE FIG. 1.

Substrate	Bottom Dielectric	TMD	Top Dielectric	Metal Contacts
Highly doped p-type Si	290 nm thermal SiO_2	Mechanically exfoliated MoS_2	~9 nm HfO_2 or 6 nm HfO_2/ 3 nm Al_2O_3	Cr/Au (20 nm/150 nm)
	~10 nm ALD HfO_2			
	~27 nm ALD Al_2O_3			

C. Electrical Characterization

Current – Voltage (I – V) measurements were executed using a Keithley 4200 analyzer. For TFTs, I_d–V_g measurements were employed in the linear regime, where an I_d-V_g hysteresis with a forward sweep to various maximum V_g bias values and back on a given device was measured. Standard I-V performance results were collected for MoS_2 FETs. Variable frequency capacitance – voltage (C-V) measurements were executed using an Agilent E4980A LCR meter to investigate electrically active defects in high-k gate dielectrics.

III. RESULTS AND DISCUSSION

Depositing high-k gate dielectrics at relatively low temperatures may present charge-trapping challenges for these non-Si transistors. Therefore, atomic layer deposited HfO_2 and Al_2O_3 at relatively low temperatures compared to typical Si-based CMOS are evaluated herein.

A. Zinc Oxide Thin-Film Transistor Evaluation

PLD is a technique that enables the low temperature deposition of thin-film semiconductors. The deposition pressure has been shown to impact carrier concentration, mobility, and resistivity of the semiconducting layer [ref]. A simple study of two different deposition pressures was used in the fabrication of ZnO TFTs to investigate the electrical response (Fig. 3). The inset illustrates the influence of pressure on the I_{ON}/I_{OFF} ratio and the subthreshold slope (SS), where 20 mTorr results in the best performance. The 30 mTorr pressure had a higher oxygen flow rate that could have impacted the exposed surface of the underlying Al_2O_3 to make a less robust dielectric and interface compared to 20 mTorr devices.

Dielectrics for large-area/flex-compatible devices require low temperature deposition, which could present challenges in gate dielectric quality. Therefore, relatively low-temperature, atomic layer deposited HfO_2 and Al_2O_3 were evaluated (Figs. 4 and 5, respectively). For HfO_2, results demonstrate that scaling reduces hysteresis, which usually means reduced charge

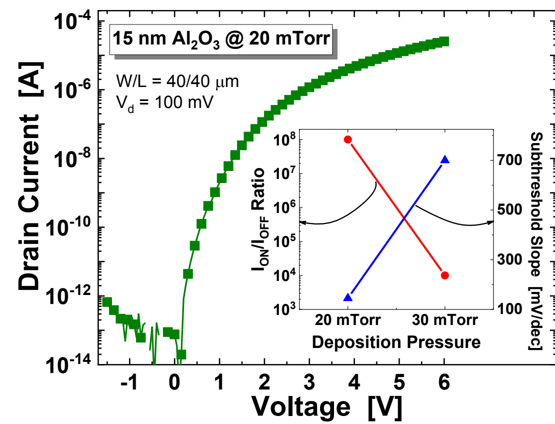

Fig. 3. Effect of PLD pressure of ZnO (Table I). Example result from the optimal 20 mTorr condition. Inset: Deposition pressure adversely affects the I_{ON}/I_{OFF} ratio and subthreshold slope compared to the 30 mTorr condition.

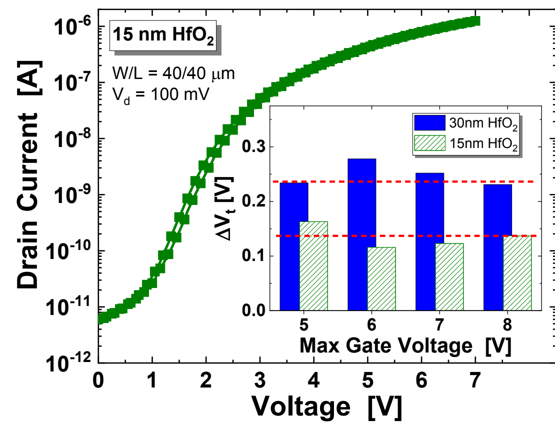

Fig. 4. Scaling effect of low temperature ALD HfO_2 on V_t instability (i.e., hysteresis, ΔV_t). 15 nm results in significantly reduced hysteresis versus a nominally 30 nm HfO_2 thickness (inset).

trapping in electrically active defects (Fig. 4). This mimics the typical trend seen in silicon-based HfO_2 scaling research previously observed [5]. On the other hand, Al_2O_3 ΔV_t values are comparable, irrespective of the thickness (Fig. 5).

With the hysteresis present in these, low temperature dielectrics, a forming gas anneal was applied to the previously measured devices (Fig. 6). The results indicate that the ΔV_t was drastically reduced, which suggests the electrically active traps are passivated in similar manner as typical Si semiconductor devices that experience an FGA.

B. Dual-Gate Molybdenum Disulfide Transistor Evaluation

Recently, our group has evaluated various process techniques that have helped enable top gate FET operation with low gate leakage [3, 6]. Figure 7 illustrates the impact that various treatments and anneals have had. In our evolution of arriving at our currently optimized top-gated MoS_2 FET, an ultra-violet ozone (UV-O_3) surface functionalization treatment [4] was needed to enable uniform sub-10 nm, pinhole-free high-k dielectric deposition (Fig. 2, TEM). This resulted in FETs with high I_{on}/I_{off} ratios, but V_t values that were quite negative and a I_{on} that appeared to be low, which means there could be significant positive charge in the HfO_2 film and possible

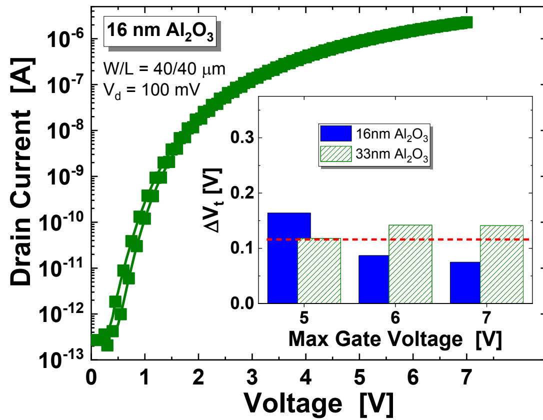

Fig. 5. Scaling effect of low temperature ALD Al_2O_3 on V_t instability (i.e., hysteresis, ΔV_t). Overall, reduced (30 nm) or comparable (15 nm) hysteresis is observed when compared to HfO_2 (Fig. 4).

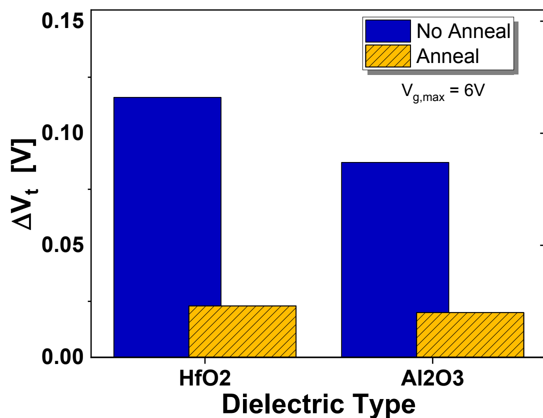

Fig. 6. Impact of forming gas anneal on 15 nm HfO_2 and Al_2O_3 ΔV_t values where the FGA noticeably passivates traps and reduces the hysteresis.

inability to completely modulate the electron channel of the FET (Fig. 7a). The cause is suspected to be the relatively low temperature required for deposition of the HfO_2 on the UV-O_3 treatment, and/or residual contamination on the transistor channel region as a result of the fabrication process. Therefore, we introduced an ultra-high vacuum (UHV) anneal to remove any residual contaminants, which exhibited much improved device characteristics (100 times higher I_{on} and mobility in Fig. 7b). We later introduced a FGA which passivated electron traps thereby shifting the V_t towards 0V, but appears to have impacted the "on" current (Fig. 7c). Further investigation is required to ascertain the reason for this impacted current.

Another one of our investigations involved the influence of the bottom gate dielectric on top-gate performance [refs] where the bottom gate was left floating while the top gate bias was swept. Here, the same ALD HfO_2 was deposited as the top gate dielectric for all three bottom dielectrics to ensure a systematic study of the bottom dielectric effect [7]. Fig. 8 shows that the Al_2O_3 provides a significant subthreshold slope improvement without sacrificing saturation current performance.

Our previous studies [3, 8] have shown that when HfO_2 is deposited on MoS_2 as the top gate dielectric layer, a 400°C forming gas anneal was needed to remove the positive charges in the HfO_2 layer. However, the post-annealed devices still

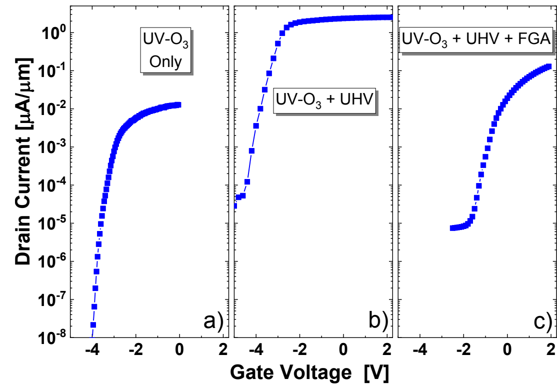

Fig. 7. Impact that various treatments and anneals on performance. a) Ultra-violet ozone (UV-O_3) surface functionalization treatment [4] was needed to enable uniform sub-10 nm, pinhole-free high-k dielectric deposition (Fig. 2, TEM), which resulted in high I_{on}/I_{off} ratios but low I_{ON} and V_t values that were quite negative, suggesting significant positive charge is present, b) Ultra-high vacuum (UHV) anneal removes any residual contaminants, which exhibited much improved device characteristics (100 times higher I_{on} and mobility) c) FGA helps passivate traps but appears to have impacted the "on" current.

may have large numbers of interface traps (D_{it}) and border traps (D_{bt}), which degrades the performance of the MoS_2 transistors [8]. However, the bottom gate Al_2O_3 dielectric enabled better top-gate performance. Fig. 9 illustrates the evaluation of a two terminal, Al_2O_3 bottom gate MOSCAP, which demonstrated much improved multi-frequency C-V characteristics with reduced frequency dispersion compared to our previous HfO_2 C-V behavior [8, 9]. Therefore, we have introduced transistor gate stacks with 3nm Al_2O_3 as the top-gate interfacial layer between HfO_2 and MoS_2, considering that the ALD Al_2O_3 potentially has better interface behavior on MoS_2, compared to HfO_2 only (Fig. 9) [7, 10].

Figure 10 - 11 shows the electrical characterization results for a MoS_2 transistor with $HfO_2/Al_2O_3/MoS_2$ as the top-gated stack. Without any annealing steps after the ALD and gate metal deposition, the transistor is able to be turned off, indicating significantly lower density of positive charges in the dielectric layer compare to HfO_2/MoS_2 [3]. The transistor has a peak field effect mobility of 9.2 $cm^2/V\cdot s$, with an I_{ON}/I_{OFF} ratio larger than 10^6. The capacitance – voltage (C-V) characterization exhibits frequency dispersion in both depletion and accumulation regions, indicating the existence of D_{it} and D_{bt}, respectively. However, the dispersion is much less than previously shown in the HfO_2/MoS_2 samples [8]. The D_{it} value, which is extracted by high-low frequency method, is in the range of 10^{11}-10^{12} $eV^{-1}cm^{-2}$, about an order lower than the device with HfO_2/MoS_2 post-annealing at 400°C. The Al_2O_3/MoS_2 demonstrates a better interface compared to HfO_2/MoS_2, by having a lower positive charge density, lower D_{it}, and higher mobility in the channel. However, the physical origins of the D_{it} and D_{bt} still need to be understood, and the interface needs to be further improved by reducing those traps.

IV. Summary

ZnO and MoS_2 transistors with relatively low temperature, atomic layer deposited HfO_2 and Al_2O_3 gate dielectrics were electrically characterized to assess the influence of the process on device performance. Results demonstrate that low temperature (≤ 200°C) gate dielectrics exhibit electrically

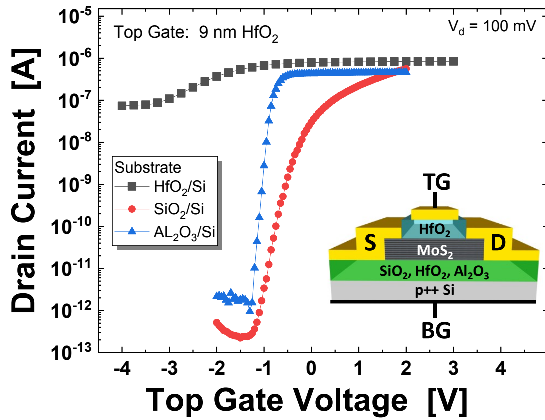

Fig. 8. Even without any backside bias, Al_2O_3 as the bottom-gate dielectric layer has a positive influence on HfO_2 top-gate FET performance — because the top-gate field effect mobility and subthreshold slope drastically improved when compared to SiO_2 or HfO_2 as back gate dielectric.

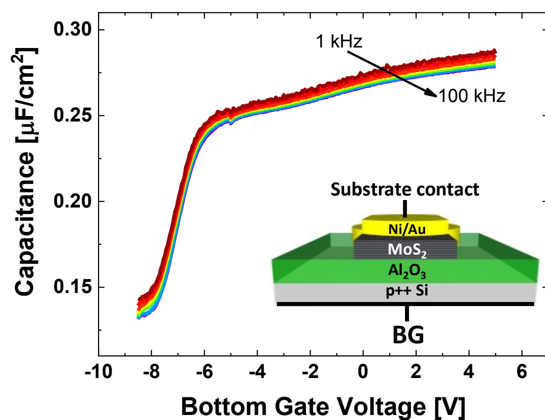

Fig. 9. C-V result of bottom-gated Al_2O_3 demonstrating much less frequency dispersion than our prior HfO_2 top-gate dielectric results [8, 9] .

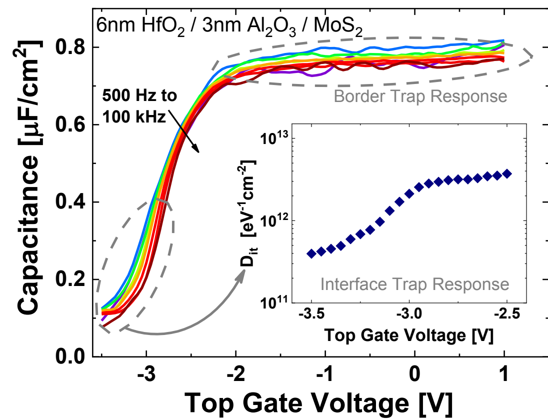

Fig. 10. Capacitance- voltage data from a top-gated MoS_2 transistor with HfO_2/Al_2O_3 as the dielectric layer showing frequency dispersion in both accumulation region and depletion region, indicating interface and border traps, respectively. Inset: D_{it} extracted from C-V data by high-low frequency method.

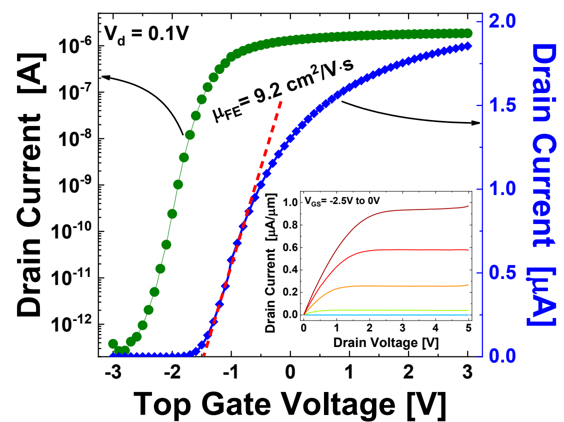

Fig. 11. Electrical characterization of a top-gated MoS_2 transistor with HfO_2/Al_2O_3 as the dielectric layer illustrating I_d-V_g curves on log and linear scales: V_T = -1.5V and the peak μ_{FE}=9.2 $cm^2/V{\cdot}s$. Inset: I_d-V_d results demonstrating linear I-V data due to ohmic-like source/drain contacts.

active defects, which create threshold voltage instability. For ZnO TFTs, the defects induced hysteresis in the I_d-V_g data. However, with dielectric scaling and/or forming gas annealing, the trap density was noticeably reduced. For MoS_2 top-gate FETs, a surface functionalization treatment in addition to different forms of annealing are required to reduce interface and border traps in order to obtain optimal device performance.

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