Positive Bias Instability in ZnO TFTs with Al_2O_3 Gate Dielectric

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***Abstract*— Positive bias instability stress (PBI) was done on ZnO thin-film transistors (TFTs) with Al_2O_3 deposition at 100ºC and 250ºC. The threshold voltage (V_T), transconductance (g_m), and subthreshold slope (SS) were monitored where the 100ºC samples demonstrated a "turn-around" phenomenon in the ΔV_T compared to the 250ºC samples. The 250ºC samples show consistent $+\Delta V_T$, suggesting a higher Al_2O_3 deposition temperature results in the absence of the defect responsible for the "turn-around" effect. Both sets also demonstrate negligible degradation in Δg_m and ΔSS – suggesting little to no influence on the V_T shift by interfacial state generation.**

***Index Terms*-- ZnO, TFTs, Al_2O_3, V_T, PBI**

I. Introduction

Large-area/flexible electronics may rely on oxide-based semiconductors that are desirable because of their compatibility with low-temperature fabrication required for large-area/flex-compatible technologies. ZnO is an oxide-based candidate to be used as an active layer in thin-film transistors (TFT) circuitry due to inexpensive processing and noteworthy electrical performance [1]–[3] and possible uses in flexible circuits [1]. For flex compatibility, deposition of high-k gate dielectrics at these low temperatures will be required as well.

With all the low-temperature processing, thin-film transistor reliability must be evaluated due to threshold voltage (V_T) instability experienced by TFTs with high-k dielectrics [4]–[6]. In this work, TFTs are constant voltage stressed while monitoring critical parameters to assess the reliability of ZnO-based TFTs.

II. Device and Stress Procedure Description

Zinc-oxide TFTs are fabricated using traditional photolithography to pattern staggered-bottom-gate and top-contacts, as previously reported[7], with the final device cross-section in Fig. 1. The devices are fabricated on a glass substrate with patterned 135 nm of indium tin oxide (ITO) to serve as the gate electrode. Then, a 15 nm Al_2O_3 gate dielectric is deposited by atomic layer deposition (ALD) at 100ºC or 250ºC followed by 45 nm of zinc oxide (ZnO) as the semiconductor channel deposited by pulsed laser deposition (PLD). A protection layer (parylene) is used prior to patterning the ZnO, and then a hard mask (parylene) is deposited to protect the TFTs from ambient conditions. Finally, the gate and source/drain vias are opened in order to deposit Al contact metal followed by patterning. Stress testing was performed by applying stress voltages of either 5.5 V, 5.75 V, or 6 V to the gate only, with intermittent I_D-V_G sense measurements.

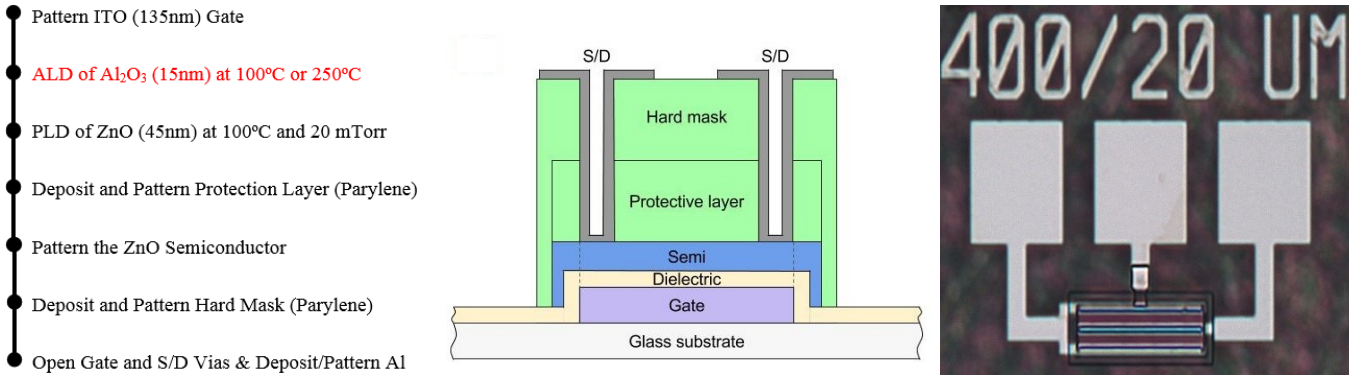

Figure 1. (left) Process flow for ZnO TFTs with Al_2O_3, (middle) cross-section schematic of the TFT structure, and (right) plan-view of the TFT structure.

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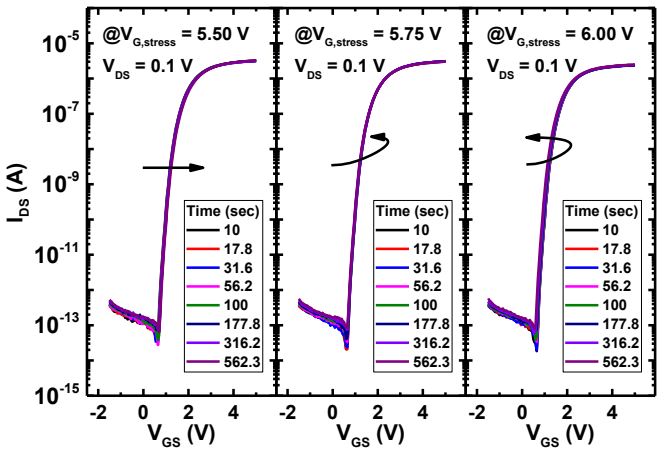

Figure 2. Example I_{DS}-V_{GS} of TFTs with 100°C Al_2O_3 at 3 different stress biases. The threshold voltage (V_T) shift appears to be minor with no apparent degradation in the subthreshold slope (SS); however, a "turn-around" effect is observed during stress.

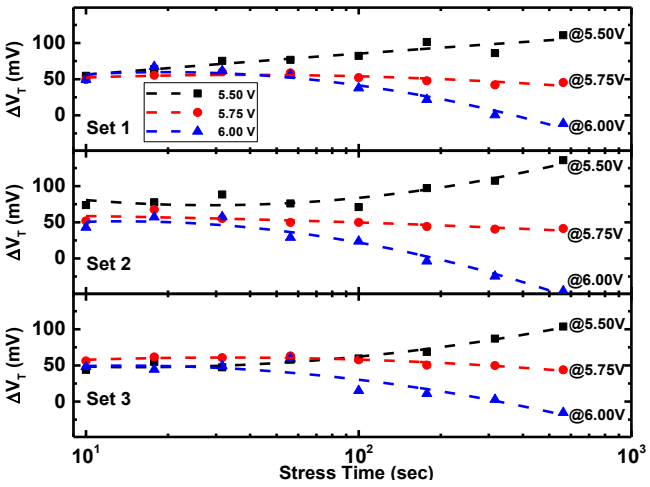

Figure 3.The ΔV_T vs stress time for different sets of TFTs with 100°C Al_2O_3 at 3 different stress biases. The fitted lines show the ΔV_T demonstrating the "turn-around" effect shown in Fig. 2.

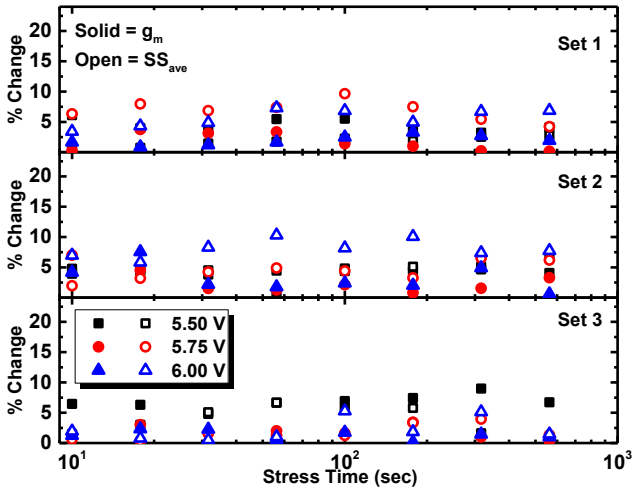

Figure 4. The % change in maximum transconductance (g_m) and average subthreshold swing (SS_{ave}) for TFTs with 100°C Al_2O_3 suggests that there is little to no interface state generation contributing to ΔV_T during stress.

III. Data/Results and Discussion

Low-temperature high-k dielectrics are essential for compatibility with large-area/flex electronics. A comparison between a 100ºC and a more robust 250ºC dielectric is needed for understanding the effect of dielectric deposition temperature on V_T instability. To demonstrate consistent trends across devices, multiple TFTs were measured for each deposition temperature at 3 different stress voltages. V_T is extracted using linear extrapolation of I_D-V_G at the point of maximum transconductance. All devices had dimension of W/L = 400/20 µm, as shown in the plan-view picture of a device in Fig. 1.

A. Al_2O_3 Deposited at 100ºC

Fig. 2 illustrates the evolution of I_D-V_G degradation for devices with 100ºC Al_2O_3 at the three different stress bias conditions. One can observe a minor V_T shift with little to no degradation in either g_m or SS. Extraction of the ΔV_T across all three sets of TFTs in Fig. 3 yields a more comprehensive understanding of the behavior of the V_T with stress time. At a stress voltage of 5.5 V, the V_T monotonically increases, but at voltages of 5.75 V and 6 V, an initial positive V_T shift is observed followed by a negative V_T shift. This "turn-around" phenomenon has been observed in Hf-based dielectrics [8], [9] as well more recently in IGZO TFTs [10]–[12]. This effect is exacerbated at higher voltages, consistent with previous reports [13]. This suggests that for TFTs with 100ºC Al_2O_3, the defect mechanism responsible for the negative ΔV_T is dominant at higher voltages compared to the defect mechanism responsible for positive ΔV_T observed at the lower voltage. This could be due to the lower temperature deposition of 100ºC, where an additional defect may be present, which may be responsible for "turn-around" effect thereby enabling electron de-trapping to occur at the same time as electron trapping. Previous temperature dependent studies suggest that higher residual hydrogen content (>10 at.%) in low temperature Al_2O_3 may be the culprit [14]. Fig. 4 shows the negligible % change in the g_m and average SS (extracted using an exponential fit from 10^{-11} A to 10^{-9} A) for all sets with 100ºC Al_2O_3, suggesting little to no interface state generation.

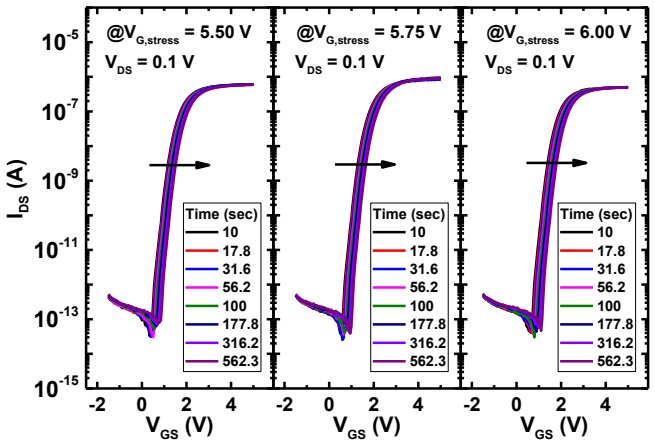

Figure 5. Example I_{DS}-V_{GS} of TFTs with 250ºC Al_2O_3 at 3 different stress biases. The threshold voltage (V_T) shift is significant in this dielectric with no apparent degradation in the subthreshold slope (SS). No "turn-around" effect is present during stress.

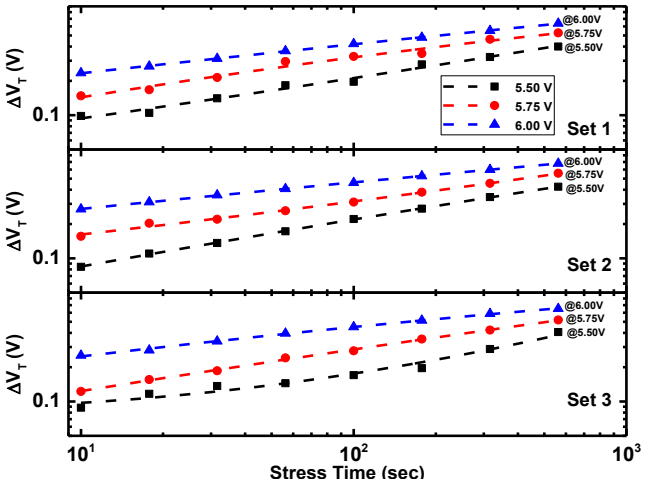

Figure 6. The ΔV_T vs stress time for different sets of TFTs with 250ºC Al_2O_3 at 3 different stress biases. The fitted lines show trends consistent with traditional PBTI in MG/HK nMOS degradation.

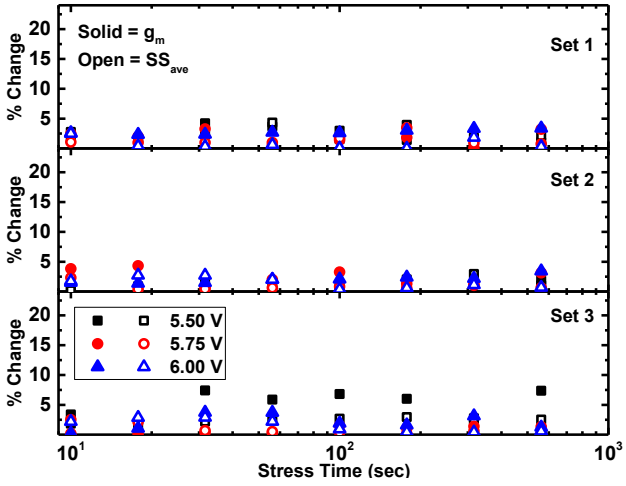

Figure 7.The % change in g_m and SS_{ave} for TFTs with 250ºC Al_2O_3 suggests that there is little to no interface state generation contributing to ΔV_T, similar to the 100ºC Al_2O_3 samples.

B. *Al_2O_3 Deposited at 250ºC*

The Fig. 5 demonstrates the evolution of the I_D-V_G for devices with 250ºC Al_2O_3 at three different stress conditions. One can observe a more prominent V_T shift, compared to the 100ºC samples, with little to no degradation in either g_m or SS. The extracted ΔV_T with stress in Fig. 6 shows monotonically increasing V_T across all sets, consistent with the trends observed for typical PBI in MG/HK NMOS, suggesting an electron trapping mechanism. Fig. 7 shows negligible % change in g_m and SS_{ave} for the 250ºC samples, similar to the 100ºC samples in Fig. 4, suggesting little to no interface state generation contributing to the V_T shift.

C. *100ºC vs. 250ºC Al_2O_3*

At first glance, comparing the I_D-V_G measurements in Fig. 2 (100ºC) with Fig. 5 (250ºC), as well as Fig. 8, the low-temperature Al_2O_3 appears to have smaller V_T shifts than the 250ºC samples. Intuitively, the high-temperature Al_2O_3 should have less V_T degradation, not more. This suggests that the two different defect mechanisms attributed to the $+\Delta V_T$ and $-\Delta V_T$ in the 100ºC samples are competing, leading a smaller net ΔV_T; whereas, the 250ºC samples only have contribution from the defect mechanism attributed to the $+\Delta V_T$, as illustrated in Fig. 9.

In an effort to comprehend why there appears to be this turn around effect, further analysis was conducted. As mentioned before, higher residual hydrogen content may be incorporated in low temperature Al_2O_3, where the at % of hydrogen present in low temperature Al_2O_3 decreases significantly with increasing temperature [14]. This would further indicate that the higher concentration of hydrogen in 100ºC Al_2O_3 may be partially responsible for the observed "turn-around" effect, whereas at 250ºC, the reduction in hydrogen content may not contribute significantly to the ΔV_T. Furthermore, after device fabrication and stress measurements results, the "turn-around" effect prompted the investigation of the elemental composition of Al_2O_3 thin films in order to ascertain if there was any other potential reason for the $-\Delta V_T$. The XPS spectra of the Al_2O_3 used in this work in Fig. 10 show Hf content in the 100ºC Al_2O_3, as well as carbon. Yet, the Hf is not present in the 250ºC Al_2O_3 sample, suggesting the Hf may be a contributing factor to the "turn-around" effect. There is also a reduction in carbon in the 250ºC Al_2O_3, as has been shown in previous reports [14]. Upon further review, the 100ºC Al_2O_3 deposition was done first, then the 250ºC deposition. Thus, prior contamination from a previous

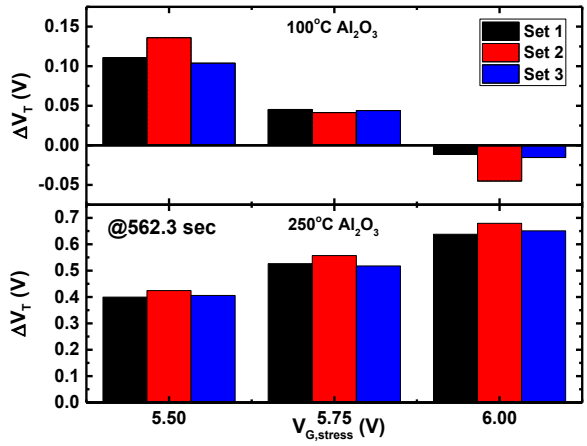

Figure 8. Comparison of ΔV_T at a fixed time between the TFTs with 100ºC Al_2O_3 and 250ºC Al_2O_3. Results demonstrate lower ΔV_T for the 100ºC samples possibly caused by the proposed competing mechanisms of simultaneous electron trapping and de-trapping within stress duration.

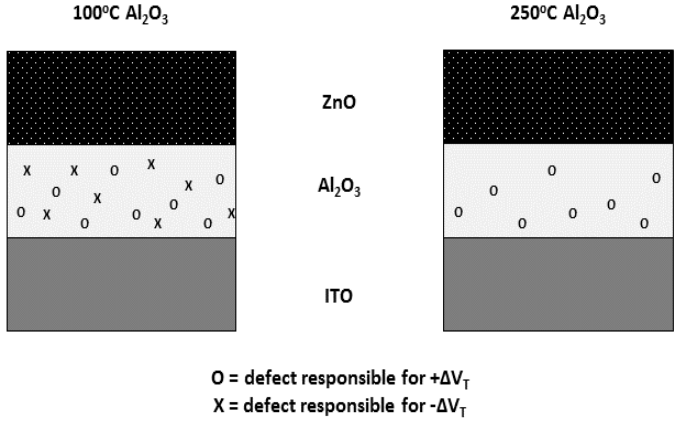

Figure 9. The schematic cross-sections of the gate stack for ZnO TFTs with different Al_2O_3 deposition temperature, illustrating an additional, plausible defect present away from the Al_2O_3/ZnO interface the defect mechanisms responsible for $+\Delta V_T$ and $-\Delta V_T$ in the 100ºC Al_2O_3 samples.

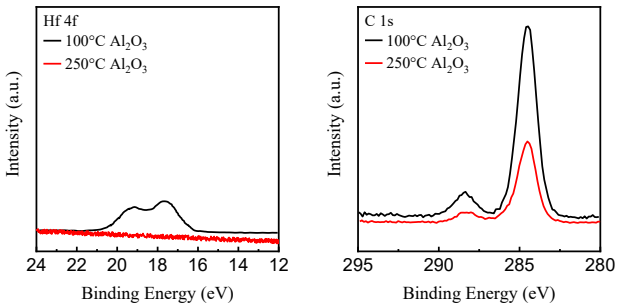

Figure 10. Comparison of XPS spectra of different temperature Al_2O_3 with (left) Hf 4f and (right) C 1s. These spectra show Hf content in oxide state, not metallic state, in 100ºC Al_2O_3 as well as C content. For the 250ºC Al_2O_3, the Hf is below the limit of detection and the C is still present but at a lower concentration.

HfO_2 deposition provided the residual Hf detected in the 100ºC Al_2O_3.

Another future work would involve the deconvolution of the exact defect responsible, whether it be the hydrogen or the hafnium or both, and the removal of the defect attributed to $-\Delta V_T$ to neutralize the "turn-around" effect in order to obtain a better comparison between the 100ºC and 250ºC samples.

IV. Conclusions

To study the impact of low Al_2O_3 deposition temperature on V_T instability, ZnO TFTs were subjected to gate stress bias. For devices with Al_2O_3 deposited at 100ºC, the V_T degradation in the interspersed I_D-V_G measurements appears minimal. Extraction of ΔV_T for multiple sets of devices demonstrates a "turn-around" phenomenon in samples with 100ºC Al_2O_3, which is attributed to two competing defect mechanisms in Al_2O_3 responsible for the $+V_T$ and $-V_T$ shifts. Compared to the 100ºC samples, the samples with 250ºC Al_2O_3 demonstrate monotonically increasing V_T with stress time and voltage, consistent with trends observed for more traditional PBI in MG/HK nMOS. Both sets of samples show little to no degradation in g_m and SS_{ave}, suggesting that interface state generation is not a major contributor to the V_T instability.

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