Understanding the Effects of Low-Temperature Passivation and Annealing on ZnO TFTs Test Structures

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Abstract—**Back-gate ZnO TFTs – with and without top-side passivation – were fabricated and electrically characterized. Passivation layers consisting of HfO_2, Al_2O_3, and Parylene were introduced to study their impact on the TFT performance. Annealing was done to improve the electrical characteristics of passivated devices by neutralizing the initial charge introduced as a result of the low-temperature passivation. Low-temperature annealing combined with an Al_2O_3 passivation layer demonstrates an I-V response comparable to ZnO TFTs without any passivation layer, indicating the viability of Al_2O_3 as a good candidate for passivating ZnO TFTs.**

Keywords—ZnO, TFT, Al_2O_3, HfO_2, passivation, annealing

I. INTRODUCTION

Large-area/flexible electronics may need to rely on oxide-based semiconductors due to their compatibility with low-temperature fabrication, which is required for large-area/flex-compatible technologies. ZnO is an oxide-based candidate that can be used as the active semiconducting layer in thin-film transistor (TFT) circuits due to its compatibility with low-cost processing and exceptional electrical performance [1]–[3], as well as its potential uses in flexible circuits [1]. Thus, having TFT test structures that lend themselves to readily evaluate fundamental device operation for its intrinsic properties – rather than have these properties impacted by the test structure and/or fabrication process – is imperative. Furthermore, for flex compatibility, passivation of the ZnO using an insulating thin film deposited at low temperatures will be required as well.

Therefore, the impact of the low-temperature passivation layer and annealing on the electrical performance of the TFT's semiconducting layer (e.g., ZnO) must be evaluated due to the introduction of possible insulator charges such as those found in high-k dielectrics [4]–[7]. In this work, TFTs are passivated with HfO_2, Al_2O_3, and parylene to assess the impact on the ZnO TFT performance. Furthermore, low-temperature annealing is used to neutralize the oxide charge to achieve device characteristics comparable to those without any passivation layer measured immediately after fabrication.

II. FABRICATION & CHARACTERIZATION

ZnO TFTs are fabricated using a common back-gate where only the S/D and the semiconductor (ZnO) are patterned. A substrate consisting of ITO (135 nm) on glass is prepared and cleaned for atomic layer deposition (ALD) of 15 nm of Al_2O_3 at 100ºC as the gate dielectric. This is followed by pulsed laser deposition (PLD) of 45 nm of ZnO at 100ºC. Aluminum (100nm) S/D contacts are patterned by lift-off, followed by ZnO patterning (see Fig. 1). This test structure allows for understanding of the impact passivation has on thin-film materials with minimal lithography and patterning, before implementation in more sophisticated TFT structures [8]. Finally, the sample is cut into 4 pieces, with 3 of them passivated by HfO_2 (10 nm, 100ºC), Al_2O_3 (10 nm, 100ºC), and parylene (50 nm). All 4 sets of devices were characterized using a Keithley 4200A semiconductor characterization system (SCS), with annealing done at 150ºC and 250ºC C for 1 hour in air.

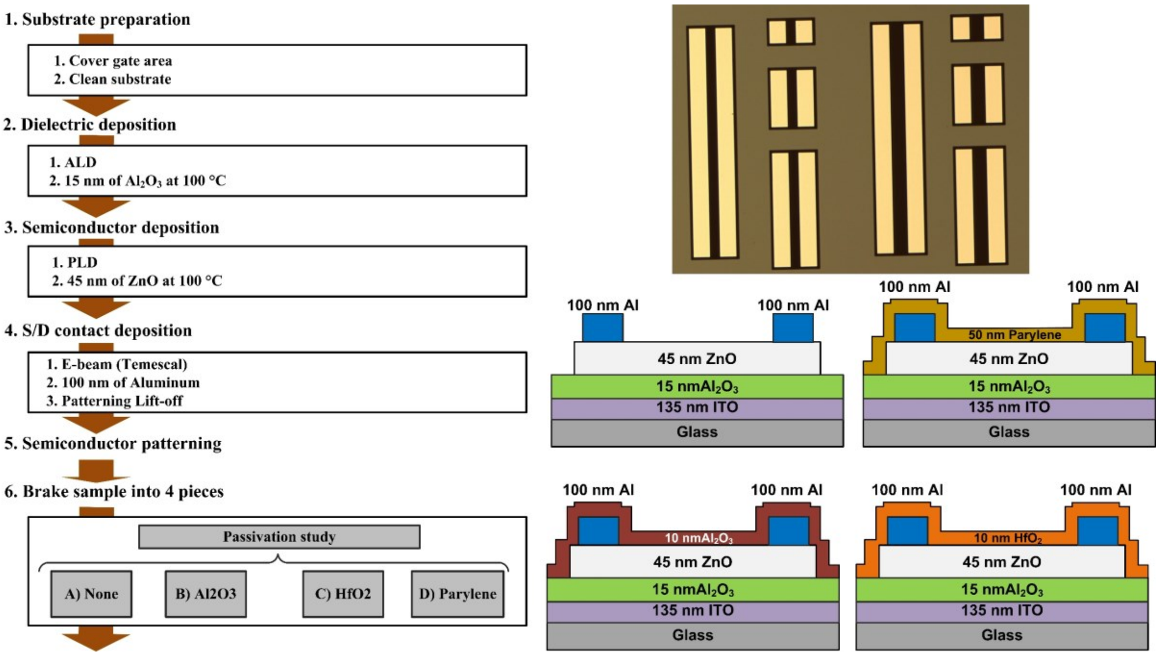

Fig. 1. Process flow, device images, and cross-sections.

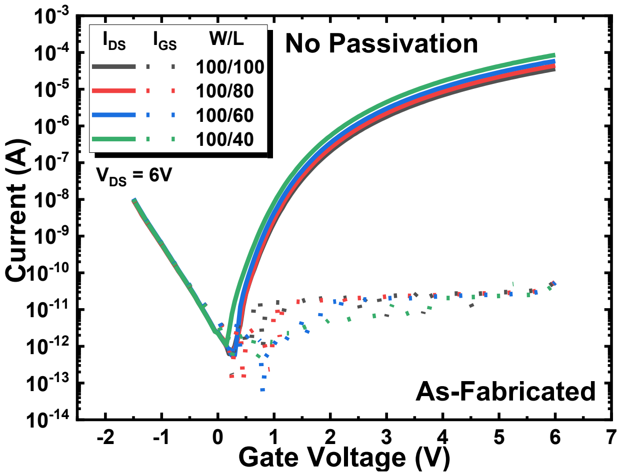

Fig. 2. The I_{DS}-V_{GS} of 4 different dimensions of ZnO TFTs without any passivation and annealing, indicating an I_{ON}/I_{OFF} of 10^8, SS of 165 mV/dec, and V_T of 2.56 V. Dotted lines represent gate current (I_{GS}).

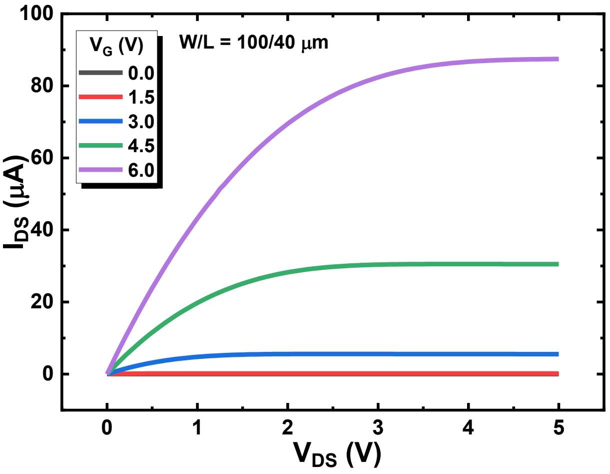

Fig. 3. The I_{DS}-V_{DS} of a ZnO TFT without any passivation and annealing.

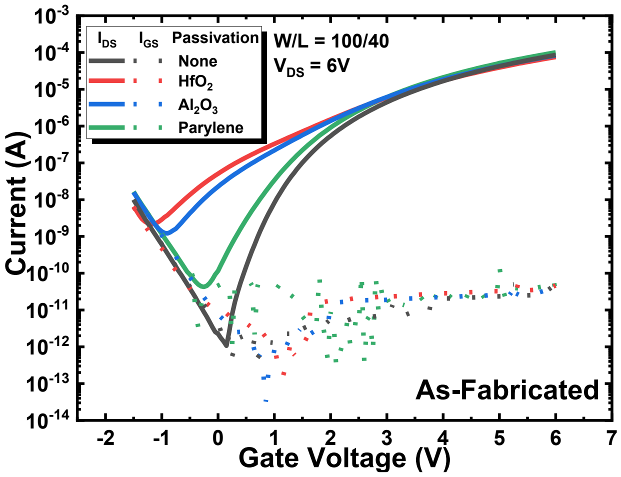

Fig. 4. The I_{DS}-V_{GS} of as-fabricated TFTs comparing the I-V response of device without passivation to those passivated with HfO_2, Al_2O_3, and parylene. The $-V_T$ shift suggests the introduction of positive charge at the top ZnO-passivation layer interface, with HfO_2 demonstrating the largest shift. Dotted lines represent gate current (I_{GS}).

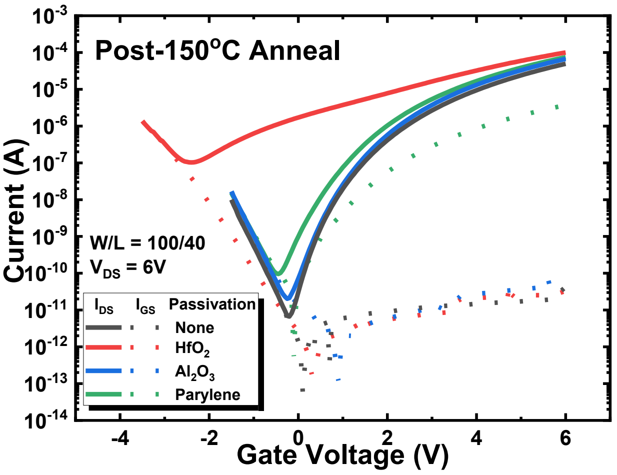

Fig. 5. The I_{DS}-V_{GS} of TFTs post-150°C annealing comparing the I-V response of device without passivation to those passivated with HfO_2, Al_2O_3, and parylene. The $+V_T$ shift of device with Al_2O_3 passivation layer suggests elimination of positive oxide charge while the further $-V_T$ of HfO_2 suggests degradation. Dotted lines represent gate current (I_{GS}).

III. RESULTS & DISCUSSION

Low-temperature passivation is needed to prevent degradation of devices from the ambient for large-area/flex-electronics. Parylene has been used previously as a passivation layer [8] and is compared in this study along with the high-k passivated devices. Fig. 2 shows the I_{DS}-V_{GS} observed for devices without any passivation, demonstrating high I_{ON}/I_{OFF} of 10^8, subthreshold swing (SS) of 165 mV/dec, and a threshold voltage (V_T) of 2.56 V. The I_{DS}-V_{DS}, observed in Fig. 3, demonstrates typical output characteristics observed for all devices, with and without passivation.

A. Passivation with Al_2O_3, HfO_2, and Parylene

Fig. 4 is a comparison of as-fabricated ZnO TFTs, comparing devices without a passivation layer with those passivated with HfO_2, Al_2O_3, and parylene, which shows a negative V_T shift for all passivated devices. There is also an increase in I_{OFF}, but it appears to be as a result of the high-gate leakage observed at negative gate voltages. A $-V_T$ shift from HfO_2 and Al_2O_3 passivation suggests an introduction of positive oxide charge, often observed in as-deposited high-k dielectrics [9]–[11]. Post-deposition annealing (PDA) has been used to alter oxide charge density in high-k dielectrics [12], [13], but typically at high temperatures (>300°C) beyond what would be compatible with large-area/flexible-electronics. Before annealing, each set of devices were cut into 2 pieces, allowing for one group to be annealed at 150°C and the other at 250°C, for comparison.

B. Post-150°C Anneal

Fig. 5 is the I_{DS}-V_{GS} comparison of passivated and non-passivated devices post 150°C annealing. The HfO_2 passivated devices show a $-V_T$ shift of 2 V post-150°C annealing, suggesting a significant introduction of more positive oxide charge, while the Al_2O_3 passivated devices show a $+V_T$, suggesting a reduction in positive oxide charge [14]–[16]. This indicates that a 150°C anneal is detrimental for the HfO_2 passivation layer but quite beneficial for the Al_2O_3 passivation layer. Furthermore, both the non-passivated and parylene passivated devices demonstrates a minor V_T shift compared to the high-k dielectrics, suggesting changes in the ZnO layer itself.

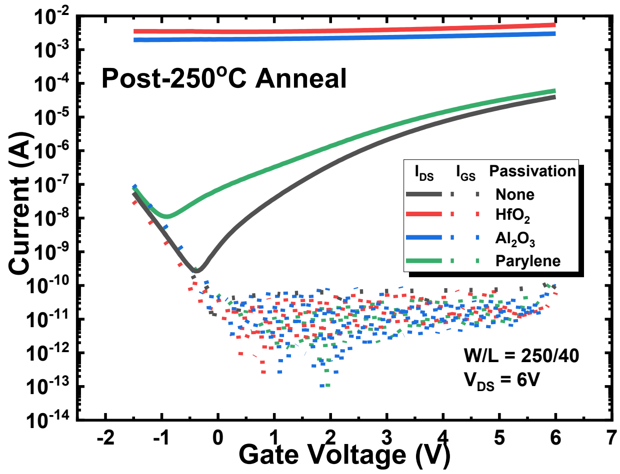

Fig. 6. The I_{DS}-V_{GS} of TFTs post-250°C annealing comparing the I-V response of device without passivation to those passivated with HfO_2, Al_2O_3, and parylene. The severe degradation for devices with HfO_2 and Al_2O_3 passivation layers suggests that the annealing temperature is too aggressive. Dotted lines represent gate current (I_{GS}).

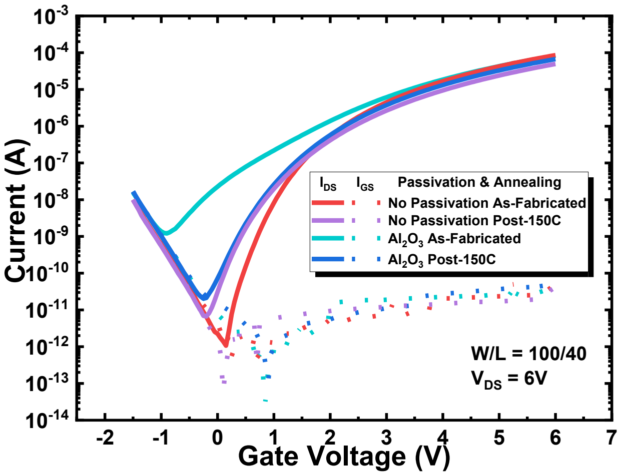

Fig. 7. The I_{DS}-V_{GS} of TFTs comparing the as-fabricated and post-150°C annealing I-V response of devices without passivation layer and those with Al_2O_3. The post-150°C comparison indicates that the Al_2O_3 passivation with a low-temperature anneal can achieve device behavior similar to devices without passivation.

TABLE I. Comparison of ZnO TFTs for those with and without a passivation layer as well as the behavior of critical device parameters post-150°C annealing and 250°C annealing. These results suggest that Al_2O_3 passivation with a 150°C anneal is able to obtain device characteristics that are comparable to those without any passivation.

	As-Fabricated			**Post-150C Annealing**			**Post-250C Annealing**		
	I_{ON}/I_{OFF}	**SS (mV/dec)**	**V_T (V)**	**I_{ON}/I_{OFF}**	**SS (mV/dec)**	**V_T (V)**	**I_{ON}/I_{OFF}**	**SS (mV/dec)**	**V_T (V)**
No Pass.	**10^8**	**163**	**2.56**	**10^7**	**250**	**2.60**	**10^6**	**451**	**2.66**
HfO_2	**10^5**	**715**	**2.33**	**10^3**	**1498**	**0.35**	**-**	**-**	**-**
Al_2O_3	**10^5**	**600**	**2.36**	**10^7**	**320**	**2.55**	**-**	**-**	**-**
Parylene	**10^6**	**338**	**2.44**	**10^6**	**377**	**2.33**	**10^4**	**971**	**2.31**

C. Post-250°C Anneal

Fig. 6 is the I_{DS}-V_{GS} comparison of passivated and non-passivated devices post 250°C annealing. Both HfO_2 and Al_2O_3 show severe degradation in the I-V, with little to no gate modulation. Although the non-passivated and parylene passivated devices show minor V_T shifts, they are nowhere near the degradation observed in the high-k dielectric passivated devices. This suggests that the bulk ZnO is not the main driving factor in the degradation due to the 250°C annealing, but more likely the ZnO/high-k dielectric interface. Compared to the 150°C anneal, the 250°C anneal appears to be too aggressive for high-k passivated ZnO TFTs.

D. Al_2O_3 Passivation + 150°C Annealing

Fig. 7 compares the I_{DS}-V_{GS} pre- and post-150°C anneal for non-passivated and Al_2O_3 passivated devices, clearly indicating that the combination of Al_2O_3 passivation and a 150°C anneal can preserve the I-V characteristics similar to the non-passivated device post-150°C annealing.

A final comparison between the major device parameters of as-fabricated, post-150°C annealing, and post-250°C annealing can be seen in Table I, indicating the best post-passivation and post-annealing characteristics are achieved with Al_2O_3 passivation layer and a 150°C anneal. Further investigations on thinner (sub-10 nm) Al_2O_3 passivation layers is needed to further enhance ZnO TFT passivation using a low-temperature process.

IV. SUMMARY

Large area/flex compatibility requires a low-temperatures process for passivation of ZnO TFTs. Deposition of HfO_2 or Al_2O_3 at 100°C as a passivation layer introduces positive oxide charge, but a post-deposition anneal can be used to neutralize the oxide charge. While a 250°C anneal severely degrades device performance, a 150°C anneal shows promise, particularly for an Al_2O_3 passivation layer, where a $+V_T$ indicates a major reduction in oxide charge. This work provides a low-temperature, high-k dielectric passivation and annealing process for ZnO TFTs that is compatible with low-temperature processing needed for large-area/flexible electronics.

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