A Fully-integrated LC-Oscillator Based Buck Regulator with Autonomous Resonant Switching for Low-Power Applications

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***Abstract*— In this paper, a fully integrated, *LC*-oscillator based buck regulator is presented for low power applications. The proposed design uses a self-resonator as both high-speed clock source and a resonant switch driver for the regulator, which not only achieves significantly improved energy efficiency at 2GHz switching frequency but also delivered a high-quality clock source eliminating requirement of the external high-speed clocks. Measurement on a 65nm testchip shows a wide tuning range from 0.35V to 0.82V with an input voltage 1.1V. The proposed design achieves a peak efficiency of 70.3% and an autonomous clock-less operation. The regulator core area is only 0.079mm^2.**

Keywords*— *Buck regulator, fully integrated, input-clock free, resonant switching, low power applications.

I. INTRODUCTION

Energy-efficient near-threshold computing has been proposed to increase energy efficiency across a wide range of applications [1]. Recent developments on low power wearable electronics and IoT devices bring new design requirements to power regulators. For example, achieving high power efficiency performance at low output voltages/current is one of the keys for near or subthreshold operation. The conventional buck regulator design normally utilizes large off-chip inductors (>1uH) with slow switching frequency (<5MHz) [2-3]. The fully integrated regulator solutions using on-chip inductors are more suitable for integration with the microprocessors and attracts more attentions recently [4-7]. However, most of the previous fully-integrated buck regulators are designed for high output power with hundreds of milliamps output current and show poor efficiency at low voltage regime, e.g. only 40% at 0.5V [5]. For near-threshold computing, the nominal operation voltage is normally around 0.4-0.6V, with only a few to tens of milliamps load current [1]. Therefore, the design strategy for buck regulator needs to be adjusted to optimize the regulator's performance at low power low voltage conditions.

For a conventional buck regulator, its step-down voltage ΔV is determined by the inductance value L and the changing rate of inductor current di_L/dt, as expressed by the equation (1):

$$\Delta V = L \cdot \frac{di_L}{dt} = L \cdot \frac{\Delta i_L}{D} \cdot f_{sw} \qquad (1)$$

in which D is the duty cycle of the switching clock and f_{sw} is the regulator switching frequency. Δi_L is the current ripple of inductor L. For the fully-integrated buck regulator designs, the small on-chip inductance value L causes the increasing of the inductor current ripple Δi_L, which potentially leads to reverse current and severely degraded efficiency assuming simple continuous-conduction mode (CCM) operation is maintained. As a result, to maintain small inductor current ripple Δi_L and small size of on-chip inductor L, the switching frequency f_{sw} of fully integrated buck regulator has to been typically pushed much higher to 200~500MHz comparing with the off-chip counterpart [5-6]. For low power applications where the current is in the order of only milliamp to tens of milliamp, the switching frequency has been further increased to 2GHz to maintain a small size of the inductor [7].

Fig.1 shows that inductance value and power loss trend with the scaling of switching frequency f_{sw}. As shown in Fig. 1(a), the on-chip inductance value, which translates to the inductor area, scales inversely proportional with switching frequency. Fig. 1(b) shows the simulated power loss components, i.e. inductor, clock, power switches as a function of switching frequency. The power loss from inductor, in fact, drops with higher switching frequency due to the reduced peak-to-peak ripple Δi_L at higher switching frequency, which leads to 2-4X less inductor loss at 2GHz compared with 500MHz. Fig. 1(c) and (d) shows the current and voltage ripple at switching frequency of 500MHz and 2GHz. The output voltage ripple is improved with higher frequency, which also leads to the benefits of reduction of required output decoupling capacitors (decap), e.g. from a few of *nF* [4-6] to 120pF in this work.

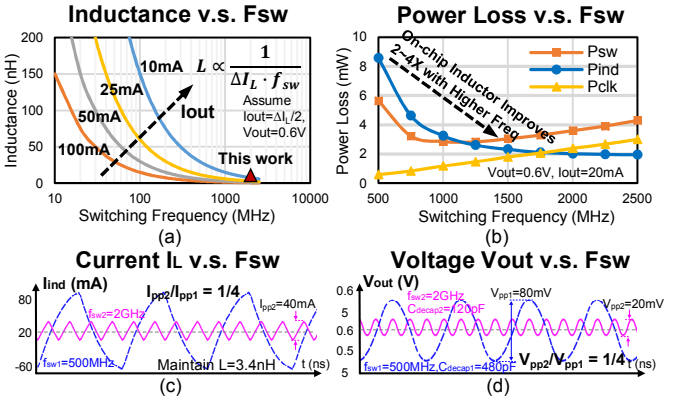


Fig. 1. (a) Inductance value, (b) power loss breakdown, (c) inductor current, and (d) output voltage ripples scaling with switching frequency.

As shown in Fig. 2, the conventional buck regulator normally needs two clocks, in which one provide the switching frequency for the power switches and the other one provides the loop sampling frequency. These two frequencies can be designed to be same frequency value or may choose two

different frequency values [4-5]. In the conventional buck regulator operating with slow switching frequency, i.e. a few MHz, the clock source power is negligible. However, for fully integrated buck regulator running at 500MHz or even higher frequency, the power consumption from the clock sources could become significant. Unfortunately, none of the previous work addresses the issue of the generation of clock source [5-7].

In this work, we proposed a *LC*-oscillator based buck regulator design, in which the oscillator serves both as the switching clock source and the power switch gate driver. A resonant switching operation is naturally formed between the *LC* oscillator and the gate capacitance of power switches, which eliminating the requirement of resonant drivers [7]. Our simulation shows a 7% to 20% efficiency improvement is observed due to the use of resonant switching, especially at low voltages, e.g. 0.3V~0.5V, where the clock power loss dominates, as shown in Fig. 2(b). In addition, the loop frequency is provided by a divided clock from the *LC* oscillator. As a result, no external clock generator is needed.

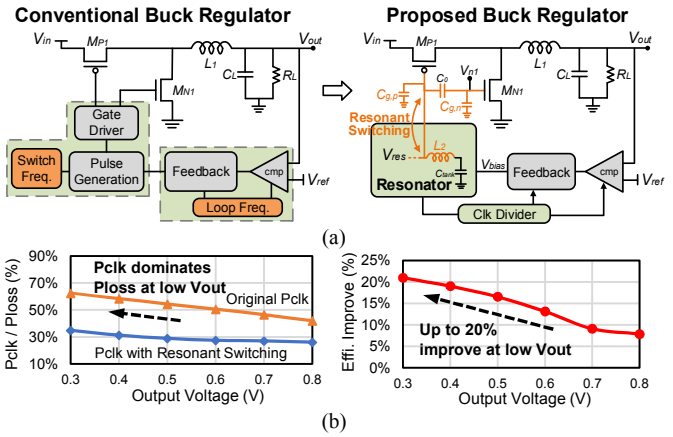


Fig. 2. (a) Concept of the buck regulator with autonomous switching. (b) Power saving benefit from the resonant swithcing.

II. Proposed Buck Regulator Design

A. Overview

Fig.3 shows the overview of the proposed buck regulator. The conventional multi-stage non-overlapping PMOS/NMOS switch drivers are replaced by a *LC* oscillator topology self-resonator, which naturally creates a resonance between the inductor L_2 and capacitance $C_{g,sw}$ from the gates of power switches M_{P1} and M_{N1}. The resonant frequency is determined by the total capacitance of $C_{g,sw}$ and a tunable capacitor C_{tune} with the oscillator inductor L_2. In this work, the self-resonator oscillation frequency, i.e. the switch frequency, is set around 2GHz, which is determined by the size limit of inductors and the low output current according to equation (1).

A resonant switching operation is formed by the self-resonator, which saves the switching clock power. When the power switches are fully turned on/off, the energy within the gate capacitance $C_{g,p}$ and $C_{g,n}$ is gradually charged or discharged into the oscillator inductor L_2. During the transition of the power switch, the stored energy is released to assist the power switch transitions. To utilize the resonant switching, the gate of the power switches M_{P1} and M_{N1} are jointly switched by the self-resonator. A coupling capacitor C_1 is added between the PMOS/NMOS gate with a high impedance DC biasing voltage V_b to shift the switching voltage of NMOS and suppress the short-circuit current. To control output voltages, a duty cycle distortion is deliberately introduced through the feedback control of the Gm transistor in the self-resonator. Feedback is realized through hysteresis comparators with reference voltages and converted into Gm tuning voltage through a R-2R DAC. The oscillation frequency is tunable from 1.6GHz to 2.4GHz through tunable capacitors C_{tune}, and is divided down by 64 times to provide baseband clock for feedback control. Therefore, there is no external clock generator required.

In the proposed design, two on-chip inductors are utilized, which is the L_1 of 3.4nH for the buck regulator and L_2 of 11.6nH for the *LC* self-resonator. The inductor L_1 is designed with wide width and less number of turns to reduce the conduction resistance. The current that flow through inductor L_2 is the charging and discharging current for the gate capacitance of power switch $C_{g,sw}$, which is much smaller than the load current. Therefore, there is less stringent Q requirement for the inductor L_2 leading to larger inductance value but similar size as L_1. Programmable static on-chip resistance load is utilized for the efficiency measurement, with an on-chip scan chain control the testing configurations.

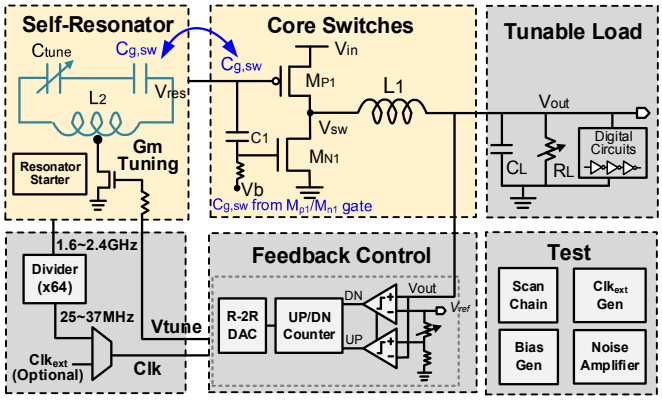


Fig. 3. Overview of the proposed buck regulator design.

B. Self-Resonantor Design

Fig. 4 shows the detailed implementation of the *LC* oscillator based self-resonator. The oscillation tank is formed from an inductor and the capacitance contributed from gate capacitance $C_{g,sw}$ of both power switches, M_{P1} and M_{N1} and additional tunable capacitors C_{tune}.

There are three special design techniques used to control duty cycle and boost slew rate of oscillation. (1) Different from the conventional self-biased inverter for generating negative resistance for oscillation, as shown in Fig. 4, the proposed design uses a separate gate bias V_{tune} for Gm transistor enabling tuning of duty cycle. Simulation shows a duty cycle from 32%~76% can be introduced at the output node of the self-resonator leading a wide range of output voltage. (2) Coupling capacitor C_3 couples the oscillation node V_{OSC} to PMOS driver M_{P2} to boost swing at V_{RES} signal and improve its slew rate. (3) Coupling capacitor C_4 is utilized to couple the square wave V_{SW} to M_{P2} to further boost the slew rate of V_{RES}. As a result, a rail-to-rail swing at the self-resonator output V_{RES} is achieved and the slew rate is improved, which leading to a significant reduction of short-circuit current and power switch loss reduction.

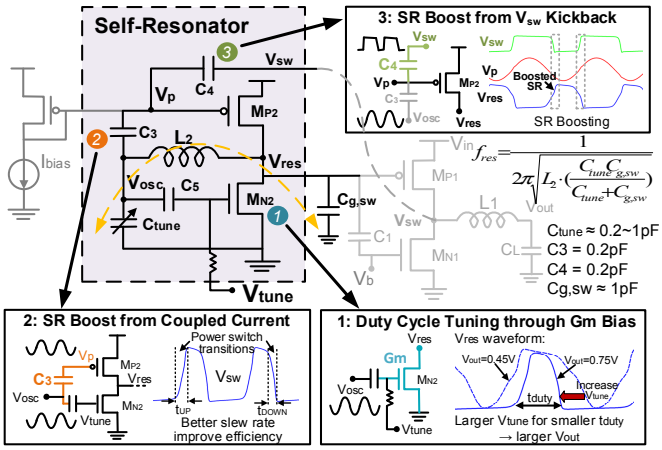


Fig. 4. Design of the self-resonator integrated with power switches and the description of duty cycle control and slew rate enhancement.

The special bias condition used here does not guarantee startup condition for the oscillation. Hence, a special startup sequence with kick-start is used to establish the oscillation, as shown in Fig. 5. Before the oscillation, a startup PMOS header is enabled to provide a constant current $i_{startup}$. The Gm transistor is pre-biased by voltage V_{tune} into the saturation region before a kick-start is applied. After completing all these initialization setup, the $V_{startup}$ signal is released and kick the oscillation. After the oscillation is built-up, the feedback control loop is enabled to generate desired voltages through duty cycle control. As the measurement waveform shown in Fig. 5, the self-resonant startup takes about 25ns to generate a 0.55V output voltage from 0V.

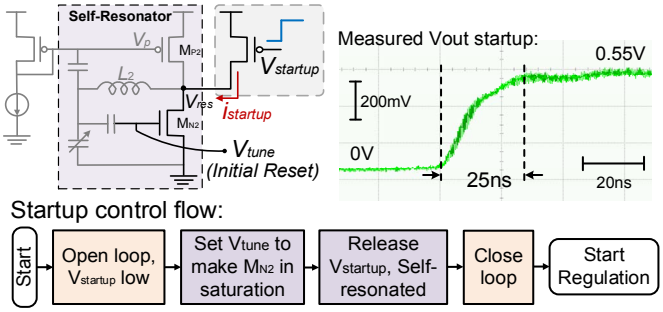


Fig. 5. The startup control flow for the self-resonator.

C. EM Simulations for Inductor Floorplan

The electromagnetic (EM) analysis and mutual coupling simulations are conducted with the actual inductor sizes and distance. Fig. 6 shows the consideration of inductor placement. As the resonant tank is placed right next to the main power inductor and consumes much less current, extra care is given to avoid pulling or glitches to the oscillator from the magnetic field of the main inductor. The effective inductance of L_1 and L_2 can derived as equation (2) and (3).

$$L_{eff,1} = L_1 + M\frac{di_{res}/dt}{di_L/dt} \approx L_1 \quad (2)$$

$$L_{eff,2} = L_2 + M\frac{di_L/dt}{di_{res}/dt} \quad (3)$$

As the inductor current i_L is much larger than the resonant inductor current i_{res}, the mutual coupling between two inductors has negligible impact to the buck regulator inductor value L_1. Meanwhile, the effective resonant inductance $L_{eff,2}$ becomes a little larger/smaller with positive/negative mutual coupling. As shown in the Fig. 6, the current rotation direction determines the polarity of the mutual coupling. The mutual coupling EM simulation results are shown in Fig. 9(d). The simulation results show that the negative mutual coupling M achieves 10~30dB better isolation than positive M at the second and higher harmonic frequency. Therefore, the negative mutual coupling inductor floorplan is chosen in this design. In addition, only a 30MHz center frequency shift of the self-resonator is observed due to mutual coupling.

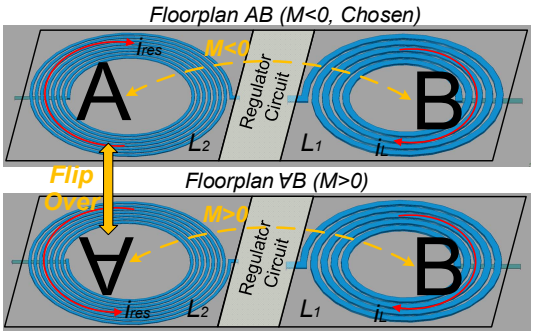


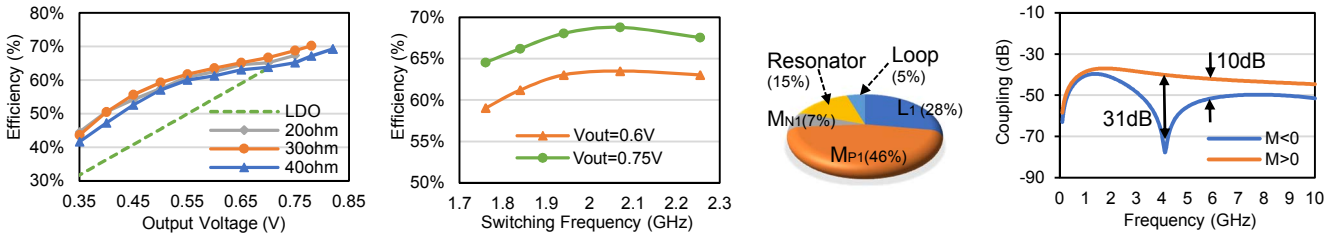
Fig. 6. Inductor placements based on EM simulations, with i_{res} rotating at reverse direction.

III. Measurement Results

The proposed buck regulator is fabricated in a 65nm CMOS process with 1.1V input voltage. The resonant inductor L_2 has the same area as inductor L_1. The regulator core area including two inductors, power switches, self-resonator and the feedback logics only takes 0.079mm^2. The overall area including input/output decaps is 0.137mm^2. The phase noise of the self-resonator was measured from the test chip at the output of the resonant tank, as shown in Fig. 7. The measured self-resonator phase noise achieves -105dBc/Hz at 1MHz frequency offset when resonating at 2GHz, which is significantly better than a typical ring oscillator and indicating a potential high-quality clock source as a by-product. The strong supply noise and lack of filtering of bias current during measurement is suspected to contribute a 6dB degradation compared with simulation results.

Fig. 8 shows the measurement results of transient tracking. The transient reference tracking waveform shows a response speed of 100ns for the voltage change of 140mV (with a single step of adjustment of 40mV at 22ns). With the switching frequency at 2GHz, a 38mV ripple is observed with only 120pF output decap. Under a transient load current change of 10mA (~50% change), the undershoot/ overshoot is around 100mV due to small decap in use and the settling time is 74~78ns. By utilizing larger decap, the undershoot/overshoot will be smaller.

Fig 9(a) and Fig. 9(b) shows the measured power efficiency versus different output voltage level and switching frequency. With the input voltage of 1.1V, a wide output ranges from 0.35V to 0.82V with output power from 3mW to 33mW is achieved. The peak efficiency is 70.3% and remains above 55% for voltage down to 0.45V. The optimal switching frequency to achieve peak efficiency is observed around 2GHz. The power loss breakdown at 0.6V and 2GHz is shown in Fig. 9(c), in which the power loss is dominated by the conduction loss from the power switch M_{P1} and the on-chip inductor L_1.



(a) (b) (c) (d)

Fig. 9. (a) Measured efficiency versus output voltage and (b) switching frequency. (c) Power loss breakdown. (d) EM mutual coupling simulation.

Table. 1 compares the performance of the proposed buck regulator with previous state-of-the-art fully integrated buck regulators. For low voltage performance, the proposed design achieves ~10% better efficiency at ultra-low voltage range of 0.3~0.6V with substantially smaller area [4-5]. The peak efficiency is on part with the previous 73% with the on-chip inductor [7] and 71% with a wirebond inductance [6]. However, the use of the proposed self-resonator eliminates the need of external clock sources and complicated clock drivers. If taking into account the power saving by eliminating the high-speed clock source, e.g. a typical ring oscillator, an equivalent extra efficiency improvement of around 5~9% is obtained. Fig. 10 shows the die micrograph.

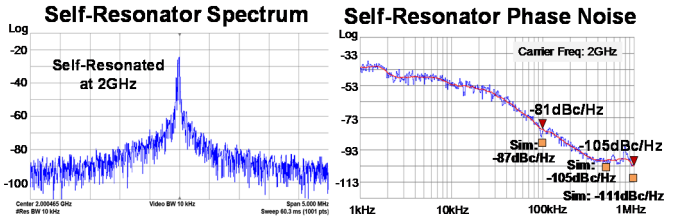


Fig. 7. Self-resonator spectrum and phase noise measurement at 2GHz.

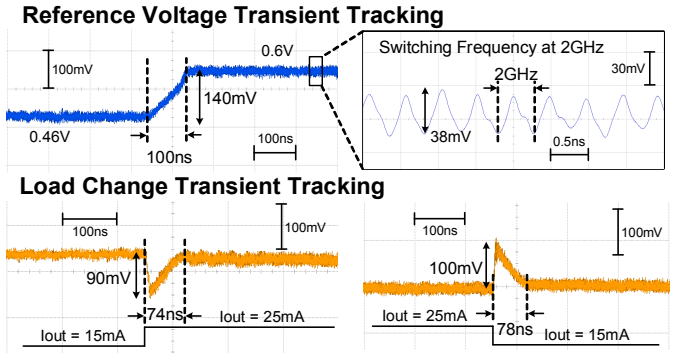


Fig. 8. Measured waveforms for the regulator transient response.

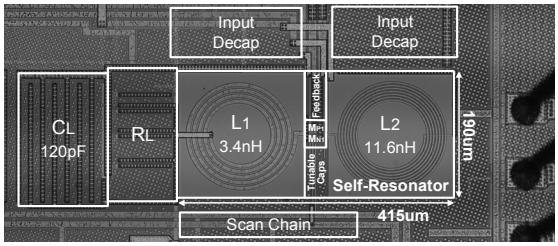


Fig. 10. Chip micrograph.

IV. Conclusion

This paper presents a fully integrated *LC*-oscillator based buck regulator which uses a self-resonator as both clock source and a resonant switch driver for low power applications. The proposed self-resonator design serves as both a high-speed clock source and a resonant switch driver for the regulator, which significantly improves the energy efficiency at high switching frequency and eliminates the external clocks. Measurement on a 65nm testchip shows the proposed design achieves a peak efficiency of 70.3% and an autonomous clock-less operation, with the regulator core area only 0.079mm^2.

TABLE I. Performance Summayr and Comparison

	[4] 14' VLSI	[5] 17' ISSCC	[6] 17' JSSC	[7] 17' VLSI	This work
Process (nm)	22	14	130	65	65
Clk source	External	External	External	External	Self-Resonator
Fsw (MHz)	500	100	125	2000	2000
Iout (mA)	250	90-330	70	10-40	10-50
L (nH)	1.5	1.5	11.8	3	3.4
C_L (nF)	10	5	3.2	0.12	0.12
Vin (V)	1.5	1.5	1.2	1.1	1.1
Vout (V)	0.7-1.2	0.4-1.15	0.45-1.05	0.3-0.86	0.35-0.82
Ripple (mV)	43	>50	84	32	38
Response (ns)	100	700	80	5	20
Peak Eff. (%)	68	84	71	73	70.3
Eff. @0.5Vin (%)	--	<50	~55	65	63
Area (mm^2)	1.5	0.4	0.5	0.073	0.079

Acknowledgment

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References

[1] N. Pinckney, D. Blaauw, D. Sylvester, "Low-power near-threshold design: techniques to improve energy," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 49–57, Jun. 2015.

[2] A. Paidimarri, and A. Chandrakasan, "A buck converter with 240pW quiescent power, 92% peak efficiency and a 2×106 dynamic range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2017, pp. 192–193.

[3] P. Chen, C. Wu, and K. Lin, "A 50 nW-to-10 mW output power tri-mode digital buck converter with self-tracking zero current detection for photovoltaic energy harvesting," *IEEE J. Solid-State Circuits (JSSC)*, vol. 51, no. 2, pp. 523–532, Feb. 2016.

[4] H. Krishnamurthy *et al.*, "A 500MHz, 68% efficient, fully on-die digitally controlled buck voltage regulator on 22nm tri-gate CMOS," in *Proc. IEEE Symp. VLSI Circuits (VLSI)*, Jun. 2014.

[5] H. Krishnamurthy *et al.*, "A digitally controlled fully integrated voltage regulator with on-die solenoid inductor with planar magnetic core in 14nm tri-gate CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2017, pp. 336–337.

[6] M. Kar *et al.*, "An all-digital fully integrated inductive buck regulator with a 250-MHz multi-sampled compensator and a lightweight auto-tuner in 130-nm CMOS," *IEEE J. Solid-State Circuits (JSSC)*, vol. 52, no. 7, pp. 1825–1835, Jan. 2017.

[7] T. Jia, and J. Gu, "A 0.3-0.86V fully integrated buck regulator with 2GHz resonant switching for ultra-low power applications," in *Proc. IEEE Symp. VLSI Circuits (VLSI)*, Jun. 2017.