Sub-Modular Circuit Design for Self-Balancing Series-Connected IGBTs in a Modular Multilevel Converter

Lu Yue
Department of Electrical Engineering
State University of New York at Buffalo
Buffalo, USA
luyue@buffalo.edu

Xiu Yao
Department of Electrical Engineering
State University of New York at Buffalo
Buffalo, USA
xiuyao@buffalo.edu

***Abstract*—Series-connected IGBTs, when properly controlled, operate similarly to a single device with a much higher voltage capacity. Integrating series IGBTs into a Modular Multilevel Converter (MMC) can reduce its complexity without compromising the voltage capacity. This paper presents the circuit design on the sub-modular level of a MMC in which all the switching devices are series-connected IGBTs. The voltage sharing among the series IGBTs are regulated in a self-balancing manner. Therefore, no central series IGBT controller is needed, which greatly reduces the sensing and communication complexities, increasing the flexibility and expandability. Hardware experiment results demonstrate that the series IGBTs are able to self-regulate the voltage sharing in a fast and accurate manner and the system can operate similarly to a sub-module in a MMC. Current**

I. Introduction

Recent developments in High-Voltage DC (HVDC) Transmission and Flexible AC Transmission (FACT) have increased the requirement for high voltage levels. However, current commercial IGBTs can only withstand voltages up to 6.5 kV per device. To increase the voltage capacity, two solutions have become promising: series-connected IGBTs and Modular Multilevel Converter (MMC) [1].

Series-connected IGBTs can handle a voltage determined by the number of devices in series, and a MMC can raise its voltage capacity by adding more sub-modules (SMs). Moreover, it has been demonstrated that, by integrating series IGBTs into a MMC, it is possible to achieve a higher voltage level by using fewer SMs, which reduces the control complexity of the MMC [2]. However, the series connection of IGBTs is challenging due to imbalanced voltage sharing among the devices caused by the mismatches in device parameters, stray elements, and gate signal delays. To regulate the voltage sharing, numerous methods have been proposed. Load-side voltage balancing methods rely on passive snubber circuits that are attached either between the gate and emitter of an IGBT or between the gate and collector of an IGBT [3], [4]. Load-side methods are simple and introduce low delay in IGBT switching time. However, their voltage balancing is poor compared to more sophisticated methods and usually cause high power loss. Gate-side methods balance voltage sharing by sensing the differences in switching behavior and actively adjust the gate signals accordingly, which can achieve effective voltage balancing [5], [6]. However, the control circuits are complicated and they can introduce long delays in switching time. The third type of voltage sharing control combines load-side and gate-side methods where the load-side status is used to adjust the gate-side signals [7].

This paper presents the sub-modular circuit design of series IGBT modules inside a MMC using the method presented in [2] and [7]. The system integration with the circuit design enables the series IGBTs to balance the voltage sharing without introducing extra loops to the MMC controller. With the proposed circuits, the series IGBTs and their corresponding controllers and drivers are plug-and-play with high flexibility and expandability. Hardware experiments demonstrate that, on the string level, the series modules are able to regulate the voltage sharing. On the sub-module level, the output alternates between zero and capacitor voltage.

II. System Diagram and Voltage Balancing Principle

The system diagram of the series IGBT modules inside a MMC phase leg is shown in Fig. 1. Instead of having two switching devices in a sub-module, there are two series strings with multiple series modules. The sub-module operates similarly to a regular sub-module and generates 0 V or V_{CSM} based on the gate signals from the central controller. In the meantime, the voltage balancing among the series modules are achieved by their self-balancing controllers.

The voltage balancing control utilizes the method presented in [2]. Each main switch $S_{j,1}$ is augmented with a snubber circuit consisting of an auxiliary switch $S_{j,2}$ and shunt capacitor $C_{shunt,j}$. The main switch and the auxiliary switch turn on and off in a complementary manner. Therefore, the off-state voltage sharing of the main switches is determined by the capacitor voltage V_{Cshunt}. If one series IGBT shares a larger portion of the total voltage than the rest, its triangular carrier is positively biased based on the voltage. As a result, when the biased carrier is used to modulate the same reference

978-1-5386-8330-9/19/$31.00 ©2019 IEEE

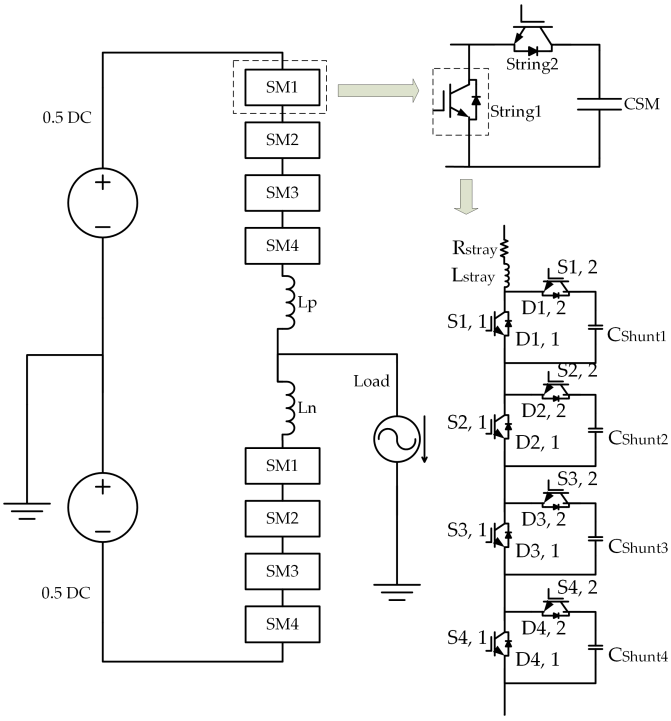

Fig. 1: An MMC with sub-modular series IGBTs

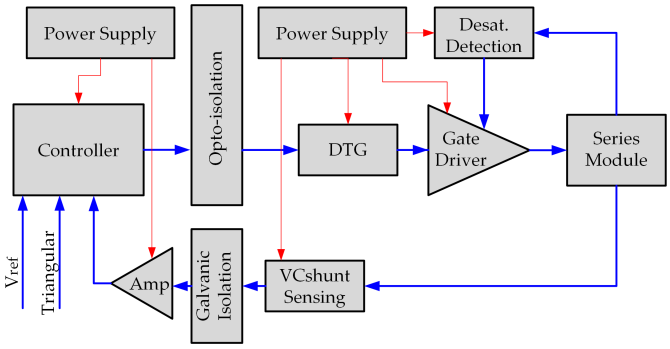

Fig. 2: System diagram of the sub-modular circuit

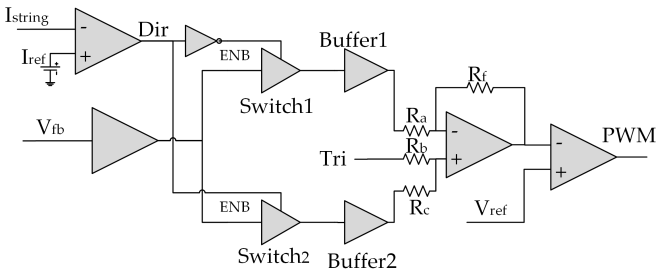

Fig. 3: Circuit diagram of the controller

signal as the other IGBTs, the corresponding IGBT will turn off later and turn on earlier. Its shunt capacitor voltage will decrease since it has less time to charge and more time to discharge. Consequently, the voltages among the series IGBTs will redistribute and achieve self-balance.

III. Sub-Modular Circuit Design

The structure of the sub-module with major function blocks is shown in Fig. 2. Each series module is essentially a self-regulating closed-loop system. The series module voltage, V_{Cshunt}, is measured and fed back to the module controller to generate gate delays following the principle mentioned in the previous section. The output of the controller is then sent to the Dead-Time Generator (DTG) before being received by the dual gate driver, which provides the gate signals for both the main and auxiliary IGBTs. The gate driver is also responsible for measuring the collector-emitter voltages of each IGBT for overcurrent protection, or desaturation detection.

A. Voltage Balancing Controller

The main goal of the voltage balancing controller is to determine which voltage balancing rule should be followed based on the strings current direction, and bias the triangular carrier to modulate the reference. The output of the controller is the PWM signal with delays added. The circuit diagram of the controller is shown in Fig.3. As can be seen, the capacitor voltage feedback will be added to the triangular carrier if the string current is positive. Whereas, if the current is negative, the voltage feedback will be subtracted from the carrier. The resulting carrier is used at the end to modulate the reference. The control rule is as follows:

$$V_{Tri}(t) = Dir_1(t) * K_1 * V_{fb}(t) + V_{Tri} - Dir_2(t) * K_2 * V_{fb}(t)$$

where $V_{Tri}(t)$ is the biased triangular carrier, $Dir_1(t)$ and $Dir_2(t)$ are the current direction indicators. $V_{fb}(t)$ is the shunt capacitance voltage feedback from the sensing circuit. K_1 and K_2 are the gains determined by the ratio of $\frac{R_f}{R_{a,b,c}}$.

B. IGBT Gate Driver

The gate driver, powered by isolated converters at +15/-5V, receives the PWM signal from the controller through an opto-isolator interface and adds a delay to the rising edges of the PWM signal to create the dead-time. The gate driver then uses the delayed gate signal to drive the IGBT. The circuit diagram of dual gate drivers for one series module is shown in Fig. 4.

When one channel input is high, i.e. a rising edge, the capacitor C_{DT} will be charged through R_{DT}. The slow rising capacitor voltage is then compared with a preset value $V*$. The dead-time can be adjusted by changing the time constant of $R_{DT} - C_{DT}$ branch and $V*$. In the proposed test system, R_{DT} consists of a bank of resistor ranging from 10 Ohms to 1 kOhm, so that the dead-time is adjustable. The selection of dead-time must take into consideration the biased triangular carriers. When used to modulate the same reference, the carriers will inject delays into the PWM signals, negating the effect of dead-time generator. Therefore, one must ensure the dead-time is greater than the biggest possible gate delay produced by the controller.

The over-current protection circuit disables the gate drive operational amplifier when the IGBT is driven out of the saturation region into the linear region by a large current.

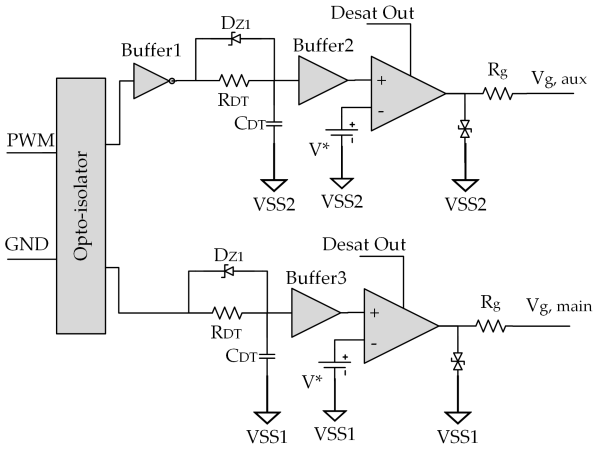

Fig. 4: The diagram of the dual gate driver.

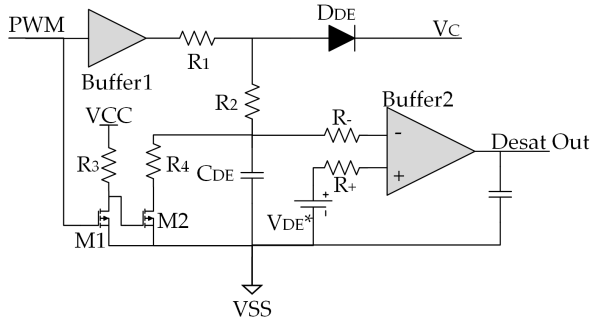

Fig. 5: Circuit diagram of the desaturation detector.

During overcurrent fault, the collector-emitter voltage will become much higher than the normal 1 V 4 V on-state voltage drop. The diagram is shown in Fig. 5. When the gate signal is at high level, the sensing diode becomes forward-biased and its anode voltage is clamped at $V_C + 0.7V$. Normally the anode voltage is not high enough to charge the capacitor C_{DE} to a voltage high enough to trigger the subsequent circuit. However, during desaturation, the capacitor voltage will surpass the set threshold $V*_{DE}$ and cause the output to be low which, in turn, disables the gate drive amplifier. During the IGBT off-state, D_{DE} blocks V_{CE} while C_{DE} discharges quickly through R_4 and M_2.

IV. Experimental Verification

A. Test System

To experimentally verify the proposed circuit design, a prototype was developed. The diagram of the test system is shown in Fig. 6. The switching unit inside a sub-module each contains two series IGBT modules. Each string regulates the voltage sharing on its own by modulating the reference input with a biased carrier. Therefore, no central controller is needed. The sub-module is connected to a dc supply through an inductor and a resistor. The circuit parameters are provided in Table I. Output of the sub-module is taken between V+ and V-, or over the String1.

TABLE I: Circuit parameters.

V_{dc}	200 V	R	94 Ω	L	1 mH
C_{shunt}	1 μF	f_{sw}	5 kHz	C_{SM}	1 mF

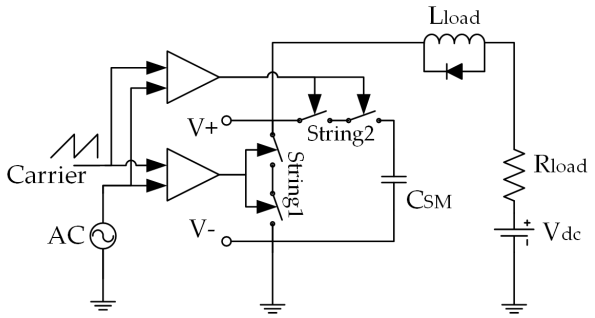

Fig. 6: The diagram of the test system with strings of series modules.

A string of two series modules is shown in Fig. 7. Each hardware module consists of three boards: the motherboard, controller, and the gate driver. The motherboard is designed to serve as the hub for all the function blocks in Fig. 2. It consists of interfaces with the controller and the gate driver, power supplies, power components, electrical isolation, and isolated V_{Cshunt} sensing. The isolated voltage sensing is achieved with an AMC1200 isolation amplifier followed by an additional operational amplifier to reduce the dc offset. The two switches in the controller circuit in Fig. 3 for routing the feedback signal are realized using CD4016 analog switches.

B. Series Module Voltage Sharing

Fig. 8 shows the imbalanced voltage sharing between two series modules. The waveforms were captured using MSO58 oscilloscope and THDP0200 voltage probes. It can be seen that without proper control, the voltage sharing is uneven with one module withstanding almost the entire source voltage.

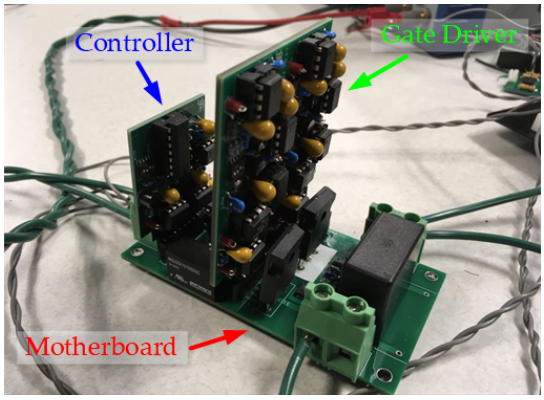

Fig. 7: One string with two series modules.

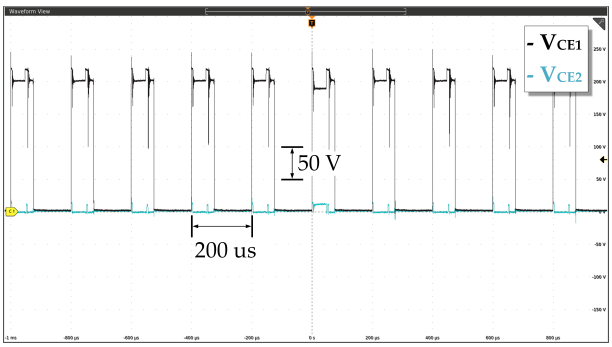

Fig. 8: Imbalanced voltage between two series modules.

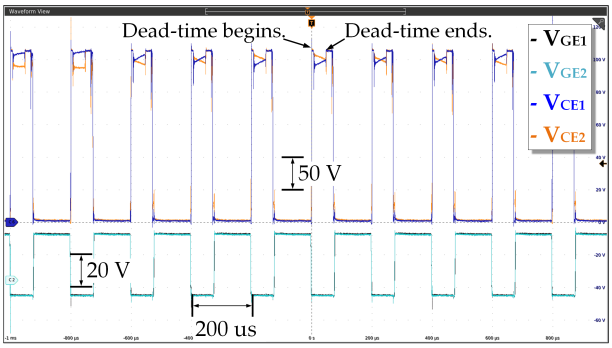

Fig. 9: Balanced voltage between two series modules.

With balancing control, the voltage sharing among the two series modules, shown in Fig. 9, is improved. It can be seen that both modules now share 100 V with little turn-on or turn-off delay. The initial imbalance at the beginning of each turn-off duration is caused by the dead-time generator. During dead-time, both IGBTs of one string are off and, since it is the interval between gate pulses, no voltage balancing can be realized. Therefore, the IGBT voltages will experience a short "free-roaming" period. One can see from Fig. 9 that, immediately after the dead-time is over, V_1 and V_2 become balanced as the next gate pulse arrives. By reducing the dead-time, one can shorten the duration of such voltage imbalance.

Fig. 10 demonstrates the transient voltage sharing during balanced turn-off. The figure on top shows the transient V_{ce} of the two IGBTs while the one on the bottom shows their corresponding gate signals. One can see that the gate signal delay introduced by the controller is short compared to the V_{ce} rise time of the IGBTs. This short delay ensures that, as a group, the two IGBTs can turn on and off with little external delay compared to a single device. From the experimental results, it can be verified that the proposed circuit is able to function on the string level, offering fast and accurate voltage balancing.

C. Sub-modular Output

On the sub-module level, the string voltages and the main IGBT gate signals of each string are provided in Fig. 11. It can be seen that, the sub-module output, $V_{string1}$, alternates between zero and source voltage 200 V. Therefore, on the

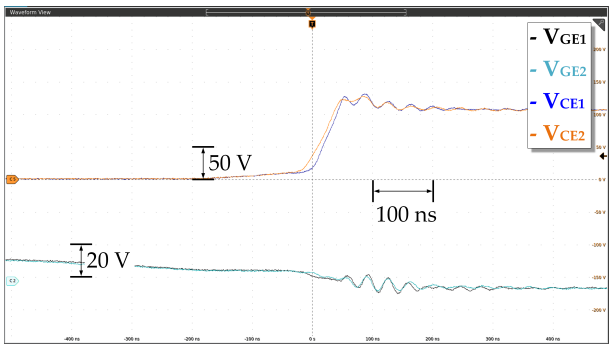

Fig. 10: Transient voltage sharing between two series modules.

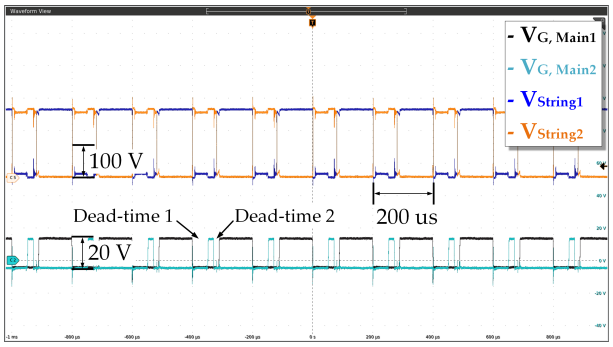

Fig. 11: String voltages and main IGBT gate signals of two strings.

system leve, the proposed circuit resembles a regular sub-module of a MMC. The main IGBT gate signals of both strings, as shown in the bottom figure, are separated by adequate dead-time. Dead-time 1 and Dead-time 2 prevent the two strings from turning on simultaneously as a result of the controller-injected delay. On the other hand, the dead-time causes voltage "free-roaming" between the two strings which results in output voltage fluctuation.

D. Current Commutation

The load and string current waveforms are plotted in Fig. 12. During steady-state, the load current is 2.1 A, determined by the source voltage and load resistance. It can be seen that, on the sub-module level, the output current resembles that of a regular sub-module.

On the other hand, if string currents within the sub-module are concerned, the current distribution during one cycle can be characterized by 4 additional transients, a, b, c, and d as marked in Fig. 12. The current paths are plotted in Fig. 13 with the assumption that each string is operating with balanced voltage sharing. Therefore, the gate delays from the controllers are much smaller than the dead-time. Consequently, each string can be regarded as one switching unit. Since the voltage balancing is a dynamic adjustment, the four transients may not all appear during one cycle.

Transient a, as shown in Fig. 13a, is caused when S_4 turns on before S_1 in the beginning of a cycle. C_{Shunt1} and C_{SM} will then be charged by the rising source current while S_1 branch remains an open circuit.

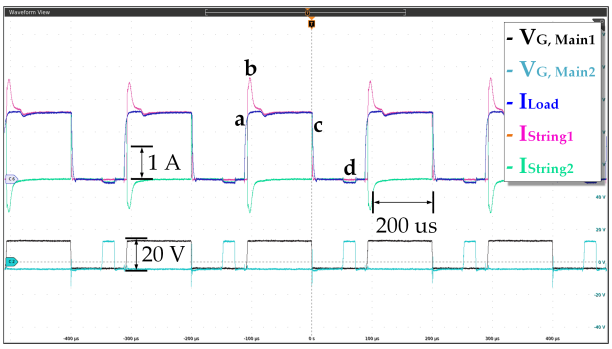

Fig. 12: Load and string currents.

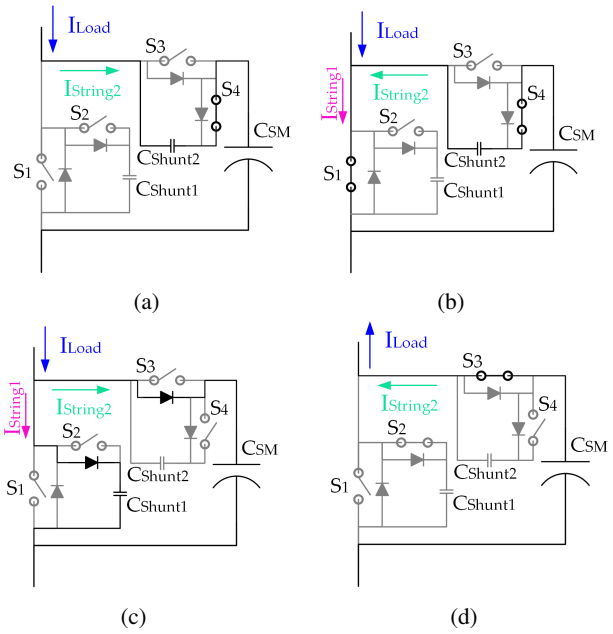

Fig. 13: Current distribution at four transients during one cycle.

Once S_1 turns on at the beginning of transient b, the collector-emitter voltage of S_1 will decrease, causing the capacitors to stop charging and start to discharge. As shown in Fig. 13b, both I_{Load} and $I_{String2}$ will contribute to $I_{String1}$, resulting in a current spike. Reducing the duration of transient a will in turn suppress such current spikes.

Transient c begins when S_1 turns off, at which instance the tailing load current will charge C_{SM} through the free-wheeling diode of S_3 because of the voltage rise at its anode. Another portion of the tail current will charge C_{Shunt1} as shown in Fig. 13c which results in a small current spike for $I_{String1}$.

When the load current falls to zero, V_{CSM} will reach its peak. However, because of the dead-time, C_{SM} will not discharge until transient d, when S_3 turns on. As can be seen in Fig. 13d, the discharge current and the load current are the same in magnitude and are both negative, meaning they flow back to the source.

V. Conclusion

In this paper, a sub-modular circuit design to integrate series-connected IGBTs with a Modular Multilevel Converter was presented. The proposed circuit design ensures that the series IGBT modules regulate the voltage sharing in a self-balancing manner. Therefore, the series IGBT control does not rely on a central controller or introduce extra control loops to the MMC controller. Furthermore, with the proposed design, the series strings as well as the corresponding controllers and drivers can operate independently as part of a sub-module. Hardware experiments on a test system at 200 V demonstrated that the voltage balancing controllers are able to regulate the voltage sharing among the series modules in a fast and accurate manner. The delay introduced by the controller is small compared to the IGBTs switching time. The output of the test system resembles that of a regular sub-module. Finally, transient current distributions between strings are examined, demonstrating that, with adequate dead-time, no dangerous current spikes will be generated.

Acknowledgment

This material is based upon work supported by the National Science Foundation under grant no. ECCS 1711659.

References

[1] R. Marquardt, "Stromrichterschaltungen mit verteilten energiespeichern," German Patent, 2001.

[2] L. Yue and X. Yao, "Investigation of control and applications of modular multilevel converter with sub-modular series igbts," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, USA, Mar. 2018, p. 1486 1491.

[3] S. Castagno, D. Curry, R, and E. Loree, "Analysis and comparison of a fast turn-on series igbt stack and high-voltage-rated commercial igbts," *IEEE Transactions on Plasma Science*, vol. 34, no. 5, pp. 1692 – 1696, 2006.

[4] J. Chen, J. Lin, and T. Ai, "The techniques of the serial and paralleled igbts," in *Proc. IEEE 22nd International Conference on Industrial Electronics, Control, and Instrumentation*, Taipei, Taiwan, 1996, pp. 999 – 1004.

[5] T. Lu, Z. Zhao, J. Shiqi, H. Yu, and L. Yuan, "Active clamping circuit with status feedback for series-connected hv-igbts," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3579 – 3590, 2014.

[6] P. Palmer, W. He, X. Zhang, J. Zhang, and M. Snook, "Igbt series connection under active voltage control with temporary clamp," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Montreal, QC, Canada, 2012, pp. 465 – 470.

[7] L. Yang, P. Fu, X. Yao, and J. Wang, "A module based self-balanced series connection for igbt," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014.