# Optimal Accelerated Test Regions for Time-Dependent Dielectric Breakdown Lifetime Parameters Estimation in FinFET Technology

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*Abstract*— **This paper proposes a methodology to find optimal accelerated test regions for lifetime parameter estimation for not only the traditional reliability concern, frontend-of-line dielectric breakdown (FEOL TDDB), but also the newly emerging wearout mechanism, middle-of-line time dependent dielectric breakdown (MOL TDDB) in 14nm FinFET technology. The framework to find the optimal test regions is introduced; the error estimating methodology is discussed in detail. Three digital circuits are presented for evaluation and comparison. The optimal test regions depend on the circuit size as well as the types of standard cells in the circuits. To ensure accurate lifetime parameter estimation, both error from sampling and error from selectivity should be considered at the same time. As a general guideline, higher estimation accuracy will be achieved by testing gate TDDB lifetime parameters at higher voltages, while testing middle-of-line TDDB at higher temperatures.**

***Keywords—time-dependent dielectric breakdown; lifetime; wearout; frontend-of-line dielectric breakdown; middle-of-line breakdown; digital circuit; FinFET; reliability***

## I. INTRODUCTION

Technology scaling has enabled the implementation of circuit designs with higher operating frequencies, smaller areas, and better performances. However, as the feature size shrinks, the reliability of a circuit has become a significant issue. Traditional wearout mechanisms, such as Front-End-of-Line time-dependent dielectric breakdown (FEOL TDDB), Back-End-of-Line time-dependent dielectric breakdown (BEOL TDDB), hot carrier injection (HCI), bias temperature instability (BTI), electromigration (EM) and stress induced void (SIV) continuously degrade circuit performance during operations and have made it harder to guarantee the reliability of a circuit over its product lifetime. With the introduction of FinFET technology, circuit designers need to consider the traditional wearout mechanisms as well as the newly emerging middle-of-line (MOL) time-dependent dielectric breakdown.

One of the dominant wearout mechanisms in modern digital circuits is TDDB. Many previous studies have analyzed exhaustively traditional FEOL TDDB, where the introduction of new device configurations and smaller feature sizes has continuously challenged dielectric integrity. As a result, FEOL TDDB remains an important reliability concern. Middle-of-line (MOL) dielectric breakdown happens between the polysilicon/high-k control gate (PC) and the diffusion contacts (CA) [1]. This recently emerging middle-of-line (MOL) TDDB is a growing concern for semiconductor device reliability. This work uses the feature-level wearout models to analyze circuit-level vulnerability to FEOL TDDB and MOL TDDB. This work could be extended to include BEOL TDDB. However, BEOL TDDB is not considered in this paper because it doesn't significantly affect the circuit structures considered. It may have a greater impact on the interconnects of the power delivery networks of larger circuits.

Lifetime data for individual wearout mechanisms is collected using dedicated test structures. However, because circuits are substantially more complex than the test structures, it is desirable to verify the lifetime of circuits directly with accelerated life tests, by applying stress to circuits at high voltages and temperatures. At high voltages and temperatures, the circuits have a lower mean-time-to-failure (MTTF).

This work shows that accelerated life tests can accelerate different wearout mechanisms, depending on the voltage and temperature settings. Consequently, the accelerated mechanisms causing circuit failures may or may not be the dominant ones at use conditions. Moreover, if the results of accelerated tests do not conform with expectations, the data collected from accelerated life tests of circuits can be used to improve the physical lifetime models of the wearout mechanisms. But, to obtain accurate model parameters, we need to decouple different wearout mechanisms by properly setting the test conditions, i.e., to select test conditions where only one wearout mechanism is dominant.

This leaves us with the important task to find the optimal test conditions for each of these wearout mechanisms. We would like to test the circuit with the corresponding test conditions where only one wearout mechanism is likely to happen. We can then use these data to obtain the parameters of the wearout model via measurements on circuits.

In previous circuit-level reliability studies, researchers have studied BTI [2]–[5], HCI [4], [6]–[8], FEOL TDDB [6], [9]–[16], backend-of-line (BEOL) TDDB [17], EM [18], and SIV [19]. Recent studies also show MOL TDDB is an non-negligible reliability concern for digital circuits and memory systems [12]–[14].

This paper investigates only FEOL and MOL TDDB wearout for digital circuits implemented in FinFET technology, as these are among the more important wearout mechanisms. Future work will extend the analysis to other mechanisms. The breakdown locations for FEOL and MOL TDDB are shown in Fig. 1. The TDDB lifetime assessment flow for circuits is

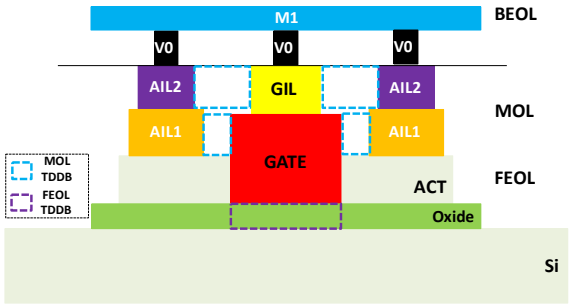



Fig. 1. Illustration of FEOL TDDB and MOL TDDB.

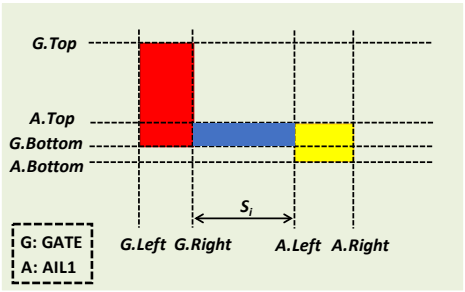



Fig. 2. Illustration of MOL TDDB vulnerable features.

TABLE I. PARAMETERS USED FOR FEOL TDDB

| Aox | β | a | b | c | d |
|---|---|---|---|---|---|
| 5.00E-07 | 1.64 | -78 | 0.081 | 8.81E+03 | -7.75E+05 |

TABLE II. PARAMETERS USED FOR MOL TDDB

| $A_{MTDDB}$ | β | m | γ(cm/MV) | $E_a$ (eV) |
|---|---|---|---|---|
| 0.000676 | 0.98 | 1 | 8.723113 | 0.5 |

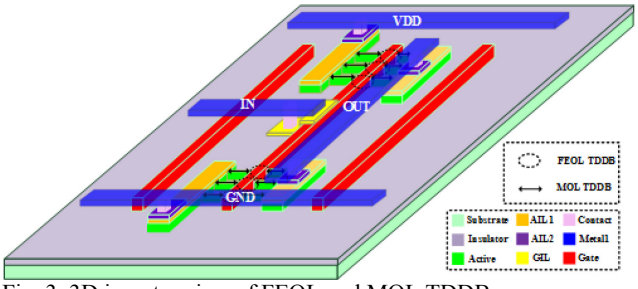



Fig. 3. 3D inverter view of FEOL and MOL TDDB.

presented in this paper as well. We compare the optimal test conditions for different digital circuits.

The rest of this paper is organized as follows. Section 2 presents the wearout models used for TDDB. In section 3, we introduce the lifetime assessment flow. Section 4 presents the methodology for calculating the errors in estimating the characteristic lifetime of circuits. Section 5 gives the comparison of optimal test regions for different circuits. Section 6 concludes the paper.

## II. DEVICE-LEVEL WEAROUT MODELS

### A. FEOL TDDB Model

FEOL TDDB is described as the build-up of traps in the gate oxide as a function of time under voltage and thermal stress. The hard breakdown (HBD) model is used in this study to characterize the transistor lifetime distribution. For ultra-thin (< 5nm) gate dielectrics, the time-to-failure due to gate-oxide degradation can be derived by connecting the oxide degradation model to the Weibull failure distribution function [20]; we use a two parameter Weibull distribution to describe the characteristic lifetime. $\beta$ is the shape parameter, and η is the characteristic lifetime, which is the time-to-failure at the 63% probability point, i.e.,

$$\eta = A_{ox}\left(\frac{1}{WL}\right)^{\frac{1}{\beta}} e^{-\frac{1}{\beta}} V^{a+bT} \exp\left(\frac{c}{T} + \frac{d}{T^2}\right) s^{-1} \quad (1)$$

where $W$ and $L$ are the device width and length, respectively, $s$ is the probability of stress, which is the portion of time that the gate is being stressed under a clock period, $T$ is temperature, $V$ is gate voltage, and $a$, $b$, $c$, $d$, and $A_{ox}$ are fitting parameters. A gate is under stress if it is "on", which means that the gate voltage is "1" and "0" for NMOS and PMOS devices, respectively. To obtain those parameters, p+poly/n-Si capacitors are used as the test structure and tested under various voltages and temperatures [21]. The detailed values are shown in Table I. This data was obtained from tests of ultra-thin oxides (<5nm).

### B. MOL TDDB Model

Although we do not discuss BEOL TDDB in this paper, the device-level lifetime model for MOL TDDB is similar to that of BEOL TDDB [22] as follows:

$$\eta = A_M L_i^{-1/\beta_i} \exp(-\gamma E^m - E_a/kT) s^{-1} \quad (2)$$

where $A_M$ is a constant that depends on the material properties of the dielectric between the gates and contacts, γ is the field acceleration factor, $E_a$ is the activation energy (~0.5eV), $L_i$ is the vulnerable length, and $m$ is 1 for the E model. We calculate the electric field by $V/S_i$, where V is the voltage difference between the two conductors and $S_i$ is the distance between the two conductors. S is the stress probability, which is the probability that the gate and nearby contacts are at different voltages.

As shown in Fig. 2, the red rectangle represents a poly gate and the yellow rectangle represents the adjacent contact. In this graph, the vulnerable length is shown as $L_i$ and the distance between conductors is shown as $S_i$. The temperature dependence is modelled with the Arrhenius relationship [23], where $k$ is the Boltzmann constant. To test MOL PC-CA lifetime, SiN and low-k films were used between the gates and contacts as the insulation spacer film. The test structure consisted of a MOS capacitor electrode and the adjacent contact. All MOL structures were laid out with shallow trench isolation (STI) oxide to isolate the PC-CA breakdown from gate dielectric breakdown. All parameters are extracted from results in [1]. The parameters are given in Table II are were determined using a 14nm CMOS process.

Depicted in Fig. 3, a detailed 3D illustration of TDDB in a layout in FinFET technology is presented. We can see clearly that the location of FEOL TDDB is shown as the dashed circle which happens under the gate oxide and the location of MOL TDDB is between the gate and its adjacent contact.

## III. CIRCUIT LIFETIME ASSESMENT

To estimate a circuit's lifetime, we assume a circuit is composed of n components, each modelled with a Weibull distribution, for each wearout mechanism. For FEOL TDDB the

components are the transistors. Hence a circuit with n transistors has n components. For MOL TDDB the components are the dielectric segments between the gates and contacts, illustrated in Fig. 2. Both the lifetimes of transistors and dielectric segments are defined by equations (1) and (2), respectively.

The probability of failure at time $t$ for each component is modeled with a Weibull distribution, with characteristic lifetime, $\eta$, and shape parameter, $\beta$. The probability of failure, P, at time t is calculated with the following equation [16]:

$$P(t) = 1 - \exp(-\left(\frac{t}{\eta}\right)^{\beta}) \quad (3)$$

The characteristic lifetime of the circuit, $\eta_{circuit}$, is a combination of Weibull distributions for the components and is the solution of [9]:

$$1 = \sum_{i=1}^{n}(\eta_{circuit}/\eta_i)^{\beta_i} \quad (4)$$

where $\eta_i, i = 1, \ldots, n$ are the characteristic lifetimes of all the circuit components, and $\beta_i, i = 1, \ldots, n$ are the corresponding shape parameters. Similarly [26]:

$$\beta_{circuit} = \sum_{i=1}^{n}\beta_i(\eta_{circcuit}/\eta_i)^{\beta_i}. \quad (5)$$

If the shape parameter is the same for each component, which is typically assumed,

$$\eta_{circuit} = \left(\sum_{i=1}^{n}\eta_i^{-\beta}\right)^{-1/\beta} . \quad (6)$$

To calculate the FEOL TDDB lifetime of a circuit, we need to obtain the gate-source voltage, $V_{gs}$, for each transistor and to analyze each transistor's stress probability. The stress probability for a transistor is obtained from the activity profile through the simulation result of the corresponding circuits. Combined with transistor size information, we use (1) to calculate every transistor's characteristic lifetime $\eta_i$. By using (3) – (6), we get the failure probability of the whole system.

As for the MOL TDDB lifetime, we have to analyze the standard cell layout for vulnerable feature extraction first. For each adjacent poly-contact pair in layout, we need to extract the linespace $S_i$ and vulnerable length $L_i$, as shown in Fig. 2. After that, for each poly-contact pair, the vulnerable feature pair ($S_i$, $L_i$) is associated with the poly-contact voltage difference $V$, and is plugged into (2) to get each feature's MOL TDDB lifetime. With the combination of (3) – (6), we can calculate the characteristic lifetime of the circuit under MOL TDDB.

We define the probability that a mechanism will fail first within a certain test time limit as the selectivity of that specific wearout mechanism at the corresponding voltage and temperature,

$$Prob_{x\_fail\_first} = \int_0^{t_{stop}} Prob(x < Y | Y = y) f_y(y) dy \quad (7)$$

where $f_y(y)$ is the probability density function of $y$; and in the content of this study, it is the probability density function of the Weibull distribution, i.e., $f_y(y) = \left(\frac{y}{\eta_y}\right)^{\beta_y - 1} \frac{\beta_y}{\eta_y} e^{-(y/\eta_y)^{\beta_y}}$.

The lifetime assessment flow of the TDDB lifetime simulator is shown in Fig. 4. First we supply the NCSU FreePDK15 [27] FinFET technology library to Design Compiler [28] to generate the RTL netlist of the circuit. We combine the netlist with our test vectors or benchmarks and load them onto an FPGA for emulation [29]. Then we obtain the activity and stress profile of each net in the circuit by using PrimeTime [30] activity propagation. Also, we consider the self-heating effects of FinFETs and calculate the temperature distribution using COMSOL [31]. In the meantime, our vulnerable feature extractor analyzes the spice netlist and standard cell layout to obtain the vulnerable features in the circuit. With all the data, our lifetime simulator calculates the characteristic lifetime and failure probability of the whole circuit. Details of the extraction flow and characteristic lifetime calculation can be found in [13].

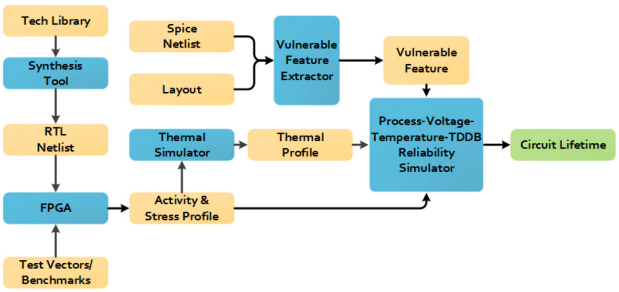



Fig. 4. Lifetime assessment flow.

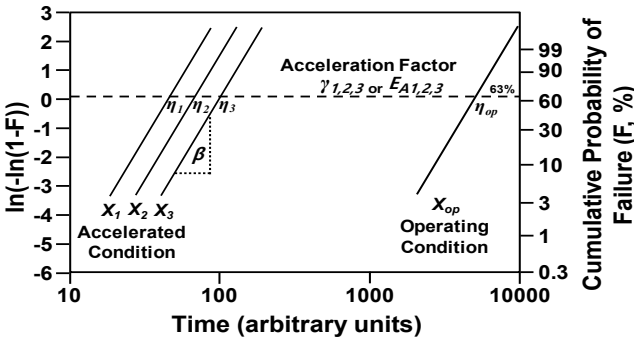


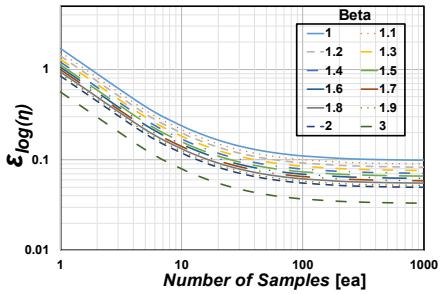

Fig. 5. Errors in estimating a Weibull distribution at the operating condition using system-level accelerated life test has two components: errors in the estimation of Weibull parameters at accelerated conditions and the errors in regression to project the results at the operating condition. The thin solid lines reflect the collected data at the accelerated test conditions and the thick solid line reflects the predicted wearout distribution at use conditions.

## IV. Errors in Estimating Wearout Parameters at System-Level Accelerated Life Test Conditions

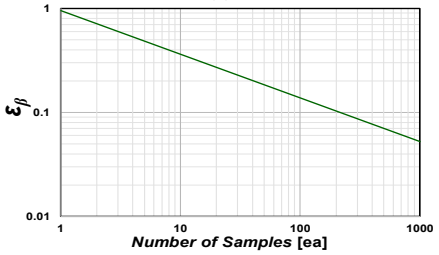
Fig. 5 shows wearout distributions obtained from system-level accelerated life test. There are two sources of errors. First, there are errors in estimating the Weibull distribution at accelerated conditions. Second, there are errors in estimating the Weibull distribution at the use conditions. The first type of error relates to the parameters of the thin solid curves at accelerated test conditions, reflected in estimating $\beta, \eta_1, \eta_2$ ... The second type of error relates to errors in estimating errors at use conditions which is depicted by the thick solid line. These are regression errors.

During testing, we monitor the time-to-failure at high stress test conditions for accelerating breakdown in the dielectrics. At each test point, we fit measured data to a Weibull distribution by employing an estimator, such as least squares or maximum likelihood regression.

Figs. 6 gives the errors in estimating $\log(\eta)$ and $\beta$, with a one-sided 95% confidence interval, calculated using Monte Carlo simulation with the generalized maximum likelihood method for estimation [32]. The terms $\varepsilon_{\log(\eta)}$ and $\varepsilon_{\beta}$ are relative errors, so that the results are independent of units. If we increase the number of samples, the accuracy in estimation of $\log(\eta)$ and $\beta$ will also increase.




(a)




(b)

Fig. 6. Relative errors in (a) estimating $\log(\eta)$ and (b) estimating $\beta$.

To calculate the errors in estimating Weibull parameters, we employ a binomial distribution to model errors caused by selectivity. To estimate such errors in estimating $\log(\eta)$ caused by selectivity, $\varepsilon_{\log(\eta)-selectivity}$, we employ the Wilson interval [32] as follows:

$$\Delta\hat{p} = \frac{2z}{1+\frac{1}{n}z^2}\sqrt{\frac{1}{n}\hat{p}(1-\hat{p}) + \frac{1}{4n^2}z^2} \tag{8}$$

where $\hat{p}$ is selectivity of a target wearout mechanism at a test condition, $n$ is the total number of TDDB failures detected at a test condition, and $z$ is the standard normal random variable ($z = 1.96$ at a 95% confidence interval). The Wilson interval is a more accurate confidence interval for the binomial variable, $\hat{p}$.

From (7), the estimated selectivity $\hat{p}$ resulting from a target wearout mechanism ranges from $[\widehat{p_l}, \widehat{p_u}]$, yielding variation in the cumulative probability of failure due to the target wearout mechanism, $F$, at a test condition,

$$F = \frac{n}{N}\hat{p} \tag{9}$$

where $N$ is the total number of circuits under test. Because of variation in $\hat{p}$, the cumulative probability of failure, $F$, is also a random variable, and $F_l = n\widehat{p_l}/N$ and $F_u = n\widehat{p_u}/N$ are the lower and upper confidence bounds respectively.

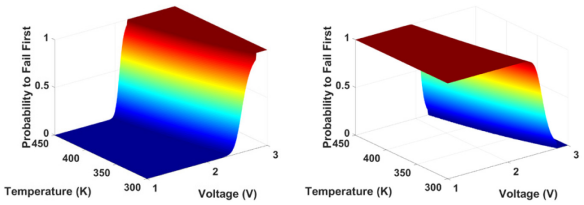
Variation in $\hat{p}$ causes variation in the cumulative probability of failure, $F$. This variation causes variation in the characteristic lifetime $\eta$,

$$\Delta\ln(\eta) = \ln(\eta_l) - \ln(\eta_u) = \frac{1}{\beta}\cdot\ln\left(\frac{ln\left(1-\frac{1}{\widehat{p_l}}+\frac{1}{e\widehat{p_l}}\right)}{ln\left(1-\frac{1}{\widehat{p_u}}+\frac{1}{e\widehat{p_u}}\right)}\right) \tag{10}$$

If we set $z = 1$ in (7), then $\varepsilon_{\log(\eta)-selectivity} = \Delta\log(\eta)/2$.

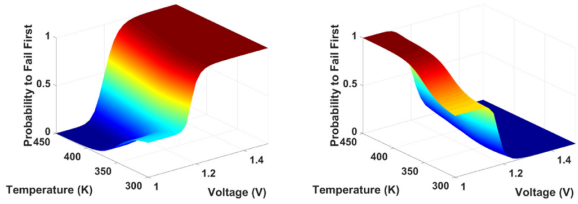
We can obtain $\varepsilon_{\ln(\eta)-sample}$ from Fig. 6, and thus, the total errors in estimating $\eta$ can be expressed as,

$$\varepsilon_{\ln(\eta)} = \sqrt{\varepsilon^2_{\ln(\eta)-sample} + \varepsilon^2_{\ln(\eta)-selectivity}} \tag{11}$$



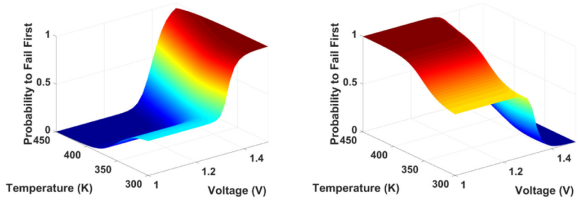

(a) (b)

Fig. 7. Selectivity for the ring oscillator: (a) FEOL TDDB and (b) MOL TDDB.




(a) (b)

Fig. 8. Selectivity for the FFT circuit: (a) FEOL TDDB and (b) MOL TDDB.




(a) (b)

Fig. 9. Selectivity for the Leon3 microprocessor: (a) FEOL TDDB and (b) MOL TDDB.

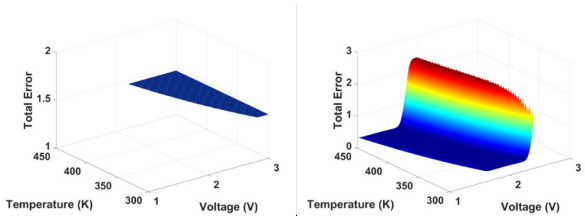
## V. Optimal Accelerated Test Region

To find the optimal accelerated test region, we simulate errors in estimating the characteristic lifetime, $\eta$, for FEOL and MOL TDDB at accelerated conditions, respectively, and select the test area with the minimum estimation error for the corresponding wearout mechanism.

In this study, we explore the optimal test region for three digital circuits. A 101-stage ring oscillator, an 8-bit FFT circuit and a Leon3 microprocessor were implemented in NCSU FreePDK15 FinFET technology. The FFT circuit consists of 112k cells and the Leon3 microprocessor has 321k cells.

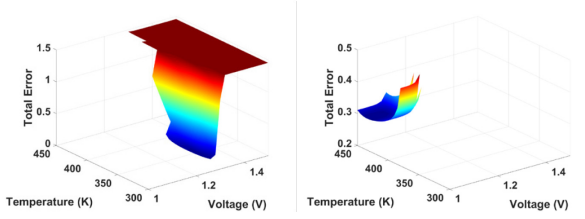
### *A. Probability to Fail First in the Whole Test Domain*

We use (1) and (2) to calculate the characteristic lifetime of each vulnerable feature in the circuit and use (4) – (6) to combine the individual characteristic lifetimes to get the whole circuit characteristic lifetime under FEOL and MOL TDDB. By applying (3), we can find the failure probability of the target wearout mechanism. And we perform the integration in (7) to get the probability of FEOL and MOL TDDB failing first under every test condition with a two-week test time. Results for our circuits can be found in Figs. 7 – 9.



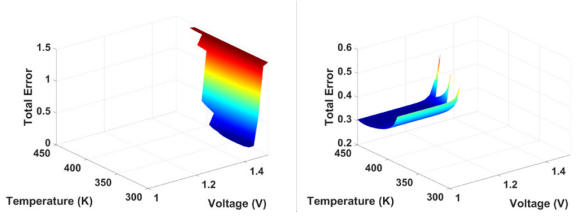

(a) (b)

Fig. 10. Total estimating errors for the ring oscillator: (a) FEOL TDDB and (b) MOL TDDB.




(a) (b)

Fig. 11. Total estimating errors for the FFT circuit: (a) FEOL TDDB and (b) MOL TDDB.




(a) (b)

Fig. 12. Total estimating errors for the Leon3 microprocessor: (a) FEOL TDDB and (b) MOL TDDB.

We can observe that different circuits have different selectivities for the wearout mechanisms. However, we can spot the trend that FEOL TDDB fails first at high voltages, while MOL TDDB is more sensitive to temperature and is more likely to fail first at high temperatures. This finding gives us a qualitative sense of the region for the optimal accelerated test conditions.

### *B. Total Errors in Estimating Characteristic Lifetime*

Using (8) and (9) we can find the lower and upper limit of the selectivity corresponding to the target wearout mechanism. When applying (10), we need to be careful to preprocess the data, since we cannot have any term in the logarithm whose value is less than or equal to zero. Thus, when using (10), we can only extract the model parameters when the selectivity is high enough. Under these specific accelerated test conditions, a large portion of the circuits fail for only one wearout mechanism, and hence the data can be used to extract wearout model parameters.

The total estimation errors for the ring oscillator, the FFT circuit and the Leon3 microprocessor are shown in Figs.10 - 12. We can find that the FFT circuit and the Leon3 microprocessor have similar results, while the ring oscillator is a relatively small circuit and needs to be tested with a higher voltage for FEOL TDDB. In addition, one may notice that although the FFT circuit has a smaller standard cell count than the Leon3 microprocessor, it fails faster than the Leon3. This can be explained by the types of standard cells used in the FFT circuit, which are more sensitive to FEOL and MOL TDDB.

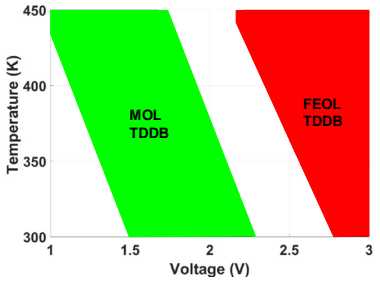



Fig. 13. Combined domain for detectability and selectivity for the ring oscillator.

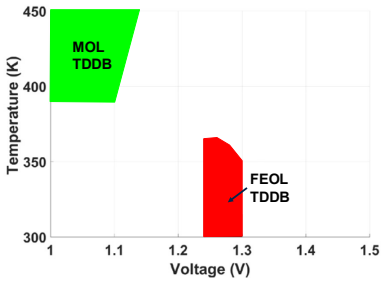



Fig. 14. Combined domain for detectability and selectivity for the FFT.

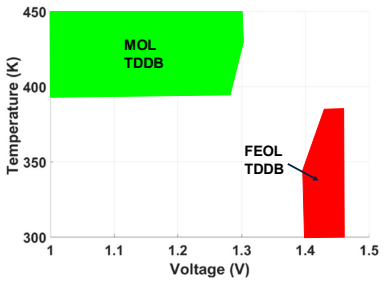



Fig. 15. Combined domain for detectability and selectivity for the Leon3 microprocessor.

### *C. Optimal Test Region*

We set the threshold to select the optimal test region where the total estimating errors are less than two times the global minimum errors for each mechanism. With this criterion, we have the optimal test region for FEOL and MOL TDDB for our circuits shown in Figs. 13 - 15.

As we expected, MOL TDDB is more sensitive to temperature, and we could obtain lower estimation errors for the characteristic lifetime in the high temperature domain. FEOL TDDB is more vulnerable under high voltages, and we could get lower estimation errors under higher voltages. However, the specific optimal test domains depend on the type of circuit as well as the size of the circuit. The ring oscillator only has 101 stages which means it needs higher stress to observe a failure, while the large cell count for the FFT circuit and the Leon3

microprocessor make them more likely to fail under accelerated test.

## VI. Conclusion

This paper investigates not only the traditional reliability concern, FEOL TDDB, but also the newly emerging wearout mechanism, MOL TDDB. A lifetime assessment flow is presented for target wearout mechanisms; moreover, the detailed error estimating methodology is introduced and the corresponding optimal accelerated test conditions for these wearout mechanisms are presented. To perform circuit-level accelerated life test, the optimal test conditions vary from circuit to circuit and need to be carefully assessed before conducting the test. Only the test in the optimal region will be able to reflect the target wearout mechanism and degradation, enabling the construction of a model based on circuit failure data. With the accurate device-level wearout model parameters, a circuit designer can use the information to identify the dominant wearout mechanisms under the normal operation conditions and can design the circuit in a more robust and reliable fashion.

## Acknowledgement

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