Estimation of the Optimal Accelerated Test Region for FinFET SRAMs Degraded by Front-End and Back-End Wearout Mechanisms

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***Abstract*—Advanced FinFET SRAMs undergo reliability degradation due to various front-end and back-end wearout mechanisms. The design of reliable SRAMs benefits from accurate wearout models that are calibrated by accelerated test. With respect to testing, the accelerated conditions which can help separate the dominant wearout mechanisms related to circuit failure is crucial for model calibration and reliability prediction. In this paper, the estimation of optimal accelerated test regions for a 14nm FinFET SRAM under various wearout mechanisms is presented. The dominant regions for specific mechanisms are compared and analyzed for effective testing. It is observed that for our SRAM example circuit only bias temperature instability (BTI) and middle-of-line time-dependent dielectric breakdown (MTDDB) have test regions where their failures can be isolated, while the other mechanisms can't be extracted individually due to acceptable regions' overlap. Meanwhile, the SRAM cell activity distribution has a small influence on test regions and selectivity.**

Keywords—FinFET; SRAM; wearout; reliability; accelerated test

I. INTRODUCTION

Although device scaling and new emerging technologies, such as FinFETs, bring about modern circuits with smaller areas and better performance, severe reliability degradation due to various wearout mechanisms still needs to be considered carefully. Static Random Access Memory (SRAM) occupies most of the area of Systems-on-Chips (SoC). And because SRAMs are a significant fraction of SoCs and are very dense, it is especially important and challenging to ensure that SRAMs achieve reliability targets. Like all circuits, SRAMs suffer from front-end and back-end degradation, due to Bias Temperature Instability (BTI) [1] - [4], Hot Carrier Injection (HCI) [5], [6], Time Dependent Dielectric Breakdown (TDDB) [7] - [14], Electromigration (EM) [15], and Stress Migration (SM) [16]. TDDB includes front-end-of-line dielectric breakdown (GTDDB), middle-of-line dielectric breakdown (MTDDB), and back-end-of line dielectric breakdown (BTDDB). Since HCI can be detected by changing the operating frequency, it is not considered here.

This work focuses on the estimation of the optimal accelerated test region for a 14nm FinFET SRAMs under BTI, TDDB, EM, and SM. Finding an optimal accelerated test region enables the extraction of wearout model parameters from circuit data, rather than from only test structures.

This paper is arranged as follows. Section II summarizes the wearout models. Section III presents the methodology for evaluating the FinFET SRAM test regions for each individual wearout mechanism. Section IV contains the analyses of detectability/acceptability and selectivity for the wearout mechanisms. And, this paper concludes in Section V.

II. FRONT-END AND BACK-END WEAROUT MODELS

A. Bias Temperature Instability

BTI relates to the accumulation of interface traps in the channel. It increases the threshold voltages of the transistors. Positive bias temperature instability (PBTI) and negative bias temperature instability (NBTI) occur in nFET and pFET devices, respectively, when positive and negative gate-to-source voltages are applied to nFET and pFET devices, respectively. With the increase of the threshold voltage, the SRAM cell performance metrics change. The probability distribution of the time it takes for the performance metrics to degrade beyond a predefined threshold value is the cell lifetime distribution.

During BTI stress, the change of interface-trap states and dielectric-fixed charge causes the shift of device threshold voltages. The reaction-diffusion (R-D) model and trapping/detrapping (T-D) model have been proposed to explain the shift in threshold voltage [17], [18]. The R-D model describes the shift as a power law, i.e., t^n, where t is time, while the T-D model describes the shift as *log(t)*. Here the R-D model, which was validated with experimental measurements on 14nm FinFET technology, is adopted to calculate the degradation of an SRAM cell array. The expressions for the threshold voltage shift of pFET and nFET devices are [19]

$$\Delta V_{thp} = A_p V_g^{-m} e^{-E_a/k_B T} t^{n_p} \quad (1)$$

$$\Delta V_{thn} = A_n e^{(-\gamma \cdot V_g)} e^{-E_a/k_B T} t^{n_n} \quad (2)$$

where A_p, A_n, m, n_p, n_n, and γ are fitting constants. V_g is the gate stress voltage. The temperature dependence is modeled with the Arrhenius relationship, where E_a is the activation energy, T is temperature, and k_B is the Boltzmann constant. Unlike the previous T-D model, the intrinsic stochastic component and duty cycle dependence has not been determined for the RD FinFET model used in this work, and therefore, these components are not included in this study.

B. Time Dependent Dielectric Breakdown

For the TDDB mechanisms, when the electric field is applied to the dielectric material, progressive degradation of the dielectric will cause the formation of defects and conductive paths and will ultimately cause a short in the circuit which might lead to a functional failure. With the scaling of technology nodes, thinner dielectric materials lead to serious reliability issues. Severe leakage currents induced by TDDB cause performance degradation and the breakdown of circuits, including SRAMs.

The breakdown of a gate dielectric involves the development of defect sites (traps). When the trap density increases, a path from gate to channel starts to conduct a leakage current. When the leakage current is too large, the device can no longer function properly. The overall time-to-failure due to GTDDB depends on activity and temperature. For ultra-thin (less than 5 nm) gate dielectrics, the characteristic lifetime due to GTDDB can be modelled with [20],

$$\eta_G = A_{GTDDB}\left(\frac{1}{WL}\right)^{\frac{1}{\beta_{GTDDB}}}\frac{V^{a+bT}}{\alpha_{GTDDB}}e^{\left(\frac{c}{T}+\frac{d}{T^2}\right)} \tag{3}$$

where W and L are gate width and length, respectively, η_G is the time-to-failure for 63.2% of the sample devices, β_{GTDDB} is the Weibull shape parameter, α_{GTDDB} is the probability of stress, F is cumulative-failure percentile at use conditions, T is the testing temperature, V is gate voltage, and a, b, c, d and A_{GTDDB} are fitting parameters. The dielectric is under stress if the device is "on", i.e. the input is "1" and "0" for nFET and pFET devices, respectively.

Since the circuit supply voltage doesn't scale at the same rate as technology advances, the aggressive shrinking of the insulator between the conductors leads to a greater electric field in the dielectric. The characteristic lifetime due to BTDDB/MTDDB for each dielectric segment with vulnerable length L can be expressed as [21],

$$\eta_{B/M} = A_{B/M}\frac{L^{\frac{-1}{\beta_{B/M}}}}{\alpha_{B/M}}e^{-\gamma E^m}\cdot e^{\frac{E_a}{k_B T}} \tag{4}$$

where $\alpha_{B/M}$ is the stress probability, $\beta_{B/M}$ is the *Weibull* shape parameter, γ is the field acceleration factor, k_B is Boltzmann's constant, E_a is the activation energy, T is temperature, and E is the electric field through the dielectric segment which corresponds to $V/S_{B/M}$. V is the supply voltage and $S_{B/M}$ are supply voltage and the space between conductors. For MTDDB the conductors are a gate and a contact. $A_{B/M}$ is a constant which depends on dielectric material properties. m is 1 for the E model, and ½ for the $\sqrt{E}$ model. Here the $\sqrt{E}$ model is applied for BTDDB, and the E model is applied for MTDDB. The stress probability is the probability that the two conductors surrounding the dielectric are at different voltages. For MTDDB, this is the fraction of time when a gate voltage and the nearby contacts are different, and for GTDDB, this is the fraction of time when the nearby interconnects are at different voltages. These stress probabilities depend on the input patterns of the circuit and/or the application run on the microprocessor.

C. Electromigration

EM describes the process of metal atom migration under the traction of electric field applied to the interconnect. Along the direction of conduction, atoms migrate from cathode to anode. When the stress formed in metal lines exceeds a threshold value, the interconnect resistance starts to rise, which leads to circuit failure. It is predicted that EM is getting to be more significant for more advanced technology nodes involving FinFETs [22], [23].

The EM relevant mean time to failure (*MTTF*) of a metal line can be evaluated with Black's equation while considering the Blech limit [24], [25],

$$MTTF = Aj^{-n}\exp(E_a/k_B T) \tag{5}$$

$$(jL)_{crit} = \frac{\Omega\sigma_{crit}}{eZ^*\rho} \tag{6}$$

where A and n are fitting constants, j is the density of current flowing through the metal line, E_a is the activation energy, T is temperature, and k_B is the Boltzmann constant. Ω is the atomic volume, σ_{crit} is the critical stress for void formation, e is the electron charge, Z^* is the effective charge number, ρ is the metal wire electrical resistivity, and L is the length of metal wire between two vias.

The mean-time-to-failure (MTTF) of each segment is calculated based on the current density which flows through it. The current density is extracted from Hspice simulations for read/write operations together with the activity distribution. Since the current flowing through each segment is different, the product of j and L varies greatly within the SRAM array. For the jL larger than $(jL)_{crit}$, the MTTF calculated from j is kept for the estimation of the overall lifetime, while for the jL smaller than $(jL)_{crit}$, the corresponding segment is neglected because it is considered to be EM immortal.

For the wires which suffer bi-directional current stress, the effective current density for EM evaluation can be computed with [26], [27],

$$j_{eff} = \frac{1}{t_0}\left[\int_0^{t_0} j^+(t)\,dt - R\int_0^{t_0}|j^-(t)|\,dt\right] \tag{7}$$

where $j^+(t)$ and $j^-(t)$ are the time-dependent positive and negative current density, respectively, R is the EM recovery factor, and t_0 is the overall stress time.

D. Stress Migration

SM, which is introduced by the stress gradient with diffusion cause by heat, has a lower probability of occurrence for narrower lines with a fixed via size [28].

The MTTF due to SM is described with [16],

$$MTTF = AW^{-M}(T_0 - T)^{-N}\exp(E_a/k_B T) \tag{8}$$

where A is a fitting constant, W is the linewidth or plate size, M is the geometry stress component, T_0 is the stress-free temperature, N is the thermal stress component, E_a is the diffusion activation energy, k_B is the Boltzmann constant, and T is the testing temperature.

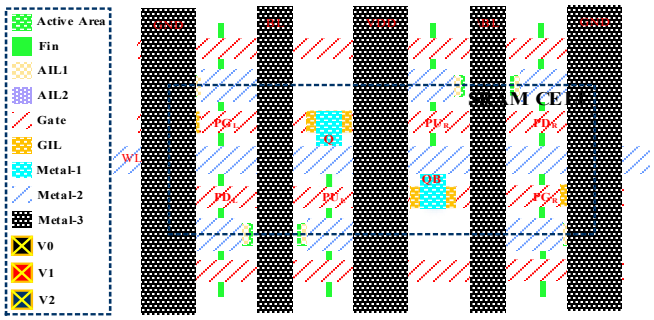


Fig. 1. Layout representation of a high-density 6-T SRAM cell with a single fin for each FinFET (1:1:1).

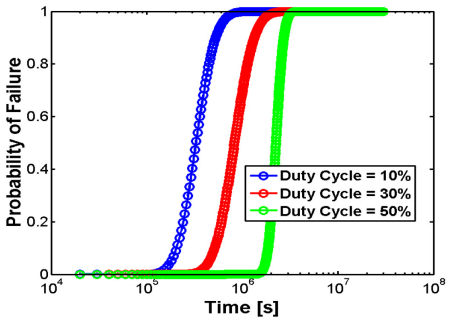


Fig. 2. The BTI induced probability of failure as a function of time for an SRAM cell under three different stress probabilities.

III. Circuit Reliability Assessment

In this section, the reliability degradation of a FinFET SRAM due to each wearout mechanism is analyzed separately. Many wearout mechanisms are a function of layout. Fig. 1 shows the basic layout of a high-density 6T FinFET SRAM cell. This layout is built with the NCSU FREEPDK15 library [29]. MOL layers include AIL1, AIL2, and GIL. BEOL layers include Metal1, Metal2, and Metal3. The other layers belong to the FEOL.

BTI induced lifetime is a function of degradation and is obtained as the time when performance metrics fall below a predefined performance criterion. Other mechanisms are assumed to cause opens (EM, SM) or shorts (TDDB). An open or short is assumed to cause a performance failure. They are modeled as time-to-failure distributions. The time-to-failure is computed for each feature using the models mentioned in the previous section. The time-to-failure of the SRAM cell is determined by the combined effects from individual layout components. In other words, the statistical distributions for individual components in the layout are combined to determine the overall lifetime of the full cell and/or circuit.

A. Assessment Methodology for Each Mechanism

With respect to BTI, the SRAM cells' lifetime distributions are evaluated based on the degradation of performance metrics, including the read static noise margin (SNMs), write margin, read current (IREAD), and minimum retention voltage (Vdd-min-ret). In order to model the lifetime and failure probability of an SRAM due to BTI, the lifetime distribution of cells under a specific stress duty cycle is firstly determined with Monte Carlo (MC) simulations [9]. In MC simulations, the die-to-die device channel length variation and within-die threshold voltage variation are considered. To calculate the threshold voltage shift, the duty cycle is used to obtain equivalent stress time in Eqs. 1 and 2. Fig. 2 shows an example of the BTI induced probability of failure which evolves with time for an SRAM cell with three different stress probabilities.

The lifetime distribution of a single cell then combines variation in duty cycle and process parameters. The resulting lifetime distribution of the cells is best fit with the Log-normal model. Then the overall expression of the time dependent failure probability for a full SRAM is a combination of the lifetime distribution of the cells, and is given by [30],

$$d_{bit,i}(t) = -ln\left(1 - F_{bit,i}(t)\right) \tag{9}$$

$$F(t) = 1 - exp\left(-\sum_{i=1}^{n} d_{bit,i}(t)\right) \tag{10}$$

where $F_{bit,i}$ is the cumulative failure probabilities due to each cell at each time point ($i=1, 2, \ldots, n$), $d_{bit,i}(t)$ is the number of reliability defects due to each cell at each time point, and $F(t)$ is the overall probability of failure as a function of time.

The lifetime distributions due to EM are also described as Log-normal distributions. First, the lifetime distributions of all features are computed, based on their current density and wire length. Since the failures due to EM are generally considered to occur in metal lines close to vias, via and interconnect segments are paired to calculate the lifetime parameters for layout features due to EM. Here, for a 32kb SRAM array, 82,513 features in the metal 3 (M3) layer were calculated. The via/interconnect pairs in metal 1 (M1) and metal 2 (M2) are neglected due to immortality because of the small current and the short wire length. These lifetime distributions are combined with equations (9) and (10) above.

Lifetime distributions due to TDDB and SM are described with the Weibull model. For GTDDB, MTDDB, and BTDDB, the lifetime parameters for each dielectric segment are computed. In the cell layout, there are 6, 13, and 4 dielectric segments for GTDDB, MTDDB, and BTDDB, respectively. For SM, the lifetime parameters are computed for each via. There are 16 vias in the cell layout. The Weibull characteristic lifetime of the SRAM lifetime distribution, η_{SRAM} due to each mechanism, is the solution of [31],

$$1 = \sum_{i=1}^{n} (\eta_{SRAM}/\eta_i)^{\beta_i} \tag{11}$$

where η_i, $i = 1,\ldots,n$ are the characteristic lifetimes of all the underlying components, and β_i, $i = 1,\ldots,n$ are the corresponding Weibull shape parameters.

Similarly, the overall shape parameter is the solution of [31],

$$\beta_{SRAM} = \sum_{i=1}^{n} \beta_i (\eta_{SRAM}/\eta_i)^{\beta_i} \tag{12}$$

The time-dependent overall probability of failure is calculated with

$$F(t) = 1 - \exp\left(-\left(\frac{t}{\eta_{SRAM}}\right)^{\beta_{SRAM}}\right) \tag{13}$$

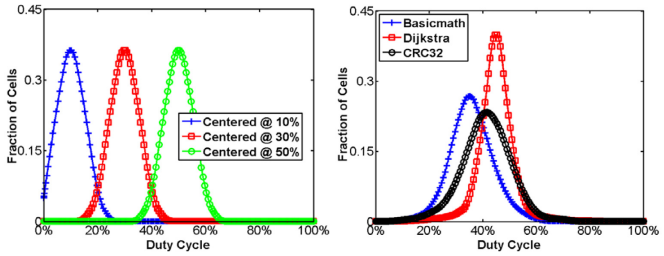
B. Probability of Failure and Detectability in the Test Domain

The lifetime of a commercial circuit is long (for example, >10 yrs). It is not possible to detect the expected time-to-failure

under normal operation conditions. Therefore, accelerated tests under higher voltage and higher temperature are performed to obtain and isolate the failures due to various wearout mechanisms. In this paper, we simulate the impact of accelerated stress on an SRAM array with 32 kb cells assuming a two week test time. In order to extract the wearout distribution of the SRAM, the SRAM is assumed to have failed when at least one cell has failed for each specific voltage-temperature condition within the two-week test time. This means that the overall probability of failure of the SRAM is approximately equal to the probability of failure of a cell times the number of cells, *N*. Therefore, a threshold value for the probability of failure of a cell of *1/N* is used to indicate SRAM failure. Appropriate test conditions are the voltage-temperature nodes with a probability of failure of a cell that is higher than *1/N*. In the two-dimensional test domain in the voltage and temperature space, the areas which have a failure probability higher than the threshold value are defined as the failure detectable region.

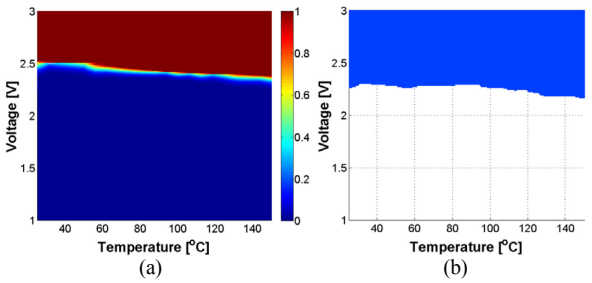
Failure rates are a function of the data stored in the cells. The duty cycle distribution of cells is set as a Gaussian distribution with a center of 30%, which is shown is Fig. 3(a). Such a distribution represents typical applications, as illustrated in Fig. 3(b). The SRAM is assumed to be operating at a frequency of 250 MHz.

Figs. 4-9 show the failure probability distribution and detectable region related to each wearout mechanism. The detectable regions overlap. Obviously, in the detectable regions, BTI and GTDDB lead to a much higher failure probability than the other mechanisms, which means they are more dominant mechanisms leading to circuit failure. On the other hand, since MTDDB has the largest detectable region, despite the relatively low probability of failure, it is easier to test and distinguish from other wearout mechanisms.



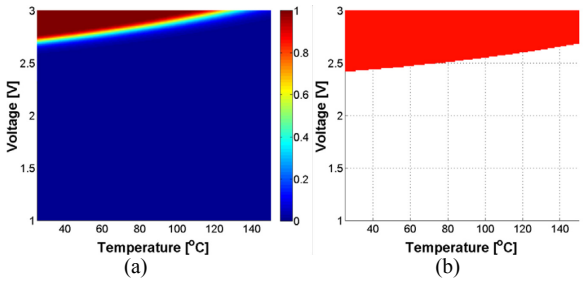
(a) (b)

Fig. 3. (a) The duty-cycle distributions centered at 10%, 30%, and 50%, respectively. (b) The duty-cycle distributions of SRAM cells in a 2-way 32KB data cache, while the microprocessor is running different benchmarks [32].



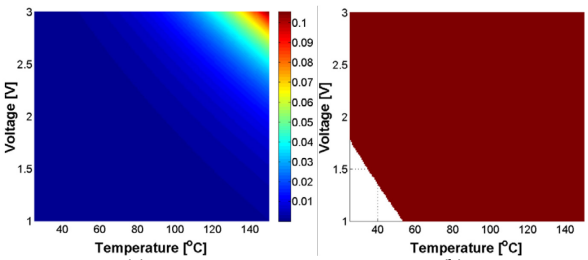
(a) (b)

Fig. 4. (a) The probability of failure distribution for an SRAM cell for BTI, and (b) the detectable test domain related to BTI.



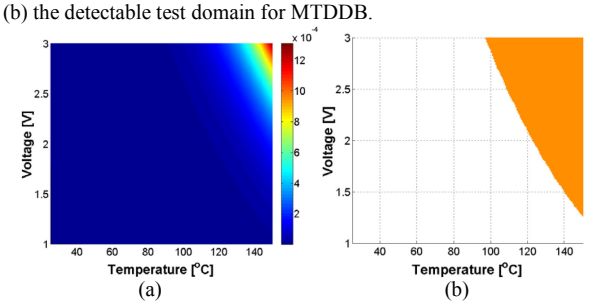
(a) (b)

Fig. 5. (a) The probability of failure distribution for an SRAM cell for GTDDB, and (b) the detectable test domain related to GTDDB.



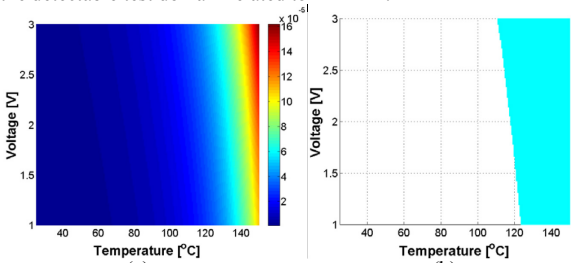
(a) (b)

Fig. 6. (a) The probability of failure distribution for an SRAM cell for MTDDB, and (b) the detectable test domain for MTDDB.



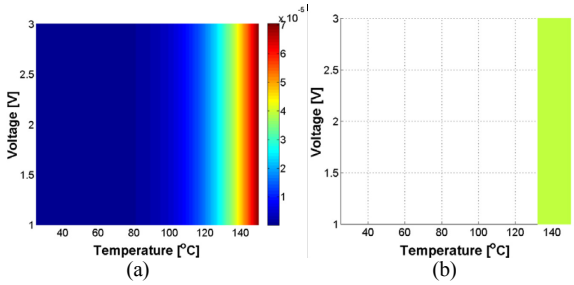
(a) (b)

Fig. 7. (a) The probability of failure distribution for an SRAM cell for BTDDB, and (b) the detectable test domain related to BTDDB.



(a) (b)

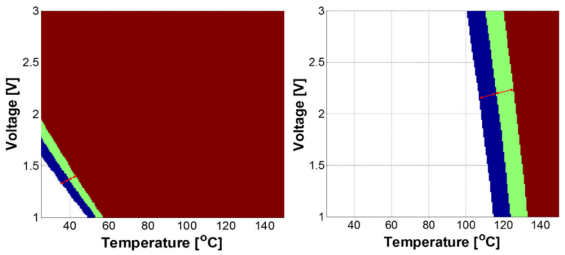
Fig. 8. (a) The probability of failure distribution for an SRAM cell for EM, and (b) the detectable test domain related to EM.



(a) (b)

Fig. 9. (a) The probability of failure distribution for an SRAM cell for SM, and (b) the detectable test domain related to SM.

The detectable test domain related to each mechanism changes as a function of the process corner. Process variation is



(a) (b)

Fig. 10. Boundary shift of the detectable test domain due to process variations related to (a) MTDDB and (b) EM.

modeled as die-to-die linewidth variation, which applied to both devices and interconnect. Fig. 10 shows the representative boundary shift of the detectable test domain related to MTDDB and EM. The three boundary lines correspond to -10%, nominal, and +10% process variations, respectively.

IV. Estimation of Optimal Test Regions

As mentioned in Section III, there are overlaps among the different detectable test regions. When a failure is detected under a specific test condition, it might be caused by more than one mechanism. In this section, the selectivity for individual mechanisms is used to identify the dominant one. If there is only one wearout mechanism for a specific test condition, then wearout parameters for that mechanism can be determined from circuit failure data without the use of failure analysis. Also, in this section, the effect of the duty cycle distribution on selectivity is analyzed. The impact of transition rate is not considered, since the current due to write operations is much smaller than that for read operations. Hence, the write currents do not contribute to EM [15].

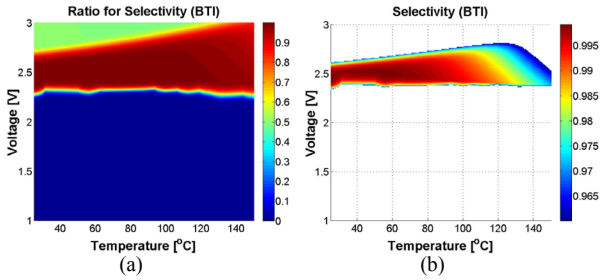
A. Selectivity

Selectivity identifies how easily one mechanism can be isolated from the others during accelerated life test. If selectivity is high, a reliability engineer knows the cause of failure with high confidence without further cost consuming testing and analysis. Here, the selectivity of one mechanism is quantified with the ratio of the probability of failure induced by it over the sum of probability of failure induced by all of the wearout mechanisms, as shown in Eq. 14.

$$S_i(t) = \frac{F_i(t)}{\sum_{i=1}^{N_m} F_i(t)} \tag{14}$$

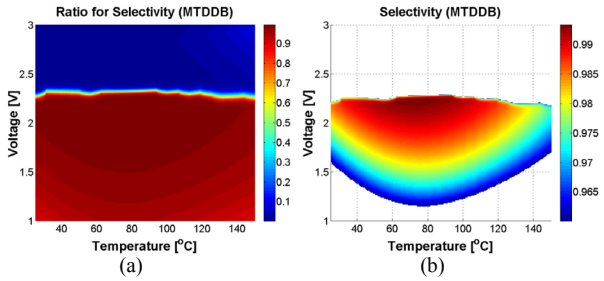
where N_m is the overall wearout mechanism number.

If the ratio is higher than 96%, a wearout mechanism is considered to be a dominant wearout mechanism. In Figs. 11 and 12, the ratio for selectivity of BTI and MTDDB are presented. Figs. 11(a) and 12(a) show the selectivity for the entire voltage-temperature domain. Figs. 11(b) and 12(b) show the parts of the voltage-temperature domain where selectivity is above 96% for BTI and MTDDB, respectively. Although the probability of failure due to MTDDB is relatively lower, the big size of the MTDDB detectable region ensures the existence of selectivity in the regions far away from regions where BTI and GTDDB dominate. The results for other mechanisms aren't shown because there are no regions where they can be isolated within the voltage-temperature domain.



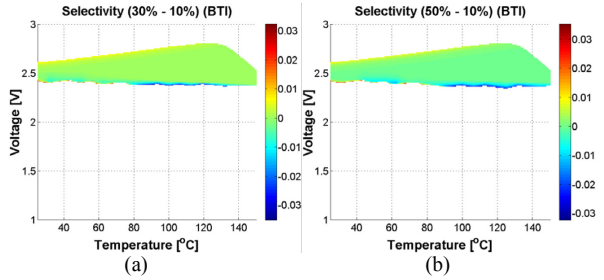
(a) (b)

Fig. 11. (a) The selectivity ratio for BTI for the FinFET SRAM, and (b) the area where the ratio is above 0.96.



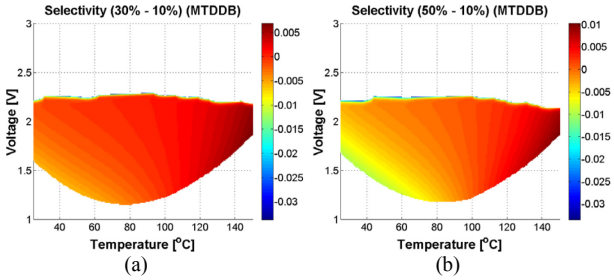
(a) (b)

Fig. 12. (a) The selectivity ratio for MTDDB for the FinFET SRAM, and (b) the area where the ratio is above 0.96.



(a) (b)

Fig. 13. The effect of the duty cycle distribution on selectivity for BTI, with (a) a distribution centered at 30% compared with the one centered at 10%, and (b) a distribution centered at 50% compared with the one centered at 10%.



(a) (b)

Fig. 14. The effect of the duty cycle distribution on selectivity for MTDDB, with (a) the distribution centered at 30% compared with the one centered at 10%, and (b) the distribution centered at 50% compared with the one centered at 10% (b).

B. Effect of the Duty Cycle Distribution

The effect of the duty cycle distribution on selectivity for BTI and MTDDB is shown in Figs. 13 and 14. The three duty cycle distributions were compared: centered at 10%, 30%, and 50%, respectively. In light of the comparison, although the shift in the duty cycle distribution leads to an increase or decrease in selectivity for both BTI and MTDDB in different regions in the voltage-temperature domain, the effect of the cell duty cycle distribution is small and negligible.

V. CONCLUSION

In this paper, the estimation of the optimal accelerated test regions for FinFET SRAMs in the presence of various wearout mechanisms is presented. The detectable region for each mechanism is determined. It is observed that BTI and MTDDB have a high probability of failure in their acceptable regions, while the other mechanisms have a relatively lower probability of failure. According to the result on selectivity, because of the existence of acceptable region overlaps, only BTI and MTDDB have significant test regions where circuit-level failure data can be isolated for each mechanism without failure analysis. In addition, the overall duty cycle distribution has a small influence on the test regions and selectivity.

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