Self-Aligned Capillarity-Assisted Printing of Top-Gate Thin-Film Transistors on Plastic

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Abstract

Top-gate thin-film transistors (TFTs) are fabricated on plastic using a self-aligned method based on capillarity-assisted lithography and inkjet printing, offering a promising platform for high-throughput manufacturing of flexible electronic devices. Plastic substrates are imprinted with a multi-tier structure containing capillary channels and ink receivers using a precision mold. Liquid inks are sequentially delivered to the microstructured substrate by inkjet printing, and capillary action draws the inks into a multi-tier capillary channel network designed for top-gate TFTs. The combination of imprinting, inkjet printing, and capillary flow yields self-aligned multi-layered devices without requiring precise registration for inkjet printing. The printed top-gate TFTs with Ag/Cu source and drain, poly(3-hexylthiophene) semiconducting channel, ion gel dielectric, and graphene gate electrode have desirable transfer and output characteristics, with a hole mobility of 0.48 $cm^2 V^{-1} s^{-1}$, threshold voltage of -0.86 V, on/off current ratio of $10^{4.5}$, and robust tolerance to bending. The top-gate geometry and careful materials selection yields devices with negligible hysteresis and sweep rate dependence, establishing the versatility and utility of this self-aligned strategy for more widespread application in printed and flexible electronics.

Keywords: thin-film transistor, top-gate structure, flexible electronics, inkjet printing, capillarity-assisted lithography

1. Introduction

Additive manufacturing based on printing processes facilitates the production of electronic devices with minimal materials waste, versatile form factor, and low cost. Due to these compelling advantages, significant research efforts have sought to develop printed electronics solutions for diverse application areas including displays, distributed sensing, smart packaging, and energy management [1-7]. In addition, printing processes are compatible with roll-to-roll production formats and flexible substrates, offering great promise for high-throughput manufacturing of bendable devices. These attributes have motivated widespread interest in roll-to-roll production of printed and flexible electronics in recent years [8-13].

Thin-film transistors (TFTs) are a fundamental building block of more complex electronic circuits and systems, and are thus a focal point for intensive research in both academia

and industry. Although considerable progress has accompanied research efforts in printing flexible TFTs [14-19], the translation of these achievements into a roll-to-roll manufacturing process remains challenging, in part because micrometer-level registration for printing multi-layered devices is impeded by the limited control over web speed and tension. To address this challenge, self-aligned processing methods have recently been proposed for printed TFTs utilizing surface energy patterning and capillarity-assisted lithography [20, 21]. Despite initial successes in TFT fabrication, however, these self-aligned methods require further research to improve device performance, to accommodate more complex and diverse device structures, and ultimately to extend the range of potential applications.

Capillary action of liquid inks within microfluidic channels has been exploited for high-resolution patterning and straightforward registration, enabling device fabrication without precise printing control [21-24]. Multi-tier capillary channel networks have enabled self-aligned fabrication of multi-layered electronic devices, including TFTs with a side-gate structure [21, 23]. Unlike conventional device structures with a gate electrode aligned over (top-gate) or underneath (bottom-gate) the semiconductor, side-gate TFTs have coplanar source, drain, and gate electrodes, simplifying the design of microfluidic channels for the capillarity-based strategy. Despite the processing benefits, these side-gate devices generally exhibit hysteresis and sweep rate dependence due to the extended spatial separation between the gate electrode and semiconductor [23, 25, 26]. These limitations hinder the development of complex integrated circuits and reduce the scope of potential applications [27], motivating the development of TFTs with an aligned-gate structure while retaining the benefits of the capillarity-assisted processing method.

Here we describe a strategy to print top-gate TFTs on plastic utilizing capillary action of liquid inks within microfluidic channels. In this process, known as self-aligned capillarity-assisted lithography for electronics (SCALE) [21], plastic substrates are imprinted with microfluidic channels and ink receivers by polydimethylsiloxane (PDMS) stamping. Functional liquid inks are then deposited into the receivers by inkjet printing, and transported into the channels by capillary action, resulting in self-aligned and high-resolution patterning of electronic devices with greatly relaxed printing tolerance. By engineering the multi-tier capillary channel networks and inks for the SCALE process, we demonstrate flexible top-gate TFTs with Ag/Cu source and drain, poly(3-hexylthiophene) (P3HT) semiconductor, ion gel dielectric, and graphene gate on polyethylene terephthalate (PET) substrates. The top-gate devices exhibit significantly reduced hysteresis and sweep-rate dependence, compared to the side-gate devices in recent SCALE work [21, 23]. Moreover, the flexible devices show good mechanical tolerance over repeated bending cycles.

2. Experimental Section

2.1 Si Master Mold Fabrication

A Si master mold was prepared with a Si wafer by three photolithography cycles (Figure S1, Supporting Information). For the first photolithography cycle, a 4-in Si wafer was pre-baked at 115 °C for 1 min, vapor-coated with hexamethyldisilazane for 3 min, and spin-coated with photoresist (Microposit S1813, Dow) at 2000 rpm for 30 s. After soft-baking at 115 °C for 1 min and UV exposure with a photomask using a mask aligner (MA6, Karl Süss), the wafer was submerged in a developer solution (Microposit 351, Dow) diluted with deionized water (1:5 v/v) for 40 s, and rinsed with deionized water. The features were then etched by reactive ion etching (320, Surface Technology Systems), followed by rinsing the photoresist with acetone, ethanol, isopropanol, and deionized water, sequentially. For the second photolithography cycle, the Si wafer was pre-baked at 200 °C for 5 min, vapor-coated with hexamethyldisilazane for 3 min, and spin-coated with photoresist (AZ 9260, MicroChemicals) at 300 rpm for 10 s and at 3000 rpm for 60 s, sequentially. After soft-baking at 110 °C for 165 s, the photoresist was exposed to UV light through a photomask. The wafer was immersed in a developer solution (AZ 400K, Merck Performance Materials) diluted with deionized water (1:4 v/v) for 4 min, and rinsed with deionized water. The features were then etched by reactive ion etching (SLR-770, Plasma-Therm), and the photoresist was rinsed with acetone, ethanol, isopropanol, and deionized water, sequentially. For the third photolithography cycle, photoresist (SU-8 2050, MicroChem) was spin-coated on the wafer at 500 rpm for 10 s and 2000 rpm for 30 s, sequentially, and soft-baked at 65 °C for 3 min and 95 °C for 9 min, sequentially. The photoresist was exposed to UV light through a photomask and post-baked at 65 °C for 2 min and 95 °C for 7 min, sequentially. The wafer was immersed in a SU-8 developer solution for 5 min and rinsed with isopropanol.

2.2 PDMS Stamp Fabrication

After silane-treatment of the Si master mold in a vacuum chamber with 0.2 mL of trichloro(1H,1H,2H,2H-perfluorooctyl)silane (Sigma-Aldrich) for 12 h, a mixture of PDMS monomer and its curing agent (10:1 w/w, Sylgard 184, Dow Corning) was poured onto the master mold and cured in an oven at 70 °C for 3 h. The PDMS stamp was peeled off from the master mold and post-cured in an oven at 120 °C for 2 h.

2.3 Imprinted Substrate Preparation

A UV-curable polymer (NOA-73, Norland Products) was poured on a PET film that was plasma-treated (PDC-32G, Harrick Plasma) for 3 min. The PDMS stamp was placed on

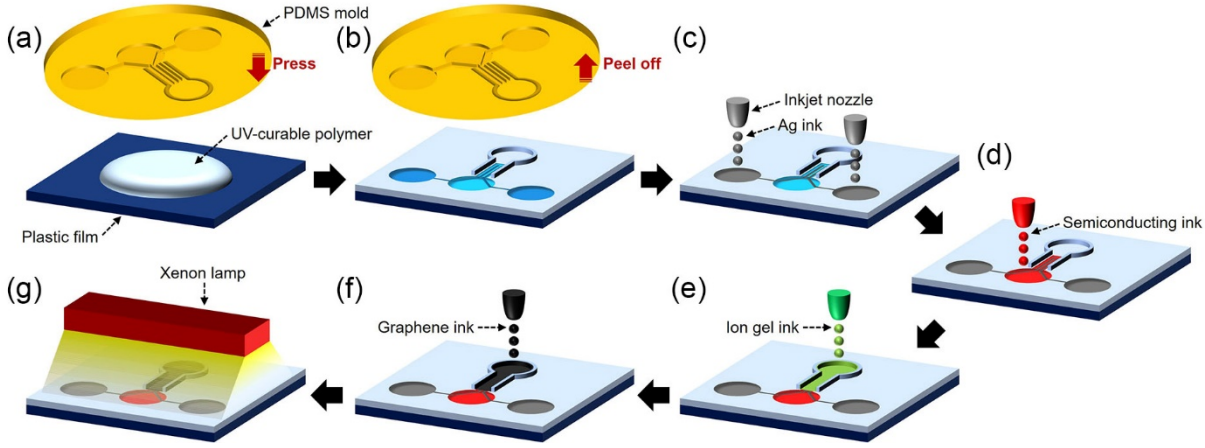

Figure 1. Fabrication steps for top-gate TFTs using the SCALE process. (a) UV-curable polymer was deposited on a plastic film and pressed by a PDMS stamp. (b) The stamp was peeled off from the polymer coating after UV curing. (c) A reactive Ag ink was inkjet-printed into the source and drain ink receivers, followed by Cu electroless plating (not shown). (d-f) Semiconducting P3HT, ion gel, and graphene inks were inkjet-printed into their respective receivers, and transported into the channels by capillary action. (g) The device was exposed to intense pulsed light of a xenon lamp.

the polymer coating and pressed by a roller to remove bubbles and obtain uniform coating. After curing the photopolymer by UV light (wavelength: 365 nm, LED SPOT 100, Dr. Hönle AG) for 90 s, the stamp was peeled off from the substrate.

2.4 Ag Printing and Cu Plating

After plasma treatment on the imprinted substrate for 1 min, a reactive Ag ink provided by Electroninks was inkjet-printed, and annealed at 100 ˚C. The sample was then submerged into a Cu electroless plating bath for 1 min, then removed and rinsed with deionized water. The bath contained 1.4 g of $CuSO_4 \cdot 5H_2O$ (J.T.Baker), 5.1 g of ethylenediaminetetraacetic acid disodium salt (Fisher Scientific), 1.6 g of NaOH (Mallinckrodt), 50 mL of deionized water, and 25 mL of formaldehyde (37% solution, VWR), and was heated on a hot plate at 55 °C.

2.5 Printing Semiconductor, Dielectric, and Gate

A semiconducting ink was prepared by dissolving P3HT (Rieke Metals, molecular weight: 50k–70k) in 1,2-dichlorobenzene (Sigma-Aldrich) at a concentration of 6 mg mL^{-1}. An ion gel dielectric ink was prepared by mixing poly(styrene-*b*-ethyl acrylate-*b*-styrene) (SEAS), 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide, ([EMIM][TFSI], EMD Chemicals), and *n*-butyl acetate (Sigma-Aldrich) at a ratio of 2:8:90 (w/w/w). A graphene ink was prepared for inkjet printing with the SCALE process by adapting previously established methods [28]. High shear mixing was used to exfoliate pristine graphene from flake graphite, using ethyl cellulose as a polymer dispersant. In a typical batch, ethanol (1 L), ethyl cellulose (10 g, Sigma-Aldrich, 4 cP grade), and flake graphite (200 g, Asbury Graphite Mills, Grade 3061) were mixed with a rotor-stator high shear mixer (2 h at 10230 rpm, Silverson L5M-A, square hole screen). Large particles of graphite were then removed by centrifugation at 7500 rpm for 5 min, followed by 4000 rpm for 105 min (Beckman Coulter J26 XPI centrifuge with a JS7.5 rotor). The supernatant was collected, containing dispersed graphene flakes, ethyl cellulose, and ethanol. The supernatant was then mixed with salt water (0.04 g/mL NaCl in deionized water) at 9:16 w/w, leading to flocculation of the graphene flakes and dispersant. These components were collected by centrifugation at 7500 rpm for 6 min, washed with deionized water, collected by vacuum filtration, and dried to yield a graphene/ethyl cellulose powder containing ~50% wt. graphene. The ink contained this graphene/ethyl cellulose powder (30 mg mL^{-1}) in a solvent mixture containing cyclohexanone, terpineol, and diethylene glycol methyl ether (Sigma-Aldrich) at a ratio of 14:3:3 (v/v/v). The ink was filtered at 3.1 µm prior to use in inkjet printing. The inks were delivered to the receivers using a custom-built drop-on-demand inkjet printer with an 80 µm diameter nozzle (MJ-AT-01, MicroFab): 20 drops for the source and drain, 10 drops for the semiconductor, 200 drops for the dielectric, and 150 drops for the gate. For all the inkjet printing, a unipolar waveform (rise/dwell/fall time: 5/30/5 µs) was used at a drive voltage and frequency of 120 V and 1 kHz, respectively.

2.6 Photonic Annealing

The printed graphene for the gate electrode was exposed to a high-intensity pulsed xenon lamp (wavelength: 200–1100 nm) in a photonic annealing system (Sinteron 2010, Xenon Corp.). The graphene was annealed with two flash pulses

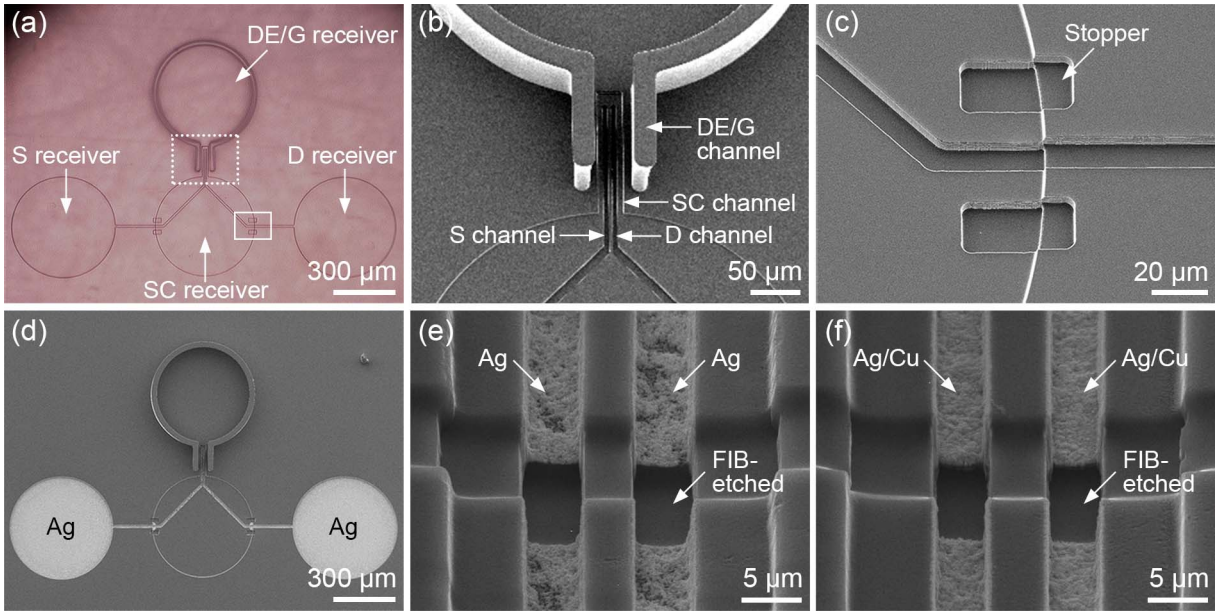

Figure 2. (a) Optical image of an imprinted plastic substrate. (b) SEM image of the central TFT region, denoted by the dotted box in (a). (c) SEM image of the stopper region, marked by a solid box in (a). (d) SEM image of Ag patterned in source and drain channels. (e) FIB cross-section of the Ag source and drain electrodes in the TFT region. (f) FIB cross-section of the source and drain electrodes following Cu electroless plating. S, D, SC, DE, and G indicate source, drain, semiconductor, dielectric, and gate, respectively.

(width: 500 μs, period: 5 s) at a lamp voltage of 3 kV, delivering an optical energy of 1.66 J cm^{-2} for each pulse.

2.7 Characterization

Prepared substrates and devices were imaged using a digital microscope (KH-7700, Hirox) and scanning electron microscopes (JSL-6500, JEOL and Quanta 200 3D, FEI). Shear viscosities of the graphene, reative Ag, ion gel, and P3HT inks were measured using a rheometer (AR-G2, TA instrument) with a 40 mm, 2° steel cone and plate geometry at a temperature of 23°C. Contact angles of the graphene and conducting polymer inks on the ion gel were measured using a drop shape analyzer (DSA-30, KRÜSS). Transfer and output characteristics of the TFTs were measured using a source meter (237, Keithley) and an electrometer (6517A, Keithley). Quasistatic behavior of inverters was characterized using source meters (237 and 2612B, Keithley) and an electrometer (6715A, Keithley). All characterization of devices was performed in a N_2 glovebox at room temperature, following annealing at 120 °C for 30 min.

3. Results and discussion

Figure 1 depicts a schematic diagram for the fabrication of top-gate TFTs by the SCALE process (details in the Experimental section). Capillary channels and ink receivers are first imprinted on a PET film with a PDMS stamp and UV-curable polymer coating. The PDMS stamp was prepared from a Si master mold in which capillary channels and receivers were created by photolithography (Figure S1, Supporting Information). The UV-curable polymer was applied on a plasma-treated PET film and pressed by the PDMS stamp (Figure 1a). Following curing of the polymer, the PDMS stamp was removed to form capillary channels and receivers on the plastic substrate (Figure 1b). The PDMS stamp can be used repeatedly to prepare additional imprinted substrates until it is contaminated by the photopolymer or dust particles. After the imprinted substrates were plasma-treated to increase the surface energy and consequently enhance the capillary flow in the channels, inks were delivered to the receivers by inkjet printing. For source and drain electrodes, a reactive Ag ink was printed to source and drain ink receivers (Figure 1c) [29], and Cu electroless plating was performed to produce thicker, more conductive electrodes and to facilitate more conformal contact of the source and drain electrodes with the semiconductor [21]. For semiconductor and dielectric, the P3HT and ion gel inks were printed into the semiconducting (Figure 1d) and dielectric (Figure 1e) ink receivers, respectively. For a gate electrode, a graphene ink was printed to the gate ink receiver (Figure 1f) and photonically annealed using intense pulsed light from a xenon lamp (Figure 1g). The inks used were prepared with a low viscosity (1 ~ 20 mPa·s, Figure S2, Supporting Information) for inkjet printing and strong capillary action. The inks filled the capillary channels in a few seconds after inkjet printing.

Figure 2a displays an optical image of the capillary channel and ink receivers imprinted on the plastic substrate. One device structure contains four circular ink receivers (diameter:

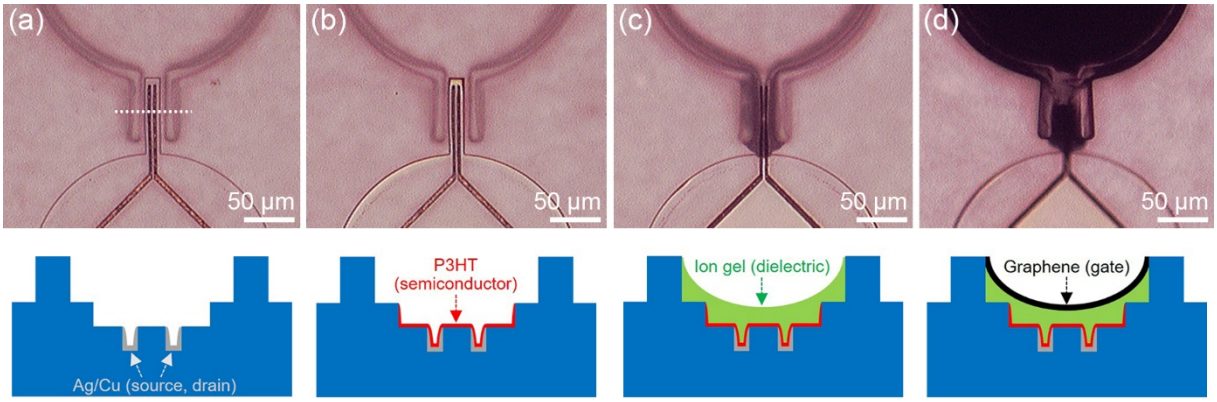

Figure 3. Optical images (top) for the device fabrication steps and their corresponding schematic illustrations (below) in a cross-sectional view after (a) Ag printing and Cu plating for source and drain electrodes, (b) depositing of P3HT ink for semiconductor, (c) printing an ion gel ink for dielectric, and (d) depositing a graphene ink for the gate electrode. The cross-sections are taken along the dotted line in (a).

500 µm) to deliver the inks for source (left in the optical image), drain (right), semiconductor (middle bottom), and dielectric and gate (middle top). The receivers feed into multi-tier capillary channels that guide the functional inks to produce a top-gate TFT. Figure 2b shows a tilted scanning electron microscopy (SEM) image for the capillary channel network in the central region (dotted box in Figure 2a). The network in the TFT region comprises four capillary channels: two channels (width: 5 µm, depth: 3 µm) for source and drain, one channel (width: 30 µm, depth: 2 µm) for semiconductor, and one raised wall channel (width: 50 µm, height: 70 µm) for dielectric and gate. In the TFT region, the source and drain channels are depressed within the semiconductor channel, and the dielectric/gate channel surrounds the semiconductor channel. Moreover, rectangular depression patterns (stoppers, Figure 2c) are incorporated in the semiconductor receiver (solid box in Figure 2a) to prevent undesirable source and drain ink flow, as discussed below.

Upon printing the reactive Ag ink to the receivers for source and drain electrodes, the ink was wicked into the adjoining channels by capillary action. With no stopper present, as the ink crossed over the edge of the semiconductor receiver, it exhibited a secondary capillary flow along the semiconductor receiver edge, in addition to the primary flow through the channels. This resulted in short circuits between the source and drain electrodes along the circular edge of the semiconductor receiver (Figure S3a, Supporting Information). Stoppers were introduced to address this, whereby rectangular depressions obstructed the ink flow along the edge by pinning the advancing contact line of the liquid (Figure S3b,c, Supporting Information). By managing the undesired flow in the complex capillary channel network, source and drain electrodes could be reliably patterned without shorting defects (Figure 2d). Figure 2e shows a focused ion beam (FIB) cross-section of the Ag electrodes in the TFT region. The Ag layer coated both the sidewalls and bottom of the channel, indicating that the ink nearly filled the channel during capillary flow. In addition, the electrodes were patterned with a resolution equivalent to the channel width (5 µm), which is higher than typical inkjet printing resolution (≥ 20 µm). After annealing the Ag ink, the substrate was submerged in a Cu electroless plating bath to develop a thin Cu coating on the Ag electrodes. Because the Ag patterns obtained with the reactive Ag ink are free from significant organic residue, the Ag electrode surface served as a good seed layer for Cu electroless plating. The FIB cross-section (Figure 2f) shows the Cu-plated electrodes that are thicker and more uniform than the Ag layer alone (Figure 2e).

On the substrate with the source and drain electrodes (Figure 3a), a P3HT (p-type semiconducting polymer) ink was printed into the semiconducting ink receiver. When delivered to the receiver, the P3HT ink filled the adjoining semiconductor channel by capillary action, and coated the source and drain electrodes in the semiconductor channel after solvent evaporation (Figure 3b). The P3HT ink was prepared with a high boiling point (BP) solvent, 1,2-dichlorobenzene (BP: ~180 °C) to retard solvent evaporation and consequently improve capillary action in the open channels. Moreover, the ink concentration was tailored to obtain the semiconductor thickness (~50 nm) optimal for the electrolyte-gated TFTs [30]. For the dielectric, an ion gel ink consisting of a gelling triblock copolymer (SEAS) and an ionic liquid ([EMIM][TFSI]) was printed into the dielectric/gate receiver [31]. When delivered to the receiver, the ink flowed into the raised wall channel by capillary action (Figure 3c), and covered the semiconductor and source/drain electrodes in the TFT region (Figure S4, Supporting Information). For the ion gel layer to be thick enough to avoid shorting between the semiconductor and gate, the dielectric channel was designed with the relatively large depth (70 µm).

To form a gate electrode (Figure 3d), a graphene ink was deposited in the dielectric/gate receiver. The graphene ink

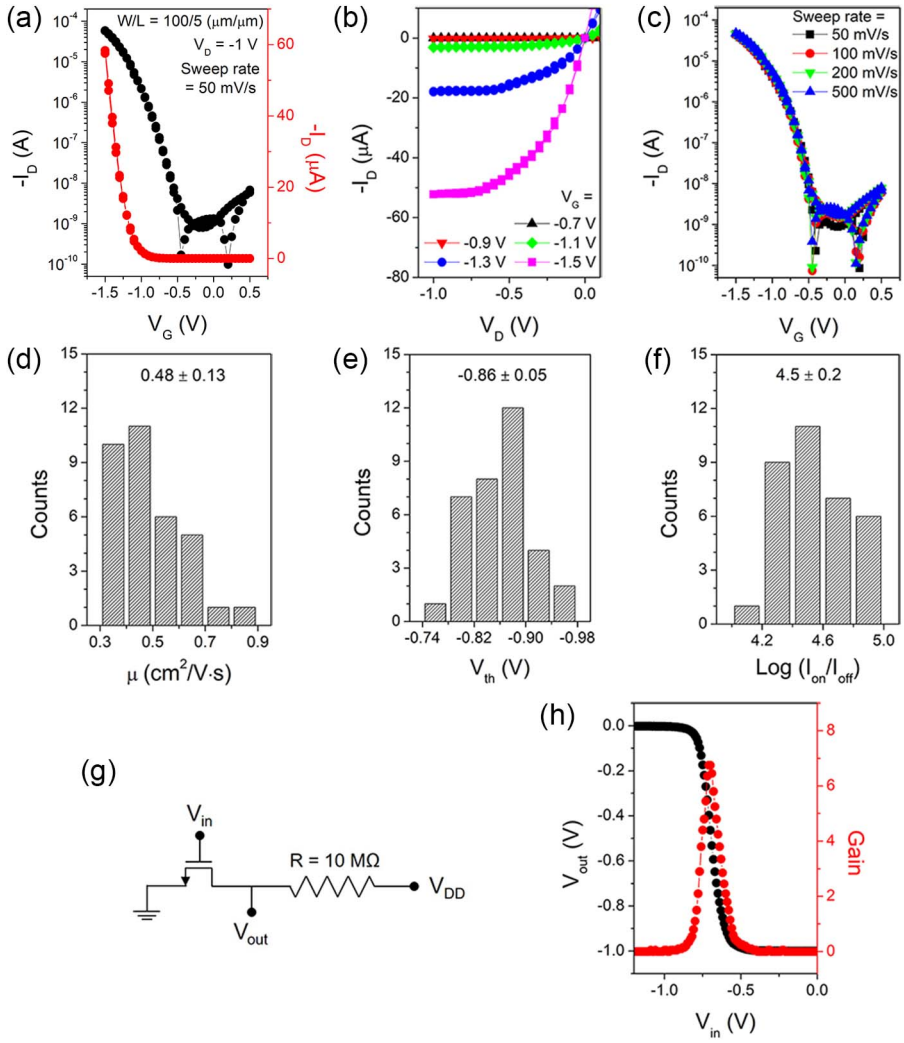

Figure 4. (a,b) Representative transfer and output characteristics, respectively, for the top-gate TFTs. The TFT channel width (W) and length (L) were 100 and 5 μm, respectively. (c) Transfer curves obtained upon increasing the gate voltage sweep rate from 50 to 500 mV s^{-1}. The transfer curves were obtained with a drain voltage (V_D) of -1 V. (d-f) Histograms showing charge carrier mobility (μ), threshold voltage (V_{th}), and on/off-current ratio (I_{on}/I_{off}), respectively. (g,h) Diagram and quasi-static behavior of a resistor (10 MΩ)-loaded inverter. The source was grounded and the drain supply voltage (V_{DD}) was -1 V.

(details in the Experimental Section) was formulated for slow evaporation and good wettability on the ion gel by modifying the previously demonstrated graphene ink preparation protocol [28]. The good wettability is critical to induce capillary flow of the graphene ink in the dielectric/gate channel pre-coated with the ion gel. Compared to the aqueous conducting polymer ink (poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) or PEDOT:PSS with contact angle on the ion gel of 94.5° ± 2.0°) commonly employed for a gate electrode in electrolyte-gated TFTs [30, 32], the graphene ink presents improved wettability on the ion gel, with a low contact angle of 13.2° ± 0.9° (Figure S5, Supporting Information). As a result, when delivered to the receiver, the graphene ink flowed well into the dielectric/gate channel by capillary action and completely covered the ion gel in the TFT region (Figure S6, Supporting Information). The sample was then irradiated with the intense pulsed light of a xenon lamp to remove the polymer stabilizers in the printed graphene and thereby enhance the electrical conductivity of the gate electrode.[24] The photonic annealing method was selected over typical thermal annealing methods (≥250 °C for ≥30 min) to avoid damage of the polymer semiconductor by the annealing temperature [28]. In addition, this photonic annealing method facilitates much faster post-treatment (<30 s, details in the Experimental section) of the graphene ink without damaging the transparent plastic substrate and organic semiconductor underneath the black graphene layer, compared to the thermal annealing methods.

Figure 4a,b display the representative transfer and output characteristics of the fabricated top-gate TFTs, respectively. The devices exhibit a negligible hysteresis between forward and backward sweeps in the transfer curve, and good linear

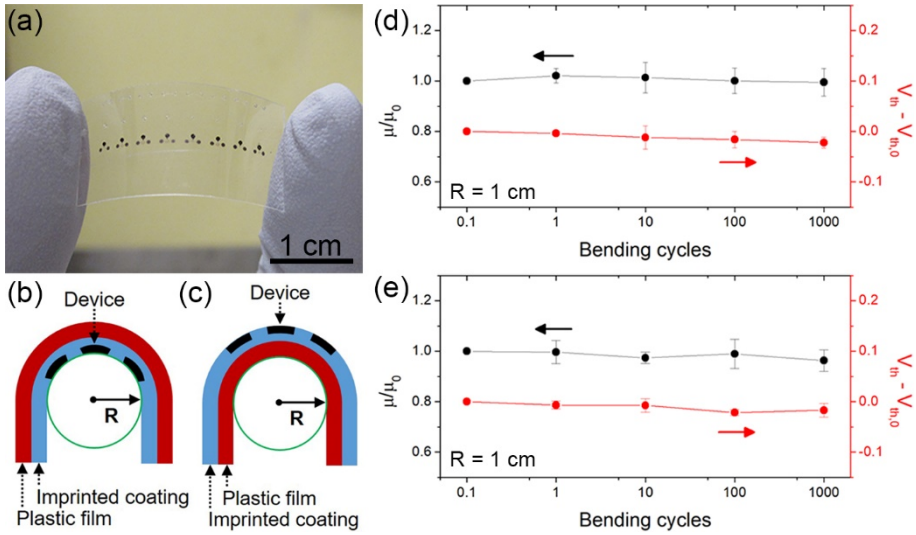

Figure 5. (a) Photograph of 8 TFTs fabricated on a PET film. (b,c) Schematic illustrations for compressive and tensile bending tests, respectively. Relative mobility (μ/μ_0) and threshold voltage change (V_{th} - $V_{th,0}$) over 1000 cycles of bending the devices (d) inside and (e) outside the substrate. The bending radius (R) for the tests was 1 cm.

and saturation behavior at low and high drain voltage in the output curve. Importantly, the devices exhibited no significant variation in transfer characteristics upon accelerating the sweep rate from 50 to 500 mV s^{-1}, as shown in Figure 4c. The hysteresis ($V_{th,\text{backward}} - V_{th,\text{forward}}$) of the top-gate devices was calculated based on threshold voltages (V_{th}) for the forward and backward sweeps in the transfer curves, and is compared with that of the side-gate devices prepared with the SCALE process in recent work [21, 23], as shown in Figure S7 (Supporting Information). The top-gate devices exhibit much smaller hysteresis compared to the side-gate devices, which can be attributed to the faster response of the electrolyte ions by more effective gating.

To evaluate the statistical distribution of device metrics, 40 devices were fabricated in 5 different batches (8 devices × 5 batches). 85% (34 out of 40) of the fabricated devices were functional, but the device failure arose mostly from the impediment to capillary action by dust particles on the substrate surface, leading us to expect improved yield when processing in a cleanroom. Furthermore, considerable batch-to-batch variability was not observed (Figure S8, Supporting Information). Figure 4d-f display the device metrics for the functional devices; the charge carrier mobility (μ), V_{th}, and on/off current ratio (I_{on}/I_{off}) were measured to be 0.48 ± 0.13 $cm^2V^{-1}s^{-1}$, -0.86 ± 0.05 V, and $10^{4.5\ \pm\ 0.2}$, respectively. The mobility and threshold voltage were calculated from plots of the square-root drain current ($I_D^{1/2}$, Figure S9, Supporting Information) as a function of gate voltage (V_G), based on the standard saturation regime relation (Equation (1))

$$I_D = \mu C_i \frac{W}{2L}(V_G - V_{th})^2 \quad (1)$$

in which the TFT channel width (W) and length (L) were 100 and 5 μm, respectively, and the specific capacitance (C_i) of the ion gel dielectric was estimated to be 23 μF cm^{-2} by displacement current measurements (Figure S10, Supporting Information) [33, 34]. In addition, resistor-loaded inverters were demonstrated with an external resistor (10 MΩ), as shown in Figure 4g-h. The inverters exhibited good conversion of high/low input voltage (V_{in}) to low/high output voltage (V_{out}) with a maximum gain (dV_{out}/dV_{in}) of ~6.8.

To assess the mechanical stability of the devices (Figure 5a), a bending test was performed with two different bending modes: bending the devices inside (Figure 5b, compressive strain: -0.7%) and outside (Figure 5c, tensile strain: 0.7%) the substrate (thickness: ~130 μm, 100 μm for the PET film and ~30 μm for the polymer coating) at a bending radius (R) of 1 cm. Figure 5d,e show the change in device performance (μ and V_{th}) during the test for compressive and tensile bending, respectively. Over 1000 bending cycles, μ was reduced by less than 4% (100% - μ/μ_0), and V_{th} was shifted by about -0.02 V ($V_{th} - V_{th,0}$) from their initial values (μ_0 and $V_{th,0}$), regardless of the bending direction. The minor change in device metrics upon bending supports the suitability of these top-gate TFTs for flexible applications.

4. Conclusion

In summary, we have fabricated top-gate TFTs on plastic using a self-aligned process based on capillarity-assisted lithography, known as SCALE. Plastic substrates were imprinted with engineered capillary channels and ink receivers, with inks subsequently deposited into the microstructured receivers by inkjet printing. The capillary action of the functional fluid inks in the microfluidic channels facilitated the self-aligned fabrication of high resolution, top-gate TFTs without precise registration. The devices fabricated

with a P3HT semiconducting channel and an ion gel dielectric exhibited μ of 0.48 cm^2 V^{-1} s^{-1}, V_{th} of -0.86 V, and I_{on}/I_{off} of $10^{4.5}$. Importantly, the top-gate devices showed significantly reduced hysteresis and sweep rate dependence from 50 to 500 mV s^{-1}, compared to results in recent SCALE reports with side-gate structures [21, 23]. Furthermore, the flexible devices showed good mechanical tolerance over repeated bending cycles. Overall, this work advances a promising strategy to print top-gate electronic devices utilizing capillarity for high-throughput manufacturing of printed and flexible electronics.

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Supporting Information

Self-Aligned Capillarity-Assisted Printing of Top-Gate Thin-Film Transistors on Plastic

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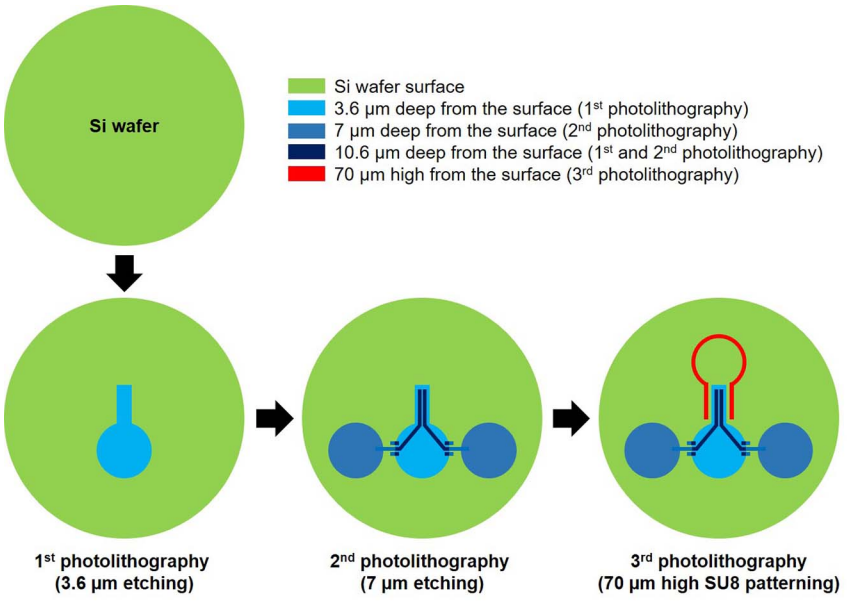

Figure S1. Schematic diagram for the preparation of a master mold with a Si wafer by a photolithography process. Different colors indicate different depths of the etched patterns from the top surface of the Si wafer.

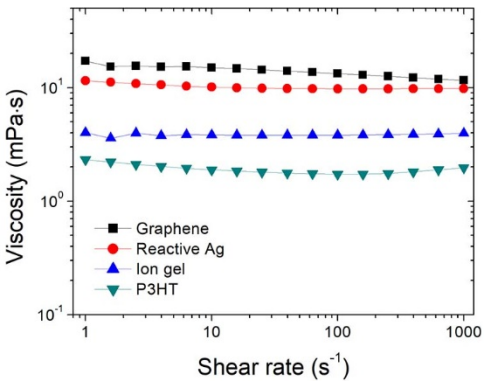

Figure S2. Shear viscosities of the graphene, reactive Ag, ion gel, and P3HT inks.

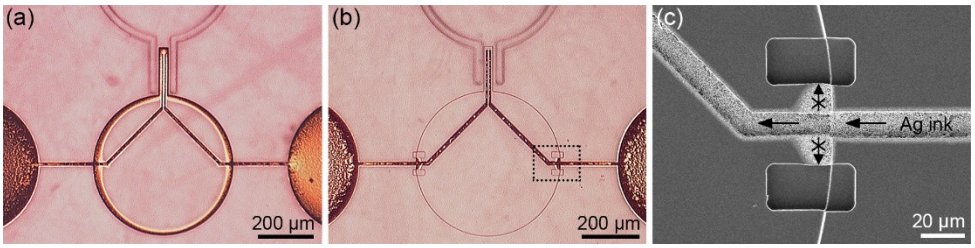

Figure S3. Optical images of Ag patterned for source and drain electrodes on imprinted substrates (a) without and (b) with stoppers. (c) SEM image of the dotted box in (b). The arrows in (c) indicate the direction of the Ag ink during the capillary flow.

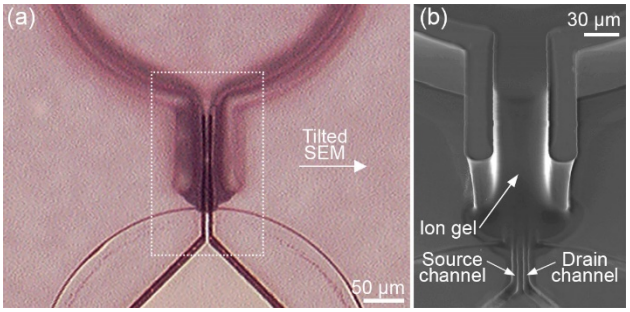

Figure S4. (a) Optical image of the device after depositing the ion gel dielectric. (b) Tilted SEM image of the box in (a).

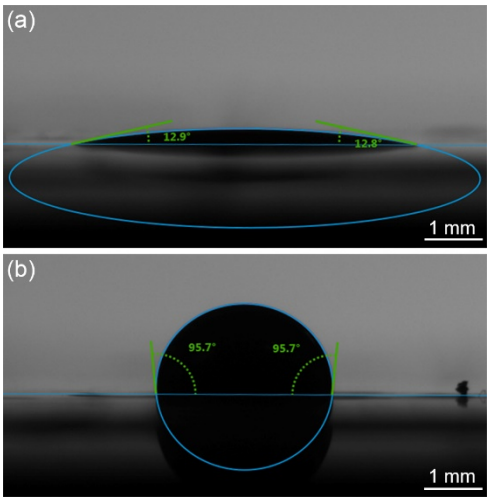

Figure S5. Optical images of contact angle measurement for (a) graphene and (b) PEDOT:PSS inks on an ion gel surface.

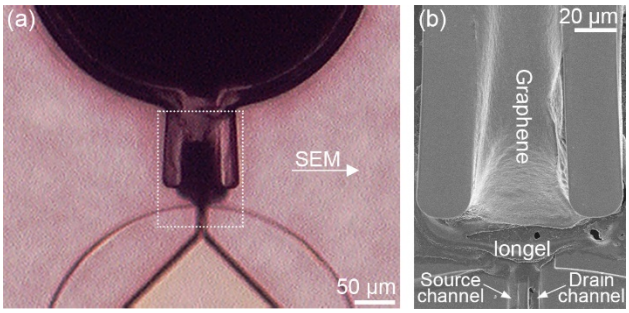

Figure S6. (a) Optical image of the device after depositing the graphene gate electrode. (b) SEM image of the box in (a).

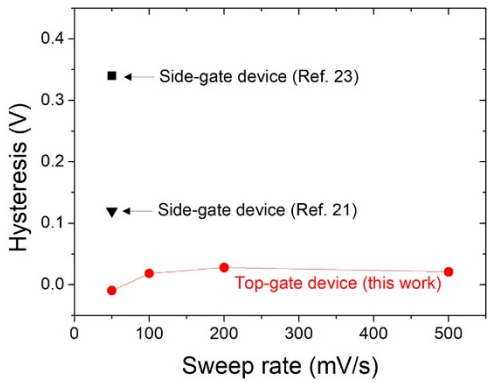

Figure S7. Comparison of hysteresis for top-gate and side-gate TFTs prepared with the SCALE process. The hysteresis was calculated based on threshold voltages (V_{th}) of the forward and backward scans, which is $V_{th,\text{backward}} - V_{th,\text{forward}}$.

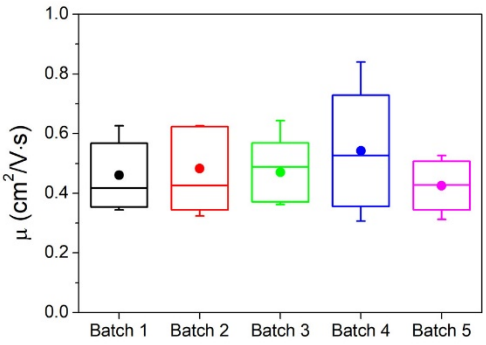

Figure S8. Box plot of mobility for the devices fabricated in 5 different batches, showing little batch-to-batch variability. A one-way analysis of variance (ANOVA) test confirms that batch differences are not a significant source of mobility variation, with a p-value of 0.56.

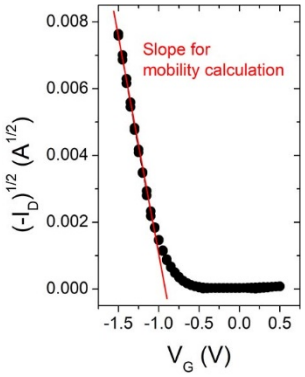

Figure S9. Square-root drain current ($I_D^{1/2}$)-gate voltage (V_G) characteristic for the mobility calculation.

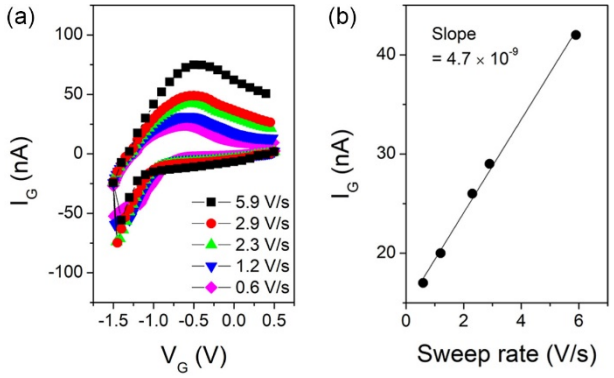

Figure S10. (a) Gate current (I_G)-gate voltage (V_G) characteristics measured at various sweep rates. (b) Plot of I_G as a function of the sweep rate at V_G = -1 V. The specific capacitance of the ion gel gate dielectric was obtained from the slope of the plot divided by the semiconductor area.