The Effects of Hydrogen Iodide Back Surface Treatment on CdTe Solar Cells

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An appropriate electrical back contact in CdTe solar cells is crucial to achieving high power conversion efficiency. In this work, a facile back surface treatment method for CdTe solar cells using hydroiodic acid (HI) is developed, and the effects of HI etching on the CdTe surfaces investigated. The electrical properties of the CdTe absorber and interfaces are characterized by current–voltage, capacitance–voltage, admittance spectroscopy, and complex capacitance spectroscopy measurements. The HI-etched devices show slightly higher apparent carrier concentrations than the control devices, suggesting an increased copper doping in the CdTe absorber. The potential barrier height of the back contact is reduced from 0.430 to 0.368 eV after the HI-treatment, accompanied by reduced contact resistance and carrier recombination. Additionally, the HI-treatment eliminates a defect signature at 0.409 eV. The HI-treatment effects lead to improved power conversion efficiency through enhancement of the fill factor, the short circuit current, and open circuit voltage.

1. Introduction

Thin-film polycrystalline CdTe solar cells have been intensively studied since the first CdTe-based heterojunction device was demonstrated in 1963.[1] After tremendous efforts over the past few decades, the record power conversion efficiency (PCE) has been improved to 22.1%, as reported by First Solar.[2] With high PCE and low fabrication costs, CdTe solar cells have become competitive with conventional crystalline silicon photovoltaic (PV) technologies.

Developing a suitable electrical back contact for CdTe solar cells is crucial for achieving high PCE. The high electron affinity of CdTe presents a challenge to forming a low-resistance ohmic back-contact for CdTe solar cells due to the lack of suitable electrode materials with sufficiently high work functions to match CdTe. Consequently, a performance-limiting back-junction barrier typically exists in most CdTe solar cells.[3] A common method to reduce the back-barrier height and achieve high PCE is to introduce Cu at the back surface to create a region of Cu_xTe alloy with a reduced electron affinity.[4,5] A Te-rich CdTe layer is highly preferable for effective Cu alloying and Te is commonly used in the back contact material stack to reduce the barrier height.[6] Wet-chemical etching has been widely used to produce such a Te-rich surface as well as to remove various oxides and/or chlorides that may form at the CdTe surface during device processing, such as the cadmium chloride ($CdCl_2$) mediated heat treatment procedure that is used to improve the electronic quality of the CdTe material. A variety of etching agents have

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been used to fabricate efficient CdTe solar cells, including nitric/phosphoric-based acid (NP), potassium dichromate sulfuric acid (KD), and bromine in methanol (BM).[7–10] However, these etching agents contain toxic and/or hazardous materials which are not desirable due to manufacturing safety concerns. NPs are strong etchants that require careful control of the treatment time and etchant concentration, otherwise they may introduce shunting pathways in the CdTe films resulting in device failure.[11] Alternatively, a TeO_2 surface layer can be formed after KD etching treatment that reduces the electrical conductivity of the back contact.[8] Bromide is an alternative method for chemical etching at CdTe, but storage and etching procedures should be performed carefully due the high activity of bromide.[8] Alternatively, a Te-rich layer can also be formed by close space sublimation (CSS) or evaporation of elemental Te onto the CdTe surface, but the potential formation of toxic TeO_2 gas during the deposition at high temperature is a concern.[12] Recently, a methylammonium iodide (MAI) in isopropanol solution was developed as a promising route for fabricating high-PCE CdTe solar cells.[13] However, an additional annealing procedure in inert atmosphere is needed for the MAI treatment, and MAI is not currently produced at sufficient scale to be considered economical for application in large scale CdTe solar cell production. So, developing a new environmentally friendly, or "green" etching processes still deserves attention.

In this work, we report on another facile and "green" chemical process to etch the back surface of CdTe using diluted hydroiodic acid (HI) in methanol. The treatment removes the back surface oxides and/or chlorides commonly formed during the $CdCl_2$ annealing treatment and forms a Te-rich back surface. We studied the impacts of HI etching on the electrical properties of CdTe films and device performance using temperature-dependent current voltage (*J–V–T*), temperature-dependent capacitance voltage (*C–V–T*), thermal admittance spectroscopy (TAS), and temperature-dependent complex capacitance spectroscopy measurements. We found that HI etching can moderately increase the carrier (hole) concentration in CdTe, reduce the potential barrier height and the effective resistance of the electrical back contact, suppress certain defects and recombination mechanisms, and consequently, lead to the improved device performance of CdTe solar cells.

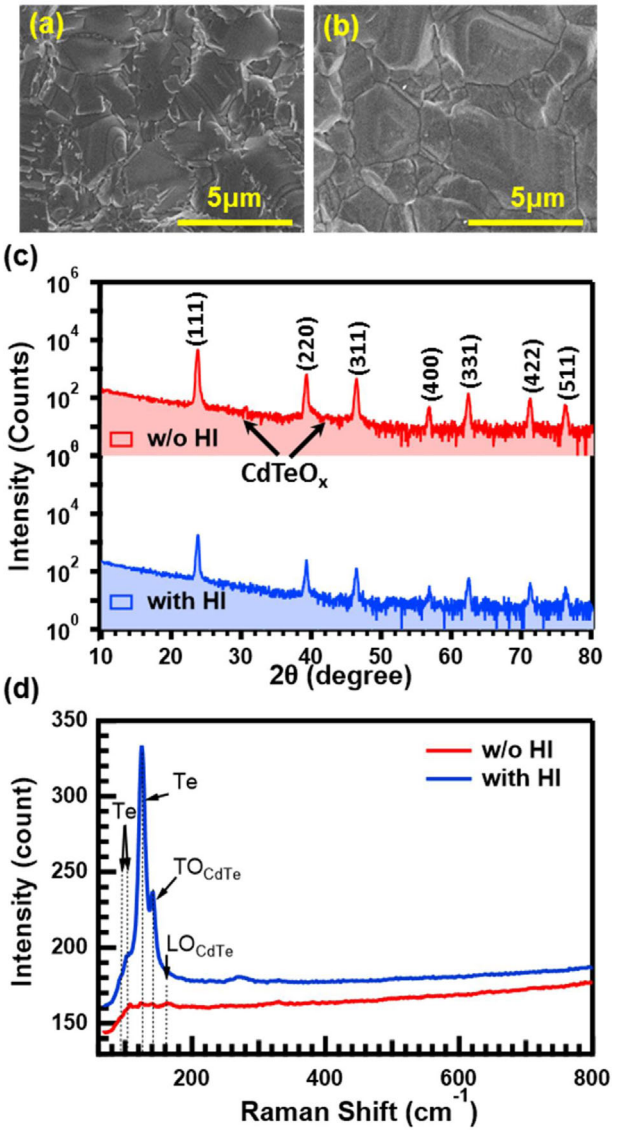

Figure 1. SEM images of a) control and b) HI-etched CdTe films. c) GIXRD patterns of a $CdCl_2$ annealed CdTe sample before (upper) and after (lower) HI etching treatment. d) Raman spectra of the control and HI-etched CdTe films.

2. Results

2.1. Solar Cell Performance

To examine the impact of HI etching on the CdTe surface morphology, we obtained SEM images of CdTe films with and without the HI treatment. **Figure 1**a shows the compact CdTe film morphology with a grain size of >2 μm after the $CdCl_2$ treatment. A significant amount of particles, likely consisting of cadmium oxides and/or chlorides as determined by energy dispersive X-ray spectroscopy (EDS) measurements (Figure S1a–c and Table S1, Supporting Information), were observed on the CdTe surface. These native oxides and/or chlorides on the CdTe surface were found to be removed by the HI etching (Figure 1b), and confirmed by glancing-incidence X-ray diffraction (GIXRD) (Figure 1c). These results were further confirmed by Auger electron spectroscopy (AES) measurement as shown in Figure S1d,e, Supporting Information. For the untreated sample, there is a high Cl signal on the surface, while Cl signal becomes uniform in the HI-treated device. Similar native oxides and chlorides have been observed on CdTe surfaces treated by $CdCl_2$.[14,15] Raman spectroscopy analysis revealed a significant increase in the intensity of stretching modes of Te–Te vibrations after the HI treatment (Figure 1d), indicating the formation of a Te-rich back surface as reported in the literature.[16] For the HI-treated device, the Te concentration is higher than Cd in the surface region. After 2 cycles of sputtering (≈6 nm), the surface is no longer Te rich as shown in the AES results (Figure S1b, Supporting Information). The formation of a Te-rich layer can also be confirmed by the magnified SEM images as shown in Figure S2a and b, Supporting Information. Before treatment, the

grains look smooth aside from the existence of the large oxide particles. After HI treatment, the grains look rougher and a layer of small particles have formed on the surface. By combining the EDS, Raman, and SEM results, the small particles uniformly covered on the grain should be Te-rich. In addition, before HI treatment, the grain boundaries (GB) look more narrow and flat than that after HI treatment, indicating the penetration of HI solution and presence of a thicker Te-rich layer in the GBs. Atomic-force microscopy (AFM) (Figure S2c,d, Supporting Information) analysis revealed that the roughness of the CdTe surface was reduced from an average roughness (Ra) of 275 ± 2 nm (and root-mean-squared roughness, rms, of 336 ± 3 nm) prior to HI etching to an Ra of 243 ± 5 nm (and Rrms of 296 ± 6 nm) after HI etching. The roughness change is consistent with observations from CdTe films etched with other agents.[17] A comparison of these quantitative results with the SEM images provided in the manuscript strongly suggest that the action of the HI etchant works to reduce the presence of sharp/jagged CdTe grain edges as well as any small outcroppings of oxide and/or oxychloride grains that may exist on the CdTe surface – both features potentially contribute to charge carrier recombination sites and/or regions of poor electrical contact with the metal back electrode.

We fabricated and compared CdS/CdTe solar cells using CdTe films with and without the HI treatment. **Figure 2**a presents the *J–V* curves of the best performing devices. Figure S3, Supporting Information, shows the statistics of the PV device performance parameters from ≈20 devices. The HI treatment shows clear improvement in all parameters. The HI-etched device exhibits a maximum PCE of 15.05%, with an open-circuit voltage (V_{OC}) of 0.85 V, a short-circuit current density (J_{SC}) of 24.39 mA cm^{-2}, and a fill factor (FF) of 72.86%. In contrast, the highest efficiency control device shows inferior PV performance, with a PCE of 12.05%, a V_{OC} of 0.83 V, a J_{SC} of 23.57 mA cm^{-2}, and a FF of 63.74%. In order of significance, HI etch increases the FF, J_{SC}, and V_{OC}. The FF of the CdTe device is dominated by a less-than-optimal back-contact and bulk resistivity of CdTe. The J_{SC} improvement and external quantum efficiency (EQE) enhancement in (Figure 2b) both the short (350–550 nm) and long wavelength range (600–850 nm) point to possible simultaneous effects by the HI etch in the front (CdS/CdTe) and back junctions. The V_{OC} improvement could result from defect reduction in the CdTe bulk and improvement of the back interface. In order to elucidate the mechanisms under which the HI etch improves the FF, J_{SC}, and V_{OC}, below we collect experimental evidence using a suite of electrical characterization techniques described in Section 2 and analyze the underlying device physics in Section 3.

J–V–T measurements were carried out on the control and HI-etched devices (**Figure 3**) to understand the effects of HI etching. Normal *J–V* diode behaviors were observed from both devices at

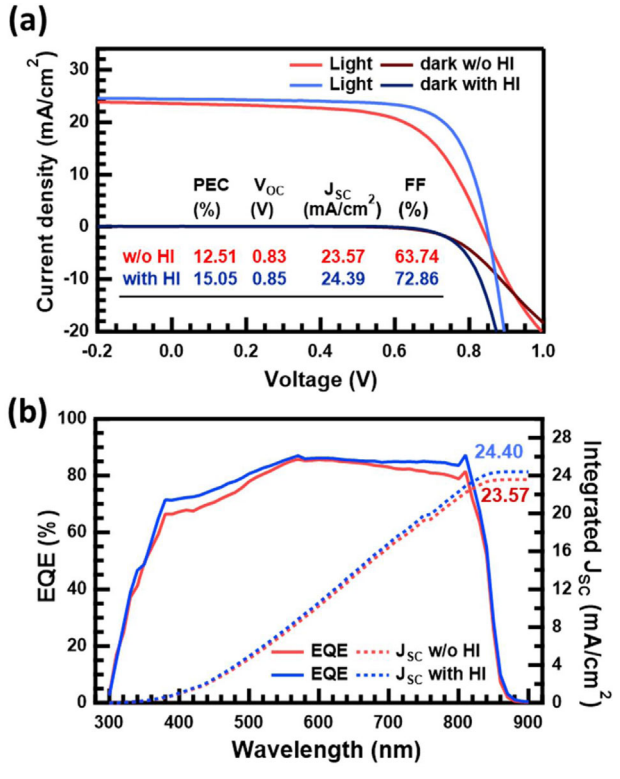

Figure 2. a) Light and dark *J–V* curves of our best control and HI-etched CdTe devices, and b) external quantum efficiency spectra and J_{sc} integrated over a 100 mW cm^{-2} AM1.5G solar spectrum of the control and HI-etched CdTe devices.

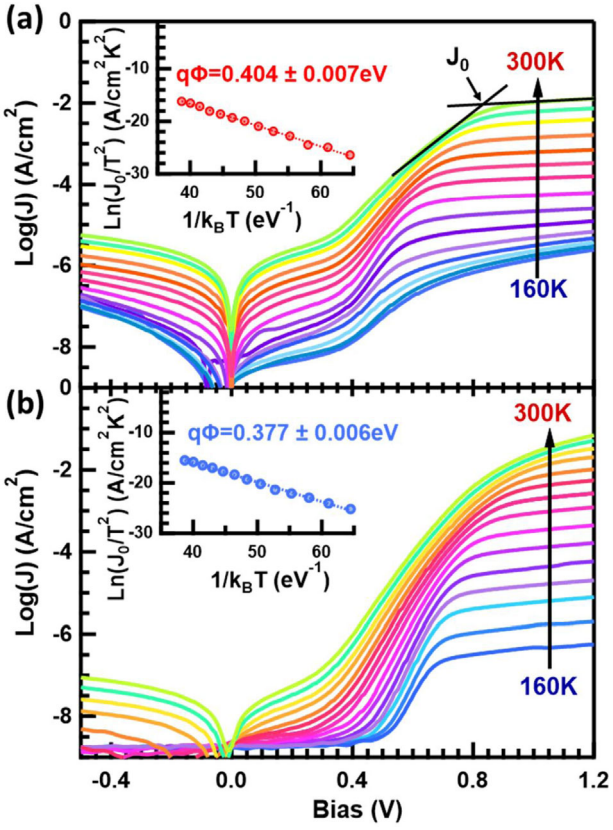

Figure 3. Dark *J–V–T* curves of the a) control and b) HI-etched CdTe solar cells. The insets show Arrhenius plots that were used to calculate back-contact barriers.

room temperature. However, cooling to lower temperatures led to a rollover at forward biases for both devices, indicating a non-ohmic contact at the CdTe/back contact interface. The non-ohmic back contact creates a barrier that blocks the hole extraction and increases recombination at the back interface. The downward band bending of the CdTe near the non-ohmic back contact also forces the minority carriers (electrons) in this region to drift toward the back-contact instead of toward the front-contact, resulting in unwanted recombination at the back contact interface. Assuming thermionic emission at the back junction, the saturation current density (J_0), which can be estimated from the intercept point of the pre- and post-rollover slopes[18] (Figure 3a), is described by the equation:

$$J_0 = A^* T^2 \left[\exp\left(\frac{q\Phi}{k_B T}\right)\right] \quad (1)$$

where A^* is the Richardson constant, T is temperature, q the electron charge, Φ the back-barrier height, and k_B the Boltzmann constant. The activation energy (E_a) for the back-barrier was extracted using an Arrhenius plot of $\ln(J_0/T^2)$ versus $1/k_B T$, as shown in the insets of Figure 3. The control device has a back-barrier activation energy of 0.404 eV, which is higher than that of the HI etched device (0.377 eV), showing that HI treatment helps reduce the back barrier height.

The current rectifying curves can be modeled according to the Shockley ideal diode equation[19]:

$$J = J_s\left[\exp\left(\frac{qV}{nk_B T}\right) - 1\right] \quad (2)$$

where n is the diode ideality factor and J_S is the saturation current density of the CdS/CdTe front junction. To find the ideality factor and the saturation current, we fitted the dark J–V curves measured at room temperature.[19] The ideality factor and saturation current density of the HI-etched device are 1.58 and 2.08×10^{-7} mA cm^{-2}, respectively, lower than those of the control device (1.65 and 9.96×10^{-7} mA cm^{-2}). These results are in good agreement with the reduction of the back barrier and PV performance for devices with the HI-treatment.

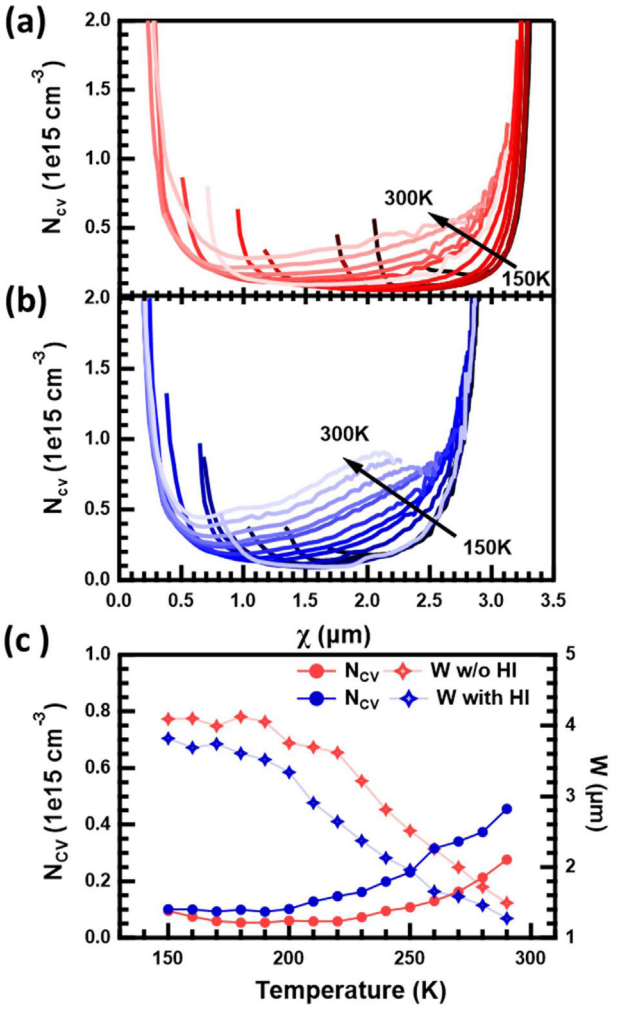

Figure 4. Carrier concentration as a function of the distance from the p-n junction of the a) control and b) HI-etched CdTe solar cells. c) Carrier concentration, calculated from the fitting curve of Mott–Schottky plot (Figure S5, Supporting Information), and the depletion region width calculated at 0 V bias voltage as a function of temperature for these devices.

2.2. Capacitance–Voltage Measurements

The C–V–T measurements were performed for the control and HI-etched CdTe devices. Figure S4, Supporting Information, shows temperature dependent Mott–Schottky plots of the control and HI-etched devices. The carrier concentration (N_{cv}) can be calculated from the following equation[20]:

$$N_{CV} = \frac{2}{q\varepsilon\varepsilon_0}\left[\frac{dC^{-2}(V)}{dV}\right]^{-1} \quad (3)$$

where ε and ε_0 are the relative permittivity value of CdTe and absolute permittivity of vacuum, respectively. The distance from the front junction (χ) is calculated directly from $\chi = \varepsilon\varepsilon_0/C$, where C is the capacitance per unit area. **Figure 4**a,b show the temperature-dependent charge carrier concentration profiling curves of CdTe cells without and with the HI-treatment, respectively. The apparent carrier density was estimated from the Mott–Schottky plot (Equation (3)) at zero bias. The carrier density of the control device increased from 9.5×10^{13} to 2.7×10^{14} cm^{-3} when temperature increased from 150 to 300 K (Figure 4a). The HI-etched device shows slightly higher carrier concentrations than the control device, with hole concentrations of 1.0×10^{14} and 4.5×10^{14} cm^{-3}, at 150 and 300 K (Figure 4b), respectively. Although both devices show temperature dependence of capacitance at reverse bias voltage (Figure S4, Supporting Information), the variation in the HI-etched device is more pronounced than the control one. The depletion region width is calculated from the following equation:

$$W = \sqrt{\frac{2\varepsilon\varepsilon_0 (V_{bi} - V)}{qN_{CV}}} \quad (4)$$

where V_{bi} is the built-in potential extracted from the Mott–Schottky plot at a bias of zero voltage. Carrier freeze-out in the HI-etched device results in a fully depleted CdTe absorber at temperatures below 210 K (Figure 4c), and the geometric capacitance (C_g) of CdTe layer is estimated to be 4.38 nF cm^{-2}.[21] The full depletion is more pronounced in the control device where the geometric capacitance (3.16 nF cm^{-2}) is reached at a higher threshold temperature (≈230 K). Hence, the doping concentrations (illustrated in Figure 4c) are independent of temperature below 200 K because of carrier freezeout. At temperatures higher than 160 K, the carrier density in the HI-etched device is higher than in the device without HI etching. We speculate that this is due to enhanced copper diffusion and doping by HI etching that removes the native oxides and/or chlorides and creates a Te-rich layer at the back surface of CdTe absorber.

2.3. Thermal Admittance Spectroscopy Measurements

To further investigate the effects of the HI treatment on the defect properties of CdTe devices, we performed TAS measurements. **Figure 5**a,b show the capacitance dependence on frequency and temperature for the devices without and with the HI treatment, respectively. The capacitance of the HI-etched device is higher than that of the control device at the same frequency and temperature. In the high-frequency region (>10^4 Hz), both devices show similar capacitance drops which could be due to series resistance effects.[22–25] At low frequencies (<10^4 Hz), the capacitance of the HI-treated device increases with increasing temperature or decreasing frequency. In contrast, the control sample shows a capacitance plateau with decreasing frequency at a given temperature. At this frequency range, the control device shows a capacitance inflection that is not observed in the etched device. This suggests the removal of a defect state that is likely due to the formation of Te-rich surface and copper diffusion via GBs. This effect is beneficial to improving the PCEs due to enhanced current collection.

Other capacitance inflection points were observed at higher frequencies for both devices, as shown in Figure S5, Supporting Information. These transition peaks shifted to higher frequency with increasing temperature because of the faster thermal emission rate over the barrier at higher temperature.[26] **Figure 6**a shows the Arrhenius plots of the transition frequency ($\ln\omega/T^2$) versus the reciprocal of temperature. The thermal

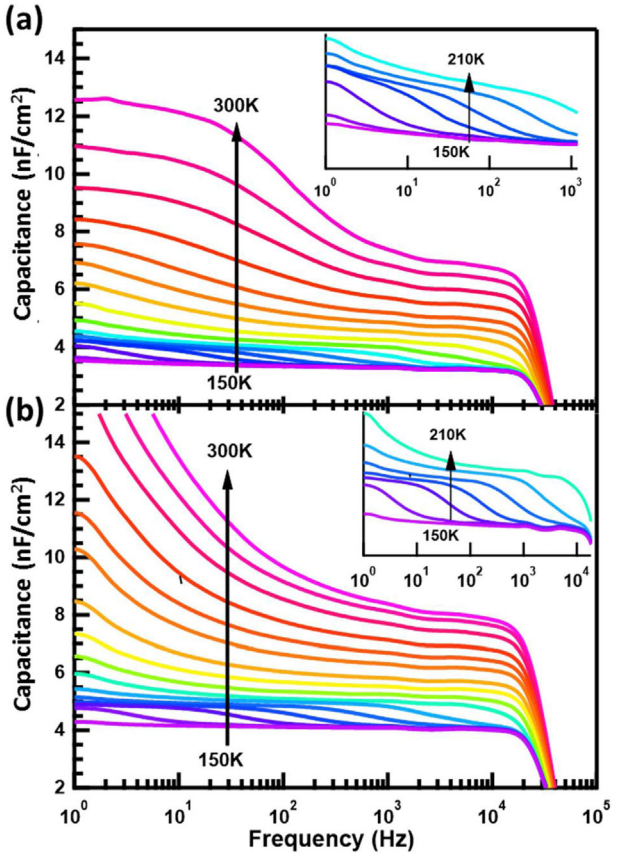

Figure 5. Capacitance-frequency spectra of CdTe solar cells a) without and b) with the HI treatment, measured under dark at 0 V applied bias at temperatures from 150 to 300 K with a step size of 10 K.

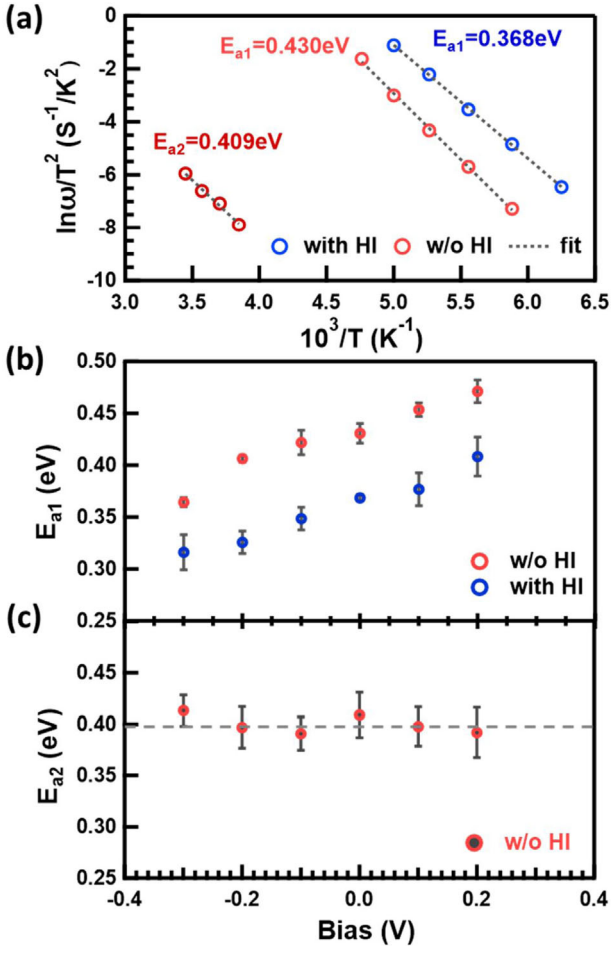

Figure 6. a) Arrhenius plots of admittance spectroscopy signatures of CdTe solar cells with and without the HI treatment measured at 0 V bias voltage. Defect activation energies b) E_{a1} of the control and HI etched devices, and c) E_{a2} of the control device as a function of DC bias voltage.

activation energy can be calculated by the following equation[27]:

$$\omega_0 = A_0 T^2 \exp\left[-\frac{E_a}{k_B T}\right] \quad (5)$$

where ω_0 is the characteristic transition frequency, A_0 is a pre-exponential factor independent of temperature, and E_a is the activation energy of the signature seen in admittance spectroscopy. Three characteristic activation energies, including ($E_{a1} = 0.368 \pm 0.008$ eV) for the HI-etched device and ($E_{a1} = 0.430 \pm 0.009$ eV) and ($E_{a2} = 0.409 \pm 0.023$ eV) for the control device, are extracted from fitting with Equation (5). The values of 0.430 and 0.368 eV for the non-HI and HI-etched devices, respectively, are most likely related to H2-type (hole trap) defects and their ionization by hole emission over the back-contact potential barrier.[18,28–31] Note that the E_{a1} values determined by TAS are in good agreement with the barrier heights that were calculated from J–V–T curves, with values of 0.404 and 0.377 eV for the control and HI-etched devices, respectively.[30,32]

The control device exhibits an admittance spectroscopy signature with an activation energy (E_{a2}) of 0.409 ± 0.023 eV. This signature is consistent with that observed in the Cu-free devices reported by Seymour et al.,[4] which is attributed to acceptor defect complexes such as V_{Cd}–Cl_{Te}, V_{Cd}–V_{Te} or Cu_{Cd}–V_{Te}.[33–34] These defects are likely formed in Te-deficient conditions and can be eliminated by introducing a Te-rich back surface as well as increasing Cu doping in the bulk CdTe.

To determine whether the defects are associated with bulk or interface defects, TAS measurements were performed at various DC biases with constant AC modulation.[35] When the AC modulation is applied, the Fermi level oscillates accordingly around a mean position. The interface states change occupancy at the Fermi level, whose position in the bandgap varies with DC bias, thus contributing to the measured capacitance and producing the TAS signature. The thermal activation energy (Equation (5)) of the TAS signature contributed by interface states will be modified by the external bias. It is well known that the E_F position can be shifted by applying a bias voltage. Such a shift would change the occupancy of interface states, but not bulk defect states. Therefore, the activation energy of interface states will depend on the applied bias voltage.[32,36–38] Figure 6b shows that the activation energy E_{a1} increases with bias voltage, indicating that the E_{a1} signature may originate from the interface states.

In contrast, the capacitance response from E_{a2} is bias independent (Figure 6c), which suggests that the charged defects contributing to the carrier transport are located in the bulk of the CdTe absorber. The HI-etching leads to Te enrichment at GBs and a drop in GB resistance (R_{GB}), which restrains the response of the bulk defects.[10] Additionally, the capacitive properties of GBs may also be changed by additional doping and the electrical field of the depletion region, when the amount of enriched Te is large.

2.4. Temperature-Dependent Complex Capacitance Analysis

We employed complex capacitance spectroscopy – a form of impedance spectroscopy – to study the impact of HI etching on the back contact properties of CdTe solar cell devices. First, we determined the equivalent circuit model that best fit the complex capacitance spectra. So far, the most commonly used circuit model consists of two parallel combinations of resistance–capacitance (R–C) elements (Figure S6, Supporting Information) with possible resistance or capacitance considered in series connection with them.[18,39] This model did not fit the complex capacitance spectra obtained from our devices very well (Figure S7a,b, Supporting Information), and is likely more suitable for ideal devices. We found that an additional constant phase element (CPE_j on **Figure 7**a) and rearrangement of the previous equivalent circuit are needed to fit our results (Figure 7b,c). The modified model is consistent with the results reported by Proskuryakov et al.[40] They demonstrated that the

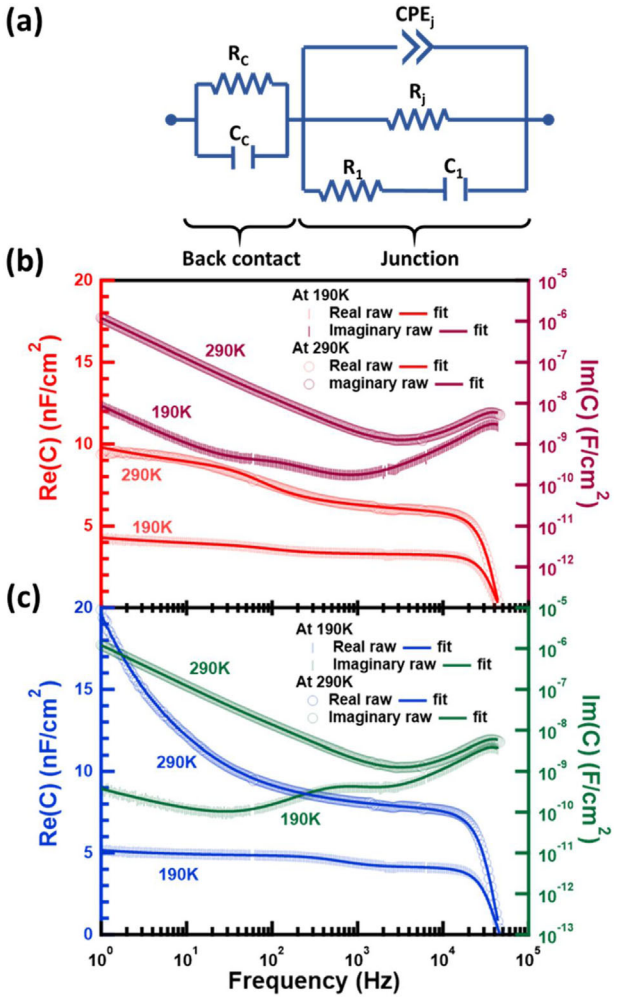

Figure 7. a) The equivalent circuit model of nonideal diode that was used to fit the complex capacitance Nyquist plot, with the elements R, C, and CPE represent the resistance, capacitance, and constant phase element, respectively, with two sub-circuits connected in series, one is due to the back contact (subscript c) and the other part due to the p-n junction and the bulk material (subscripts j and 1, respectively). Fitting parameters are used as free. Real and imaginary parts of capacitance as a function of frequency measured at 190 K and 290 K at at 0 V bias voltage for b) control and c) HI-etched devices. The solid lines are the fitted curves using the suggested equivalent circuit model of nonideal diode in **Figure 7**a.

AC response from the main p-n junction, defect levels, and interfaces inhomogeneities can be modeled by adding a parallel connection of many series assemblies of R and C elements.

A Schottky barrier (non-ohmic back contact) at the CdTe/Au interface can be described by a parallel assembly of R–C combination that is connected in series with the main junction (Figure 7a).[39–41]

The fitted back contact capacitance (C_C) as a function of temperature of the devices without and with HI etching are shown in **Figure 8**a. At temperatures <220 K, C_C of both devices are independent of temperature due to freezeout, but at higher temperatures, the back contact capacitance of HI-etched device is lower than that of the control device due to the removal of native oxides and/or chlorides that create additional barriers to holes. The fitted resistance due to the back contact (R_C) of the HI-etched device is lower than the control device by more than one order of magnitude at 190 K and about one order of magnitude at 290 K as shown in Figure 8b, where R_C is plotted as a function of bias voltage. The reduction of the fitted resistance of a Schottky barrier for the HI-treated device is due to the increased conductivity resulting from the Te-rich back surface. R_C slightly decreases as the bias voltage increases for a device at a given temperature, since the small bias voltage only leads a voltage drop at the front junction (CdS/CdTe).[36] The back barrier height can be calculated from the fitted back contact resistance using the following equation[40]:

$$R_C = \frac{B_0}{T^2}\exp\frac{q\phi}{k_B T} \tag{6}$$

where B_0 is a pre-exponential factor independent of temperature. From Arrhenius plots illustrated in Figure 8c, the back barrier heights were calculated to be 0.408 ± 0.016 eV and 0.363 ± 0.023 eV for the control and HI-etched devices. These results are consistent with our J–V–T, and admittance spectroscopy results. A similar trend was found previously by Major et al.[42] for CdTe devices that underwent nitric phosphoric acid etching that also enhances the formation of Te-rich layer at the back surface.

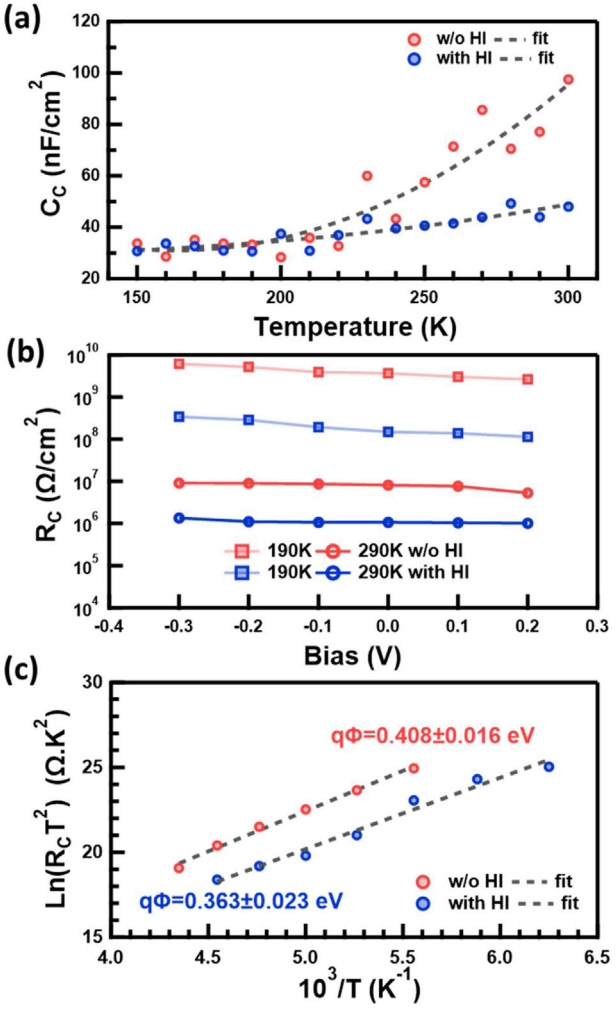

Figure 8. a) Temperature dependence of fitted back contact capacitance, b) the fitted back contact resistance as a function of bias voltage at two selected temperatures, 190 K and 290 K, and c) Arrhenius plots of the fitted back contact resistance of the CdTe solar cells with and without the HI treatment.

3. Discussion

The experimental results collected in the preceding section present three intersecting aspects of this investigation. The first aspect is based on the fact that the HI etching improves CdTe device performance through enhancement of the FF, J_{SC}, and V_{OC}. The second aspect follows the locations within the CdTe device where the HI etch may have an effect, which include the back-contact, bulk CdTe, GBs, and the CdS/CdTe front junction. The third aspect follows the electrical properties revealed by the functional characterization methods: J–V/EQE, J–V–T, C–V–T, admittance spectroscopy, and complex capacitance spectroscopy. Below we use evidences in the second and third aspects to discuss the device physics underlying the performance enhancement observed in the first aspect.

J–V–T, admittance spectroscopy, and complex capacitance analysis all consistently confirm back-contact improvement via HI etching. The measurement parameters and device physics exploited by these three methods are complementary to each other. J–V–T is a DC measurement that extracts the barrier height and a version of R_C. Admittance spectroscopy is an AC measurement that assumes an equivalent circuit, conventionally intended for defect detection, that may be used to extract barrier height but not R_C. Complex capacitance spectroscopy is one form of impedance spectroscopy, which is also an AC measurement, that is typically not intended for detection of defects. However, when applied to an improved and more sophisticated equivalent circuit, it can also yield barrier height and R_C. To our knowledge, this is the first report of the complex capacitance spectroscopy technique being used to study back-contact in a diode structure, which is proven just as effective as – and may even be more powerful than – the combination of J–V–T and TAS methods.

For FF enhancement, HI etch has an effect on both the CdTe bulk and back contact. For bulk CdTe, HI etch results in a slight increase of N_{CV} and a reduction of activation energy of CdTe bulk resistivity (Figure S8, Supporting Information). On the back contact, HI etch

reduces the potential barrier height and effective contact resistance R_C. Combined, these two mechanisms allow more current to flow through the device under large forward bias, thus improving the fill factor. The improvement of the CdTe absorber in terms of eliminating the 0.409 eV defect, together with other effects that improves the front junction quality, reduces the ideality factor, which also is a positive contribution towards higher FF.

The improvement in J_{SC} of the HI-etched device was attributed to the EQE improvements (Figure 2b). Interestingly, the HI-treated sample shows enhancement for short wavelength photons in the range of 350–550 nm, indicating improved quality of CdS/CdTe p-n heterojunction. It was reported that the presence of proper amount of Cu at the p-n junction benefits charge separation at the depletion region.[5] It is possible that the HI-treatment creates or enhances certain pathways to facilitate Cu diffusion to the p-n junction. Additionally, the increase of EQE in the long wavelength region (600–850 nm) is expected as a result of the flattening of the detrimental downward band bending and the decreased density of non-radiative recombination centers near back contact, which also contributes to the improved FF.

For V_{OC} enhancement, the HI etch works because it (1) eliminates some defects in the CdTe bulk characterized by an activation of $E_{a2,}$ (2) forms a less rectifying back contact (lower barrier height and lower R_C), whose band bending is less severe than the non-etched case, thus causing less minority electrons to recombine at the back-contact,[8] and (3) improves the defect situation at the back-contact interface due to the removal of native oxides and chlorides. That the HI-etch results in much lower saturation current density J_S (Figure 3) is a direct evidence of suppressed recombination near the CdS/CdTe front junction, which contributes to the V_{OC} enhancement.[43]

4. Conclusion

In summary, we have shown that HI surface etching can be used to improving device performance of CdTe solar cells, with an increase of our best cell PCE from 12.51% to 15.05% after the etching process. The effects of the HI etching on the CdTe film were examined structurally and chemically, while the effects on device performance were investigated by a suite of DC and AC electrical measurements which collectively provide a corroborative picture as to why the HI etch improves the FF, J_{SC}, and V_{OC}. The HI-etched devices show higher apparent carrier concentrations than the control devices, suggesting an increased copper doping in the CdTe absorber. The potential barrier height of the back contact is reduced from 0.430 to 0.368 eV after the HI-treatment, accompanied by reduced contact resistance and recombination. Additionally, the HI-treatment eliminates a defect signature at 0.409 eV.

5. Experimental Section

CdTe solar cells were fabricated on fluorine-doped tin oxide (FTO) glass substrates (TEC 15M; Pilkington NA). The substrates were cleaned sequentially with Micro-90 detergent in an ultrasonic bath in hot water (≈70 °C) for an hour, submerged in de-ionized water for 30 min for 4 times, then rinsed with de-ionized water and dried with nitrogen. An 85 nm CdS:O buffer layer was deposited on FTO by radio-frequency (RF) sputtering under a mixed gas flowrate of 40 sccm with a composition of 2% oxygen and 98% argon, followed by depositing a ≈4 μm CdTe films by CSS. A saturated solution of $CdCl_2$ in methanol was applied to the CdTe film surfaces drop-wise and then annealed at 390 °C for 30 min in dry air with a 500 sccm flowrate. After the samples cooled to room temperature, excess $CdCl_2$ was removed by rinsing with methanol. For the HI treatment, 0.3 wt‰ HI (Sigma–Aldrich) diluted in methanol (Fisher Chemical) was used to etch the back surface for 30 s at room temperature. After that, a bilayer of Cu (≈3 nm) and Au (40 nm) was deposited by thermal evaporation via a shadow mask with an individual cell area of 0.08 cm^2. Finally, the devices were annealed in nitrogen at 200 °C for 20 min to promote Cu diffusion into the CdTe.

Surface imaging and X-ray energy dispersive spectroscopy (EDS) measurements were performed using a Hitachi-4800S scanning electron microscope (SEM). Surface crystallinity and structure was determined by X-ray diffraction (XRD) measurements performed using a Rigaku Ultima III X-ray diffractometer operated in a GIXRD mode with the angle of incidence set to 0.25°. Auger electron spectroscopy (AES, Perkin-elmer, PHI 600) was performed with Xe electron source to characterize the elemental distribution on the back surface. During AES measurements, each cycle takes 6 s sputtering with a sputtering rate around 30 nm min^{-1}. Raman spectroscopy measurements were conducted using a Jobin Yvon confocal Raman spectrometer. Surface roughness measurements were conducted using a Zygo NV5000 5010 scanning white light optical profilometer. The AFM measurements were carried out using a Veeco Nanoscope IIIA Multimode with a scan area of 10 μm × 10 μm. Solar cell performance was evaluated by measuring *J–V* curves under AM1.5G illumination using a solar simulator (PV Measurements, Inc.) and a source meter (Keithley 2400). Temperature dependent *J–V–T*, *C–V–T*, TAS, and complex capacitance spectroscopy measurements were performed using a Solartron Modulab potentiostat equipped with a frequency response analyzer (Ametek, Inc.). The *C–V–T*, TAS, complex capacitance spectroscopy measurements were performed under a constant AC modulation voltage of 45 mV_{rms}. The *J–V–T* measurements were performed in dark with voltage sweeping from −0.4 to 1.2 V. The *C–V* measurements were performed in the dark with a constant 45 mV_{rms} 10 kHz AC signal superimposed on a DC bias voltage varying from −2.5 to +0.5 V. The TAS and complex capacitance spectroscopy measurements were done with frequency sweeping from 1.0 MHz to 0.1 Hz. DC biases varying from −0.3 to +0.2 V at a step size of 0.1 V were applied during TAS measurements. A liquid-nitrogen cooled cryogenic system (Janis VPF-100) was used to carry out all the temperature dependent (150–300 K with a step size of 10 K) measurements. The temperature was controlled by a temperature controller (Lakeshore 330). A temperature sensor was mounted on the top of the device directly, to ensure that the recorded temperature is the device temperature. The equivalent circuit model fitting of the complex capacitance spectra was done using RelaxIS impedance spectrum analysis software.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

admittance spectroscopy, CdTe solar cells, carrier density profiling, complex capacitance spectroscopy, HI etching

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