Fast Detection of Open Circuit Device Faults and Fault Tolerant Operation of Stacked Multilevel Converters

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Abstract— **This paper proposes a simple and fast technique for power device open circuit (OC) fault detection in stacked multicell converters (SMCs). A mitigation technique allowing for fault-tolerant operation using a simple front-end routing circuit is also proposed for SMCs. The fault detection concept only needs to sense the voltage and direction of current at the output terminal of the SMC to detect and localize an OC switch fault to a particular rail of the SMC. The proposed technique compares the measured and expected voltage levels considering the commanded switch states and the direction of the terminal current flow. Once an OC fault is detected and localized, the front-end routing circuit will be activated to reconfigure the SMC converter to a simple flying capacitor multilevel converter (FCMC) to maintain the output power flow with a reduced number of voltage levels. A window detector circuit is proposed to track the output voltage level and current direction with high bandwidth. Simulations were performed to validate the fault detection method and router performance. The functionality of windows detector is investigated with a hardware prototype 7 level 300 V SMC.**

Keywords— stacked multilevel converter, fault detection, fault tolerant, open circuit fault

I. INTRODUCTION

The concept of multilevel converters (MCs) were first developed for medium voltage drives to overcome the voltage rating and switching frequency limits of available power semiconductor switches [1]. Scalable structures, lower stress on the switches and improved output distortion with reduced switching frequency are the main advantages of this family of converters compared to conventional 2 level bridge type converters. A large number of multilevel converter topologies have been developed including diode clamped multilevel converters (DCMC), flying capacitor multilevel converters (FCMC), modular multilevel converters (MMC), cascaded multilevel converters (CMC), and stacked multicell converters (SMC). While initially developed for medium voltage applications, there is an increasing interest in adopting the multilevel topologies into lower power and voltage applications, especially those utilizing wide bandgap (WBG) switches [2, 3]. The reliability of today's WBG devices remains a major concern and for GaN devices voltage ratings are still limited. It would be advantageous to facilitate fault detection and fault tolerant operation in multilevel converters using WBG or silicon power switches.

A number of approaches have been proposed to detect and localize faults in IGBT multilevel converters [4]-[10]. These approaches can be categorized into the following broad categories: 1) harmonic spectrum analysis of the output voltage or current, 2) comparison of the predicted values of internal states with measured values, 3) complex identification techniques based on wavelets or fuzzy logic and 4) comparison of the commanded output voltage with measured values.

An example of the harmonic spectrum analysis approach for fault detection in FCMC using the output terminal voltage is presented in [4]. This method can detect short circuit faults but will not work properly for more than 3 switching cells. In addition, it requires a high computation effort and precise sensors to determine the fault location. Fault detection may require at least one cycle of the fundamental output waveform to be sampled.

Comparison of the predicted values of the capacitor voltages with measured values has also been used for fault detection in FCMC [5], MMC [6], and bridge FCMC [7]. A model predictive control (MPC) approach is used to predict the internal capacitor voltage states and current. This prediction is computationally expensive and requires precise sensor measurements of the capacitor voltages and currents for each capacitor. For open circuit (OC) faults the dynamic change internal states maybe slow and to discriminate that a OC fault has occurred it may take several cycles of the modulated waveform.

Complex methods based on wavelet and fuzzy logic approaches are reported in [10-11] which can be extended to multilevel converters. These methods suffer from high computational requirements, difficulty of localizing the fault, the need for a large number of additional sensors, and increased difficulty for high switching frequency WBG multilevel converters.

A number of researchers have used the comparison of the measured output terminal voltage with the commanded switch state to detect that a fault has a occurred and localize it [8], [9], [12-14]. This method has the advantage that a minimum number of sensors are required with relatively low computational effort. The sampling time and bandwidth of the

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voltage sensors however has limited the application of this technique for OC-fault detection. In [9] the filtered output terminal voltage is used which requires up to three modulation waveform cycles to detect the OC-fault. It will be shown later in this paper how a long detection and shutdown/fault bypassing time can lead to a cascading failure. To achieve synchronized fast sampling times, an FPGA can be used [12-14]. However commercial oscilloscope high bandwidth differential voltage (MTX 1032-B and CV 3-1200) and current probes (PR30) have been used by a number of researchers which are not realistic for commercial application because of their cost and bulk [12-14].

In [8], a MAX187 analog to digital converter (ADC) with 75 kHz bandwidth was used to detect the voltage levels. It takes 20μsec for the conversion, which means missing many output voltage level transitions or pulses, even for less than a 10 kHz switching frequency for AC modulation. Plus, the input of many ADCs are unidirectional so we need to rectify bipolar signals for AC modulation which may impose additional and potential asymmetrical delay for positive and negative modulation, high frequency gain attenuation, and additional components. Although the low switching loss of WBG devices allows for increased switching frequencies compared to silicon devices, fault detection method methods have not kept pace in terms of their fault detection and localization speeds. Also, sensor bandwidths have not kept pace with increasing switching frequencies.

Many references reported that OC-faults in the family of switched capacitor converters are not destructive and it was concluded that fast fault detection might not be mandatory to save the converter and avoid fault propagation as their main focus was on the OC-fault in the IGBTs [4] and [6-8]. In this paper, we will show that if there is an OC-fault in the antiparallel diode of a switch in a multilevel converter, a cascading failure can occur if the fault is not detected quickly and mitigated.

Once a fault is detected and localized, the converter must be disconnected from the power source and de-energized, the gating signals removed, or, for fault tolerant operation, the fault isolated and bypassed. In previous fault tolerant converters bypassing breakers or switches are needed for each commutation cell [6, 7, 9].

The contributions of this paper are the identification of the consequences of an OC-fault in multilevel converter antiparallel diodes, an OC-fault detection and faulted rail localization approach for single phase SMCs, and OC-fault tolerant SMCs using a front end router. The OC-fault detection and rail localization strategy for active switches is proposed by using the terminal output voltage signature of the converter compared to its commanded switching state. It can detect and localize the fault in less than $k-2$ switching transitions for a k levels converter. Fault tolerance is incorporated into the SMC by two simple front-end routing circuits consisting of either two switches operating at the PWM frequency of the rest of the converter or 3 on/off switches/breakers. The number of additional devices is either 2 or 3 regardless of the number of voltage levels and commutation cells. For high bandwidth detection of the output pulse voltage levels and current direction, a simple window detector circuit is proposed. It can respond to terminal voltage changes in around 0.1μsec allowing for high frequency PWM operation.

II. OC FAULT CONSEQUENCES

Many research studies assume the OC-faults in multilevel converters will not propagate because they focus on OC-faults in the controllable switches. The potential for fault propagation if an OC-fault occurs in a switch's antiparallel diode is discussed here in the context of SMCs [15], Fig. 1. However, the same phenomenon would occur in other types of multilevel switched capacitor converters.

A 7-level SMC with three switching cells is picked as a case study which is shown in Fig. 1 with black elements [15]. Phase shifted PWM (PSPWM) as a simple modulation method is used in this study. However, the results are independent of the applied modulation technique or the number of cells in the SMC.

For a purely resistive load, the terminal voltage and terminal current are always in phase and of the same polarity. However, for a load with non-unity power factor, there is always a period of time for which fundamental harmonic terminal voltage and current are not the same polarity. Assume that for this period of time, the converter synthesizes the positive cycle of a desired AC signal and the current is either flowing toward the converter from the load or vice versa. For a converter equipped with unidirectional switches like IGBT with antiparallel diodes, if one of the IGBTs faces OC-fault, there is no over voltage or over current in the converter.

However, if the converter loses one of the antiparallel diodes to an OC fault, in the period that the fundamental

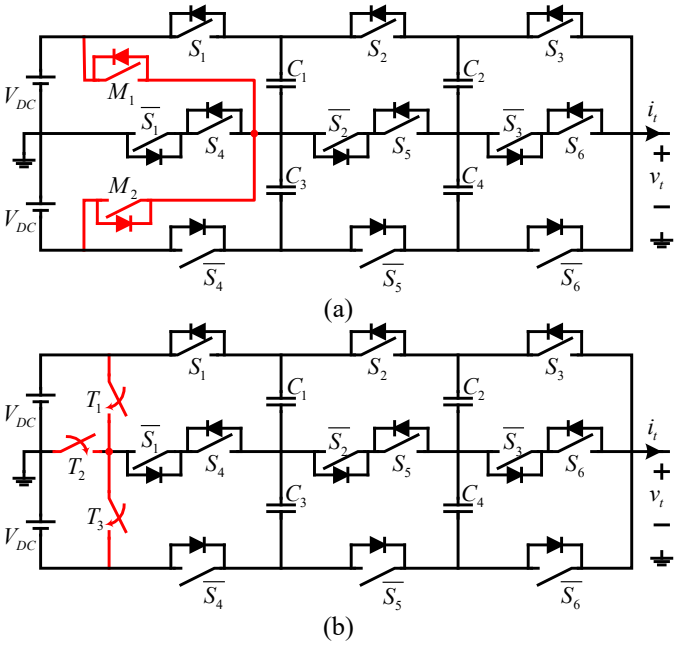


Fig. 1. 7 level stacked multilevel converter equipped with router circuits for post open circuit fault operation. (a) router with two PWM frequency switches M_1 and M_2; (b) router with three ON-OFF switches, T_1, T_2, and T_3.

voltage and current are not in phase while its corresponding IGBT is ON, there is no current path for the inductive load current to flow when the switch turns off. Hence, a large voltage spike will be imposed on the switch corresponding to the faulty antiparallel diode as well as two other OFF switches in the commutation cell. For instance, if the antiparallel diode of $\overline{S_5}$ has an OC-fault and $v_t < 0 \,\&\, i_t > 0$, when the current attempts commutate from S_5 *to* $\overline{S_5}$ where the antiparallel diode open circuit fault is located if the $\overline{S_5}$ switch is an IGBT it cannot reverse conduct. So there is no path for the load current as $S_5 S_2 = 00$ and an over voltage will be imposed on $\overline{S_5}, S_5 \,\&\, S_2$. This overvoltage can destroy these switches and also propagate to the rest of converter and damage the whole system.

However, for bidirectional switches like FETs, losing the external antiparallel diode to an OC fault will not necessarily cause an over voltage as the corresponding switch of the faulty diode can potentially handle the current in both directions through the body diode albeit with potentially increased losses. If an external antiparallel diode is not utilized with a FET and an open circuit fault occurs in the FET, its reverse conduction properties through its internal body diode will also be lost leading to a similar voltage overshoot condition on other switches in the same commutation cell.

To overcome this issue, two strategies can be envisioned. The first one is to locate the faulty diode and commutate the current to an extra path. However, we cannot detect the diode OC-fault before letting that diode to be in the path of current which means a voltage overshoot in the circuit and instantaneous destructive consequences. The second way which is simple and practical is to ensure that FETs and IGBTs are equipped for each of the switches with an external antiparallel diode as is normal for MOSFETs and IGBTs but is not always implemented for GaN based FETs. This redundant diode protects the circuit from the discussed overvoltage surge. This phenomena is simulated for a 7 level SMC with IBGT switches and a fault on the antiparallel diode of S_5 with a very small inductive load connected, Fig. 2. The load here is $50\,\Omega$ and $l = 10\,mH$ which corresponds to power factor of 0.99. As is shown in Fig. 2, a large overvoltage spike will be imposed on the output terminal of the converter and across the corresponding switch, $\overline{S_5}$ to the diode with the OC fault and similarly switches, S_5, S_2. The figure's per unit scale is limited to -2 pu but actual over voltage spikes are larger. For lower power factors, this problem will be more severe with larger and longer lasting voltage overshoots. This over voltage will be repeated in each cycle of output voltage waveform. So, if this fault is not mitigated, the circuit surges continuously till the system is destroyed and the flow of power blocked.

III. OC Fault Detection

The main focus of this paper is on the detection of switch OC-faults in SMCs. For detecting short circuit (SC) faults, conventional methods like desaturation detection which are commercially available can be used to distinguish between OC and SC faults to avoid ambiguity and false action of the controller.

For detecting a switch OC-fault we use the voltage signature of the output voltage terminal. In normal operation, depending on the switching state, the output terminal voltage has to be at a certain level. So simply, if the output terminal voltage level does not meet the normal operation signature and no fault has been reported from the other types of fault detection units such as a SC, then an OC-fault has happened in the converter.

For fault mitigation as discussed in section IV only the rail in which the OC fault has occurred needs to be located for uninterruptable operation of a converter equipped with a front end router. What is presented here is a simple way to find the faulty rail which even can be implemented using logic gates and a counter. However, more advance techniques can be used to find the exact location of the fault which is out of the scope of this paper. A 7-level SMC is used as a representative example but the proposed technique is not limited and can be extended for SMCs with other number of levels.

In the steady state, a 7-level SMC using natural voltage balanced techniques such as phase shifted pulse width modulation (PSPWM), the voltage of the flying capacitors are naturally balanced to $V_{C1} = V_{C3} = 2V_{dc}/3$ and $V_{C2} = V_{C4} = V_{dc}/3$. As it shown in Fig. 2, the top and the middle rails are switching for the positive half-cycle of the modulation waveform while the middle and bottom rails are switching for the negative half. Eight allowable switching configurations for the positive half cycle of the modulation waveform are listed in Table 1 for $\sigma_p = S_1 S_2 S_3, p = 0,...,7$.

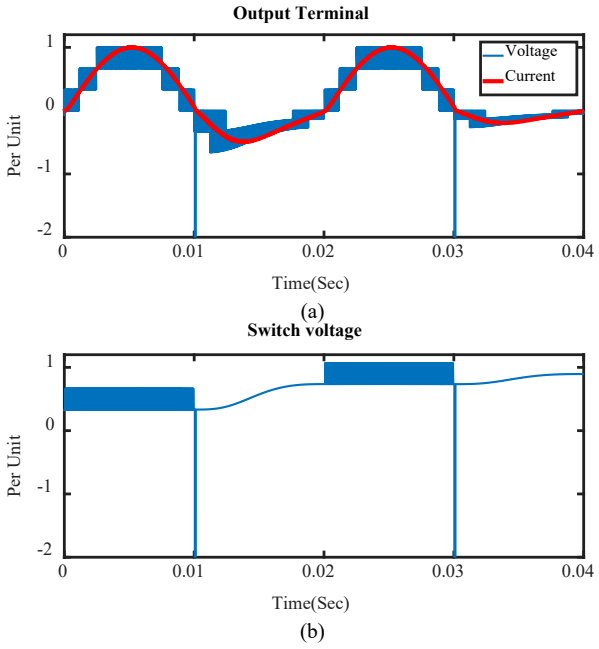


Fig. 2. OC-fault for antiparallel diodes of $\overline{S_5}$; (a) output terminal voltage and current, (b) switch voltage overshoot across $\overline{S_5}$ (similarly for $S_5, S_2, \overline{S_2}$).

TABLE I. VOLTAGE SIGNATURES FOR POSITIVE MODULATION WAVEFORM

			$\sigma_p = S_1S_2S_3$	0 = 000	1 = 001	2 = 010	3 = 011	4 = 100	5 = 101	6 = 110	7 = 111
Normal Operation Terminal Voltage				0	$V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	V_{dc}
Terminal Voltage for a Given OC Switch Fault Location	Upper Rail	$i_t > 0$	S_1	0	$V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$	0	$V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$
		$i_t > 0$	S_2	0	$V_{dc}/3$	0	$V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$
		$i_t > 0$	S_3	0	0	$V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$
	Middle Rail	$i_t < 0$	$\overline{S_1}$	$V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	V_{dc}	$V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	V_{dc}
		$i_t < 0$	$\overline{S_2}$	$V_{dc}/3$	$2V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	V_{dc}	$2V_{dc}/3$	V_{dc}
		$i_t < 0$	$\overline{S_3}$	$V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	V_{dc}	V_{dc}
		$i_t > 0$	S_4	$-V_{dc}/3$	0	0	$V_{dc}/3$	$V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	V_{dc}
		$i_t > 0$	S_5	$-V_{dc}/3$	0	$V_{dc}/3$	$2V_{dc}/3$	0	$V_{dc}/3$	$2V_{dc}/3$	V_{dc}
		$i_t > 0$	S_6	$-V_{dc}/3$	$V_{dc}/3$	0	$2V_{dc}/3$	0	$2V_{dc}/3$	$V_{dc}/3$	V_{dc}
			F_p	F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7

The notation of switching states are simplified as $\overline{\sigma_k}$ corresponding to the compliment of σ_k. In Table I, each switching state corresponds to a terminal voltage. During the OC-fault condition the terminal voltage may deviate from the normal condition depending on the switching function, the direction of the terminal current, and the exact location of fault, indicated by the grey shading in the Table I. However, faulty states do not have a unique terminal voltage signature. For instance, for $\sigma_p = 1$, for the fault in S_3, S_4 or S_5, the terminal voltage drops to 0 and the controller cannot distinguish between a fault in the top-rail, S_3, or the middle rail, S_4 or S_5. However, by processing/latching the fault signals over the next five switching states, we can determine the location of the fault. A similar table may be derived for the negative half cycle of the modulation waveform and localization of the fault to the middle or bottom rail. A fault flag signal, $F_p^{[n]}$ is generated for n samples after the detection of the initial fault. The flag signal takes a value of 0 for the normal operation and 1 if a fault is detected. The switch state p is also stored. As soon as, $F_p = 1$, it will be sent to the fault decision making unit and wait for a maximum next five successive flags to localize the fault based on the total accumulated fault flags vector of $\vec{F} = \left[F_p^{[1]}, F_p^{[2]}, F_p^{[3]}, F_p^{[4]}, F_p^{[5]}, F_p^{[6]}\right]$. Depending on the instantaneous value of the modulation command, v_m, we can divide the switching states to three subregions for a positive modulation command and the fault flag entries are used for fault detection. For $i_t < 0$ and $v_m > 0$, as soon as $F_p = 1$, fault is in the middle rail. For $i_t > 0$ and $v_m > 0$, the decision making is as in the following;

a) If $0 < v_m < (V_{dc}/3)$

Theoretically in this region if just $F_0^{[1]} = 1$, the voltage signature of the middle rail is different and the fault is in the middle rail. The fault decision making unit does not need to wait for the next five flags. However, if $i_t \approx 0$, it can cause a false positive detection as the terminal current will abruptly fall to zero and the output voltage will be zero as well. To guarantee the correct rail localization process, the decision should be based on the fault vector $\vec{F} = [F_1^{[1]}, F_2^{[3]}, F_4^{[5]}]$. If just one bit of $\vec{F}$ is 1, the fault is in top rail, or else the fault is in the middle rail. The required decision making time is six successive switch states. The simulation results for this condition are shown in Fig. 3 (a) and (b).

b) If $(V_{dc}/3) < v_m < (2V_{dc}/3)$

In this condition we need to use the fault vector $\vec{F} = [F_3^{[1]}, F_5^{[3]}, F_6^{[5]}]$ for the fault localization due to the similarity of the voltage signatures. If just one bit of $\vec{F}$ is 1, the fault was in the middle rail, or else the fault is in the top rail. The decision making time is six successive switch states. The simulation results are shown in Fig. 5 (c) and (d).

c) If $(2V_{dc}/3) < v_m < (V_{dc})$

We just need two switching state sequences. F_7 is one member of $\vec{F}$ and the other member is F_3, F_5 or F_6. If $F_7 = 1$, the fault is in the top rail, or else the fault is in the middle rail. The simulation results are shown in Figure. 3 (e) and (f).

For $v_m < 0$, the OC-fault will be detected similar to what is discussed for $v_m > 0$ by expanding the fault signature table for the negative modulation. Regardless of the number of levels, this method can be utilized for a k level SMC with OC-fault detection in maximum $k-2$ switching transitions.

IV. STACKED MULTILEVEL CONVERTER WITH FRONT-END FAULT MITIGATION ROUTER

Two routing methods are proposed to ensure an uninterruptable operation of the converter after the OC-fault incident. Additional components added to achieve the fault tolerance are shown in red in Fig.1. Once the OC-fault is

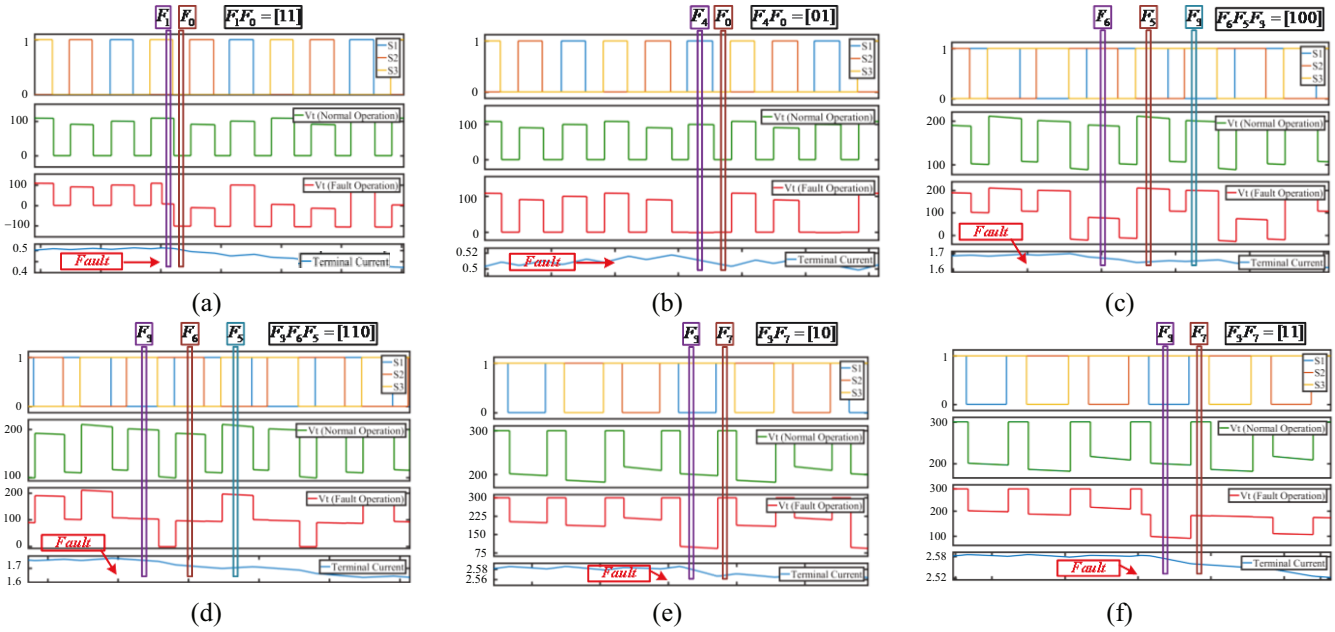


Fig. 3. Fault simulation waveforms (a) $0 < v_m < (V_{dc}/3)$ and fault in S_4, (b) $0 < v_m < (V_{dc}/3)$ and fault in S_1, (c) $(V_{dc}/3) < v_m < (2V_{dc}/3)$ and fault in S_6, (d) $(V_{dc}/3) < v_m < (2V_{dc}/3)$ and fault in S_2, (e) $(2V_{dc}/3) < v_m < V_{dc}$ and fault in S_5, (f) $(2V_{dc}/3) < v_m < V_{dc}$ and fault in S_3.

detected and localized using the techniques presented in the previous section or other approaches, the router will bypass the faulty rail and transform the 7-level SMC to a 5-level FCMC. In general, for a k level SMC, the circuit will be transformed to a $k-2$ levels FCMC.

For the first circuit (Fig. 1a), the router consists of two switches. These switches switch at the same PWM frequency as the remaining SMC switches during the post fault operation. The switch states of the router switches are defined by the switching variables M_1M_2 concatenated as a vector. The switch states of 7-Level SMC for positive half cycle of the modulation are defined by $S_1S_2S_3$ and for the negative half cycle by $S_4S_5S_6$. A switch state of 1 indicates that the switch is on and a switch state of 0 indicates that it is off. In the normal operation without a fault, $M_1M_2 = 00$ which indicates M_1 and M_2 are off. The positive and negative modulation commands are given in (1) and (2) for normal steady state operation.

$$v_{m1} = m\sin(\omega t)\left[u\left(t - T\left(k+0.5\right)\right) - u\left(t - Tk\right)\right] \quad (1)$$

$$v_{m2} = m\sin(\omega t)\left[u\left(t - Tk\right) - u\left(t - T\left(k+0.5\right)\right)\right] + 1 \quad (2)$$

As soon as the OC-fault would be detected, depending on the fault location, the modulation waveform will be changed according to (3) and (4) to operate the healthy rails as a FCMC. If the fault is in the top rail, M_1 will be substituted with S_4 in the modulation scheme of Fig. 4a and $\overline{S_1}S_4M_2 = 000$.

$$v_{m1} = 0.5\left(m\sin(\omega t) + 1\right) \quad (3)$$

$$v_{m2} = 0 \quad (4)$$

If the fault is in the middle rail, $\overline{S_1}S_4\overline{S_2}S_5\overline{S_3}S_6 = 000000$ and the modulation will follow (5) and (6) for the post-fault period.

$$v_{m1} = 0.5\left(m\sin(\omega t) + 1\right) \quad (5)$$

$$v_{m2} = 0.5\left(m\sin(\omega t) + 1\right) \quad (6)$$

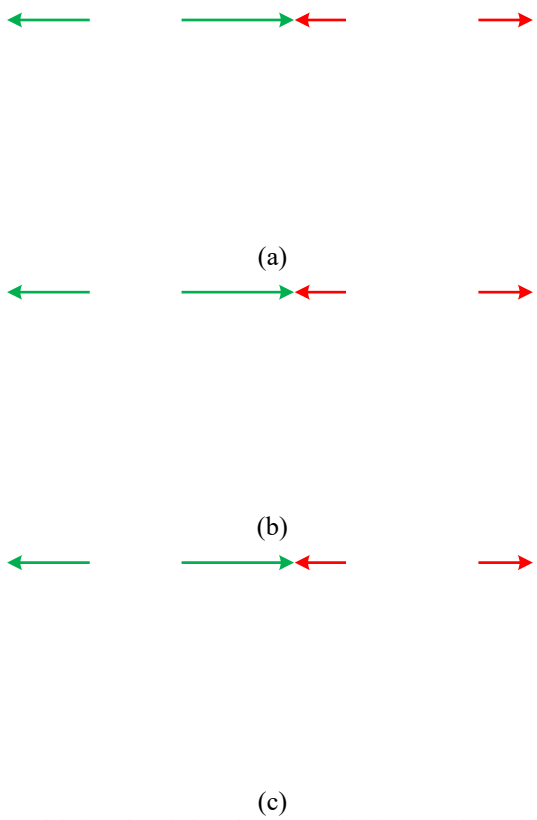
And for the fault in the bottom rail, M_2 will be substituted with $\overline{S_1}$ in the modulation scheme of Fig. 4c and $\overline{S_1}S_4M_1 = 000$ with the modulation changed to (7) and (8).

$$v_{m1} = 0 \quad (7)$$

$$v_{m2} = 0.5\left(m\sin(\omega t) + 1\right) \quad (8)$$

A second fault mitigation router concept is shown in Fig. 1b, router consists of three switches T_1, T_2, and T_3. These switches reroute the connections of the input voltage sources and are not modulated unlike the first routing circuit. In the normal condition, $T_1T_2T_3 = 010$. If the fault is localized to the top rail, the router circuit changes configuration to $T_1T_2T_3 = 100$ and the modulation waveform will be changed according to (3) to (4). For a fault localized to the middle rail $T_1T_2T_3 = 000$ and modulation will follow (5) and (6), with $\overline{S_1}S_4\overline{S_2}S_5\overline{S_3}S_6 = 000000$. When the fault is detected and localized to the bottom rail $T_1T_2T_3 = 001$ and the modulation scheme is changed as in (7) and (8) for the post fault condition, which are all shown in Fig.4.

The synthesized output terminal voltages utilizing both routing circuits are the same. An important consideration is during normal operating conditions for a k level SMC, the pre-OC-fault voltage across the switches is $V_{S_{1,\ldots(k-1)}} = 4V_{dc}/(k-1)$, $V_{M_{1,2}} = V_{dc}$ and $V_{T_{1,2}} = V_{dc}$ and for post OC-fault operation the voltage across the switches are $V_{S_{1,\ldots(k-1)}} = 4V_{dc}/(k-3)$, $V_{M_{1,2}} = V_{dc}$ & $4V_{dc}/(k-3)$ and $V_{T_2} = V_{dc}$. The voltage rating of

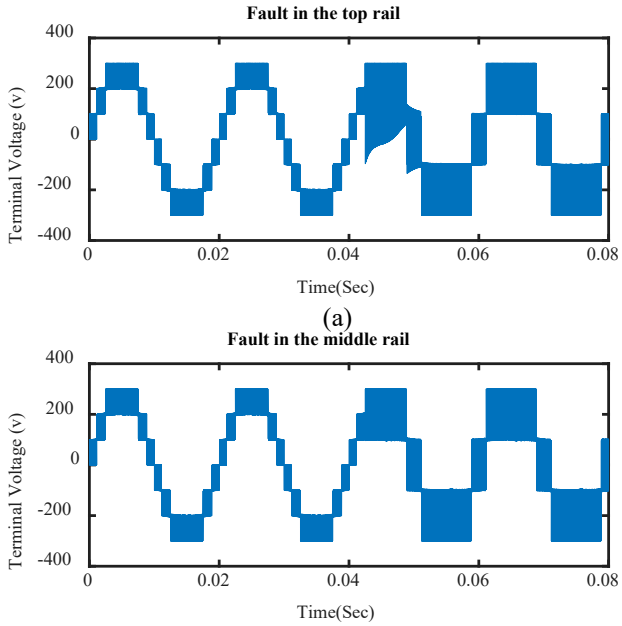


(a)

(b)

(c)

Fig. 4. Modulation phased shifted PWM modulation waveforms for 7 level stacked multilevel converter equipped with router circuit. Depending on the rail location of the open circuit fault the modulating wave is adjusted: (a) top rail open circuit fault, (b) middle rail open circuit fault, and (c) bottom rail open circuit fault.



(a)

(b)

Fig. 5. Output terminal voltage pre- and post- open circuit fault of SMC equipped with router; (a) Fault in the top rail, (b) fault in the middle rail.

the switches must be considered to ensure continued safe operation post OC-fault.

The 7-level SMC with the first proposed router is simulated using MATLAB Simulink's SimPowerSystems Toolbox with $V_{dc} = 300\,V$, $C = 100\,\mu F$, $f_{sw} = 10\,kHz$, $f_m = 50\,Hz$ and $R_{Load} = 50\,\Omega$. The fault occurs and the router circuit is triggered at $t = 0.044$ sec . The result of output terminal voltages for fault in the top rail and the middle rail are shown in Fig 5. The results for the fault in the middle rail is similar for the top rail.

V. SENSING VOLTAGE LEVELS AND CURRENT DIRECTION

For implementing fault detection based on the output terminal voltage signature, one of the biggest challenges is achieving a sufficiently high sensor bandwidth and detection logic with high PWM switching frequencies. For instance in the discussed fault detection method for a 7-Level SMC, the switching state can be changed up to six times during one PWM period. So, the sensing units have to respond quickly to follow the transitions. The other challenge is the duration of each particular PWM subcycle pulse can be very short, potentially even less than $1\,\mu$sec for certain switching states with AC modulation depending on the switching frequency of the converter. In addition, minimum pulse width restrictions imposed by gate drive circuitry may prevent the turn on and off of a switch even when commanded to. The measured voltage during that particular PWM subcycle would then not satisfy the expected values even in the un-faulted condition leading to a false positive detection of a fault.

Instead of using ADCs or oscilloscope probes, which are used in [8], [12-14], a simple windows detector circuit was developed to avoid any unnecessary complexity while maintaining a fast detection response. This circuit can be used for both sensing the terminal voltage level and also the direction of current. The implemented windows detector circuit is shown in Fig. 6 for finding voltage levels L_k where $(k = -M,...,0,...,+M)$, for a $k = 2M+1$ level converter.

This overall circuit contains a voltage divider for reducing the high voltage terminal with a sensing terminal, s, fed to the window detectors. Other voltage dividers set the boundaries of the detection windows. Two comparators are used, sensing each output voltage level and an AND gate at each coupled comparators to confirm the signal falls in the window band. As the input of the comparators are unidirectional and they can support from 0 to $+2V_{CC}$, two LDOs are used to provide $+V_{CC}$ & $-V_{CC}$ from an isolated supply and their common ground is directly connected to the power ground.

With this arrangement, a bidirectional windows detector can detect both positive and negative output voltage levels. A, 1 or logical true for each output pin indicates the value of the measured parameter is in the defined window band for each coupled comparator. For detecting the current direction, a similar concept is applied. Terminal current will pass a current sensing resistor to transduce the current and two windows cells, one for positive and other for negative current, will take care of finding the current direction. A small dead band in between can avoid zero crossing oscillation. In this circuit, the

ground of the bidirectional supply will be connected to the load positive rail which again can carry on the bidirectional input for TTL ICs in comparing stages similar to what was discussed for the voltage detector. At the end we have $2M+1$ bits for voltage levels and also 2 bits for detecting the current direction which all would be passed through an isolation barrier to the controller unit.

VI. EXPERIMENTAL RESULTS FOR WINDOWS DETECTION

An experimental prototype of the windows detector circuit is designed for a 300 V_{dc} input, 2 A MOSFET based 7-level SMC. Seven window detector bands were created to detect output terminal voltage levels of $\pm 300\,V, \pm 200\,V, \pm 100\,V \,\&\, 0\,V$. Each detection level has a band of $80\,V$ centered around the ideal output voltage level which is set using the voltage dividers previously described. In addition, two stages for detecting the current direction are also built with a 0.1% tolerance for zero crossing assuming a pure harmonic current. The window detector prototype is shown in Fig. 7 and the components are listed in Table. II.

The representative example fault operation of the window detector circuit for a modulation index of one, switch PWM

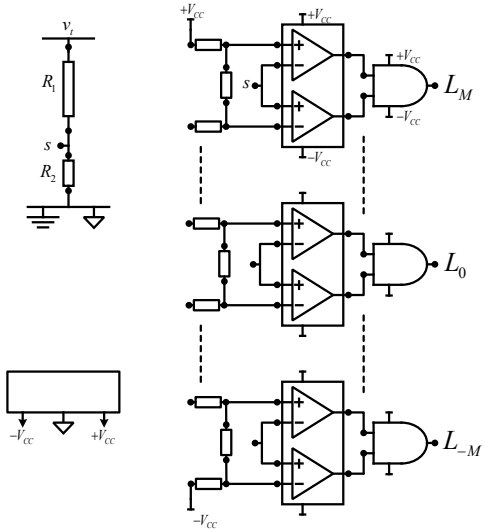


Fig. 6. Window detector circuit for fast terminal voltage and current direction sensing.

TABLE II. LIST OF COMPONENTS FOR THE WINDOWS DETECTOR

Component	*Part#*
AND gate	SN74LVC1G08DBVR
Dual Comparator	TLV3502AIDR
Digital Isolator	ISO7640FMDWR
2.5V LDO	LP5907MFX-2.5/NOPB
-2.5V LDO	TPS72325DBVR

frequency of 4 kHz, and converter output equivalent switching frequency of 12 kHz is shown in Fig. 8. Figure 8(a) shows the response of the windows detector to state transitions. In this figure the following traces are shown: PWM gate signal to S_1 (yellow), L_3 represents the window detection output for voltage level of 300V (green), window detector current direction with positive current outflowing current indicated by a high signal (blue) and the output terminal voltage of the converter (pink). In Fig. 8(b), the minimum pulse width of the output and the zero level window detector output is shown. It demonstrates that the proposed window detector circuit can detect pulses as small as $1\,\mu\text{sec}$. with the delay response of $0.13\,\mu\text{sec}$.

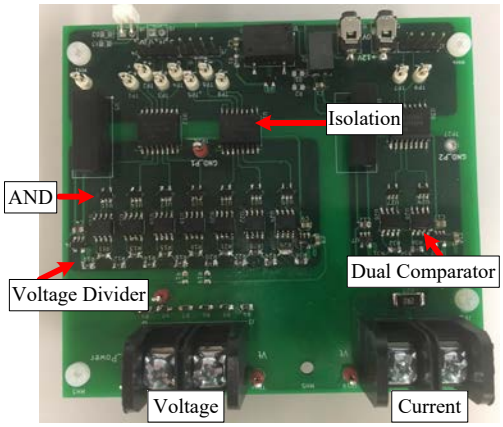


Fig. 7. Windows detector prototype hardware.

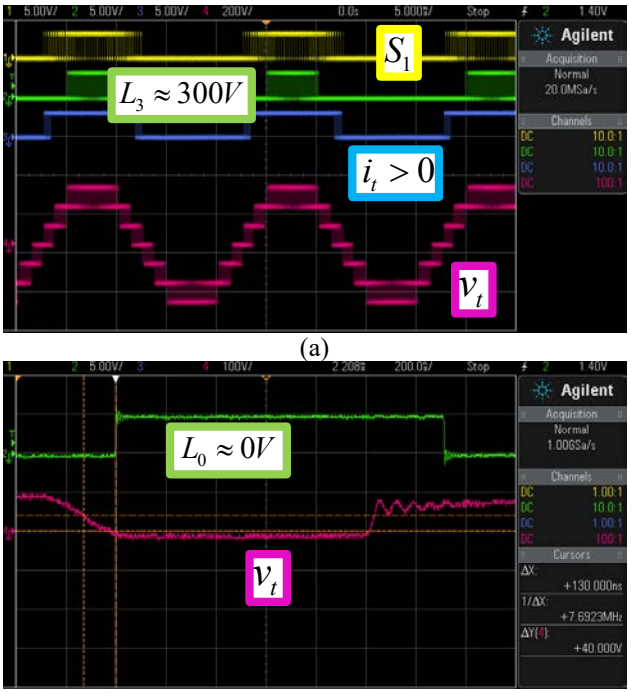


Fig. 8. Window detector prototype (a) operational demonstration and (b) minimum output pulse width detection.

In Fig. 9, an OC fault is applied on S_3 when $100\,V < v_t < 200\,V$ and the response of the window detector circuit and also the effect of the OC-fault on the prototyped 7-level SMC are shown. As it was explained in Sec. III, $F_3^{[2]} = 1$ which represents a fault in $\sigma_3 = S_1S_2S_3 = 011$ the second subcycle after the fault, $F_5^{[4]} = 0$ which means no fault in 4th subcycle after the fault corresponding to the switch state

$\sigma_5 = 101$ and $F_6^{[6]} = 1$ corresponds to a fault in $\sigma_6 = 110$ for the 6th subcycle. As a result the accumulated fault vector, $\vec{F} = [1,0,1]$ where there is more than one bit equal to one indicating a OC-fault in the top rail.

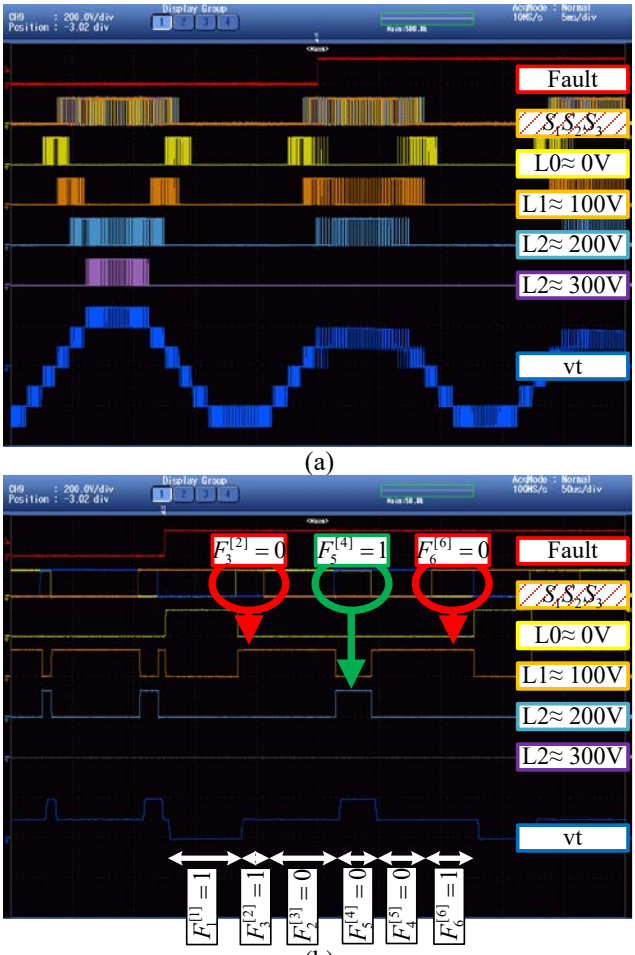


Fig. 9. OC-fault on S_3 (Top-Rail) when $100\,V < v_m < 200\,V$; (a) all signals for positive modulation (b) Zoomed signals $\vec{F} = [F_3^{[1]}, F_5^{[3]}, F_6^{[5]}] = [101]$.

VII. Conclusion

An OC fault detection and localization algorithm has been proposed for single phase stacked multicell converters. For high bandwidth output terminal voltage sensing a fast window detector circuit has been developed. By comparing the expected output voltage level and the measured voltage of PWM pulses OC faults may be detected. Measuring and comparing up to six successive PWM pulses allows the OC fault to be localized to a rail of the SMC. Two front-end routing circuits are proposed to bypass the OC fault. One configuration uses two switches one of which begins to PWM to bypass the OC fault. The second routing circuit uses three on/off switches to bypass the fault. The rail of the OC fault determines which router switches are activated and changes to the modulation waveform. With either router circuit the SMC may continue operation uninterrupted as a flying capacitor multilevel converter with the number of levels reduced by 2. An experimentally prototyped window detector circuit allows for the detection of fast PWM subcycle transitions.

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