Oscillators Utilizing Ferroelectric-Based Transistors and Their Coupled Dynamics

Niharika Thakuria, Atanu K. Saha, Sandeep K. Thirumala, Byunghoo Jung, and Sumeet K. Gupta, *Member, IEEE*

***Abstract*— We propose the application of ferroelectric (FE)-based transistors, viz., negative capacitance FET (NCFET) and Hysteretic ferroelectric FET (FEFET) in the design of coupled oscillators. The proposed oscillator utilizes hysteretic inverter voltage transfer characteristics, which is achieved by virtue of: 1) negative output conductance (NOC) in NCFETs and 2) hysteretic transfer characteristics in FEFETs. With the aid of output-to-input feedback in the inverter, we show sustained oscillations which are controllable by the gate voltage of the feedback transistor (V_{BIAS}). With focus on NCFET-based designs, we show that feedback implementation with pass transistor (PT) and transmission gate (TG) yields relaxation and sinusoid-like characteristics, respectively. Such behavior offers promises for dynamically reconfiguring the oscillator dynamics. We report the fundamental frequency (f) in the range of 12 MHz–800 MHz and 0.7 MHz–417 MHz for TG and PT implementations, respectively. We discuss how this approach can be extended to hysteretic FEFET-based designs. We also analyze coupling between two oscillators considering various strengths of coupling capacitance (C_{CP}). We establish the conditions for synchronization of f between the two oscillators with respect to difference in f and C_{CP}.**

***Index Terms*— Coupled oscillator, ferroelectric FET (FEFET), hysteresis, negative capacitance (NC), non-Boolean, Schmitt trigger.**

I. Introduction

THE CMOS-based von Neumann architectures have neared limits due to demands for increased computational ability, scalability, and sustained power. This has led to a surge in alternative paradigms of computing such as non-Boolean/neuromorphic computation for applications involving learning, matching, and recognition similar to that in neuron [1]. Several implementations of neural networks have been proposed among which oscillatory neuron networks (ONNs) are prominent [2]–[5]. This is because of the operational similarities to techniques of learning in the brain, which is accomplished by synchronization of oscillations of neuron synapses. Many applications such as pattern matching and graph coloring [3], [4] have been developed based on synchronization dynamics of oscillators.

Previously, efforts have been undertaken to design coupled oscillator-based systems with CMOS components [2]. However, the concerns of scalability in size, power, and performance have prevented them from coming to the fore. More recently, oscillators have been proposed with novel devices such as those based on electron spin [6], [7], e.g., spin-torque oscillators and correlated materials [8], [9], e.g., VO_2 and TaO_x–TiO_x. While many aspects of ONN for non-Boolean/neuromorphic computing have been researched with emerging oscillators, concerns of low power, scalability, and high frequency in such systems continue to draw attention.

Recently, steep switching devices [9]–[11] have shown promising solutions for the power-performance-scalability conflict. Among the variety of the proposed steep switching devices, ferroelectric (FE)-based negative capacitance (NC) FET (NCFET) [9], [10] has generated enormous interest as a replacement to CMOS due to its high-ON and low-OFF current enabling aggressive V_{DD} scaling for logic and SRAMs [12], [16]. Another class of FE-based transistors is hysteretic FE transistors (FEFETs) which offer several other features [13], [14] that have guided their applications in low power non-volatile memories/logic and neuromorphic computing [15], [16].

The question, therefore, arises whether efficient oscillators can be enabled with FE-based transistors that can potentially mitigate the problems associated with other technologies. If the unique properties of such transistors are ingeniously utilized to realize compact and low-power oscillators, they may result in better designs of coupled ONN. Recently, hysteretic FEFETs have been employed in designing coupled oscillators [16]. Employing capacitors in the range of nF, these oscillators display kHz range of fundamental frequency. However, their functionality and stability for smaller capacitance need further exploration to ensure their utility in high performance ONNs. Moreover, hysteretic FEFETs may limit circuit performance due to polarization switching [15] in contrast to partial polarization switching [12] in NCFETs. Partial polarization switching in NCFETs results in higher speed (lower time

Manuscript received December 19, 2018; revised February 5, 2019; accepted February 22, 2019. Date of publication March 19, 2019; date of current version April 22, 2019. This work was supported by NSF under Grant 1717999 and Grant 1814756. The review of this paper was arranged by Editor Y. Chauhan. *(Corresponding author: Niharika Thakuria.)*

The authors are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: nthakuri@purdue.edu; saha26@purdue.edu; sthirum@purdue.edu; jungb@purdue.edu; guptask@purdue.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2019.2902107

taken to partially switch polarization) and lower energy of switching (since the amount of charge switched is lower). In consequence, NCFET-based oscillators may perform better in terms of higher frequencies and energy efficiency than oscillators designed with hysteretic FEFET (in which polarization switches).

In this paper, we explore the possibility of NCFET- and FEFET-based oscillators with the focus on NCFET-based designs. We utilize the negative output conductance (NOC) of NCFET for oscillator design. To give a complete picture of implementation of the proposed oscillator, we briefly discuss the proposed oscillator with hysteretic FEFET. This paper highlights the following contributions.

1) We propose an oscillator utilizing FE-based transistor that employs the Schmitt trigger action in inverter that can be translated to voltage controlled oscillations. Such Schmitt trigger action is achieved by virtue of: a) NOC in NCFETs and b) hysteretic transfer characteristics of FEFETs.
2) Oscillations are sustained by the output–input feedback. We show that the feedback can be dynamically reconfigured to obtain distinct oscillatory characteristics, viz., relaxation or sinusoid-like dynamics.
3) We discuss device-circuit co-design of our oscillators with respect to thickness of FE (T_{FE}) and voltage (V_{BIAS}) controlling the resistance (R_f) of the feedback path.
4) We demonstrate coupling between the oscillator pairs and discuss synchronization dynamics between two oscillators with respect to V_{BIAS} and coupling capacitance (C_{CP}).

II. Modeling and Simulations

NC in NCFETs arises because of a unique relation between the electric field (E) and polarization (P) of the FE [9]. This relation can be modeled with time-dependent Landau–Khalatnikov (LK) equation [17] given as follows:

$$E = \alpha P + \beta P^3 + \gamma P^5 + \rho dP/dt \tag{1}$$

where α, β, and γ are the static Landau coefficients, and ρ is the kinetic coefficient related to the time constant associated with the change of FE polarization. Simulations in this paper are carried out using time-dependent LK equation (1) based SPICE model [18]. In the frequency limits obtained in this paper (kHz–100s of MHz shown in Section V), LK equation (which models FE as a combination of capacitor and resistor) is accurate, although for higher frequencies (THz), FE modeled as a series combination of inductor, capacitor, and resistor may be required [19]. The LK model is solved self-consistently with the 10 nm channel length Predictive Technology Model [20] for FinFETs. Si channel ($\epsilon_r = 11.9$) and 1.2-nm-thick dielectric (SiO_2, $\epsilon_r = 3.9$) are used. The model is calibrated to experiments with HZO [21] with the coefficients of LK equation as shown in Fig. 1(a).

III. Overview of Ferroelectric-Based Transistors

Here, we discuss: 1) NC [9] and NOC of NCFETs [12], [13], [22], [23] and 2) hysteretic transfer characteristics (I_D–V_{GS}) of FEFETs [24], [25] in context of the proposed oscillator.

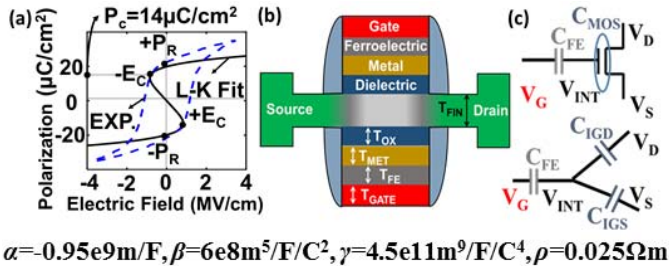

Fig. 1. (a) *P–E* loop of the FE capacitor showing occurrence of NC in FE material (HZO) calibrated with experimental data [21]. (b) Schematic of FEFET cross section [18]. (c) Circuit model of FEFET [12].

A. NOC in NCFETs and Hysteretic Inverters

For sufficiently low-FE thickness (T_{FE}) (but which is greater than critical thickness of HZO to show ferroelectricity), operation of FE-based transistors can be stabilized in the NC regime leading to steep switching [9], [10], [12], [13], [22], [23]. Aziz *et al.* [18] show that the limiting condition of T_{FE} for non-hysteretic NC behavior is given by

$$T_{FE} < A_{FE}/(|\alpha| C_{MOS}) \tag{2}$$

where A_{FE} is the area of the FE, and α is a coefficient of the LK equation. The interactions of NC (C_{FE}) of FE layer with positive capacitances of the underlying FET manifest as gate coupling ($\eta \times dV_{GS}$) and drain coupling ($\eta_D \times dV_{DS}$) as explained in [12] corresponding to the circuit model [Fig. 1(c)] for $C_{FE} < 0$.

$$dV_{INT} = \eta dV_{GS} - \eta_D dV_{DS} = \frac{|C_{FE}| dV_{GS}}{|C_{FE}| - C_{IGS} - C_{IGD}} - \frac{C_{IGD} dV_{DS}}{|C_{FE}| - C_{IGS} - C_{IGD}} \tag{3}$$

where V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltages. C_{IGS} and C_{IGD} represent the overall source and drain capacitive coupling in the underlying transistor [Fig. 1(c)], including fringing, dielectric, and other capacitances. V_{INT} represents the potential at the intermetal layer [for metal ferroelectric metal insulator semiconductor (MFMIS) gate stack—Fig. 1(b)] and the effective potential at the interface of FE and dielectric (for the metal ferroelectric insulator semiconductor (MFIS) stack within single-domain approximation). This is based on the understanding that polarization response in MFIS is a collective effect due to the effective electric field (E) [26]. Note that, device features of NCFETs that we discuss are not limited to single domain response but are also exhibited by multi domain NCFETs [26].

To understand NOC, let us consider (3). If drain coupling ($\eta_D \times dV_{DS}$) dominates the gate coupling ($\eta \times dV_{GS}$), V_{INT} decreases with increasing V_{DS} leading to NOC [Fig. 2(a)]. Such a condition arises for: 1) sufficiently low $|C_{FE}|$ [or high T_{FE} but still meet the inequality (2)]; 2) high V_{DS} (where the effect of E on I_D saturates); and 3) low V_{GS}. Here, we observe that with the simulation parameters considered for this paper,

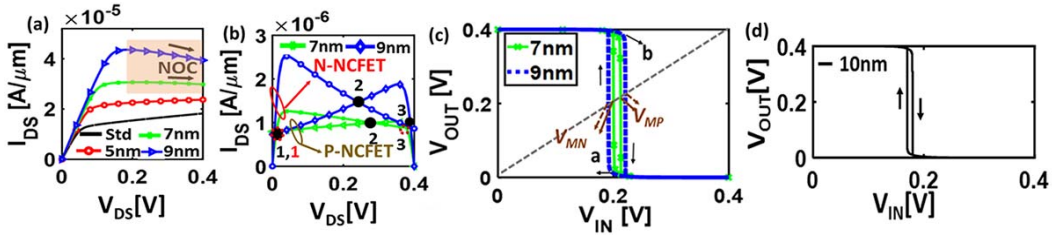

Fig. 2. (a) Output (I_D–V_{DS}) characteristics of standard FET and NCFET. NCFET with $T_{FE} \geq 7$ nm shows NOC. (b) Load line of NCFET inverter for T_{FE} (≥7 nm) at $V_I = V_{DD}/2$. Due to NOC for large V_{DS}, I_{DS} of N-NCFET lowers, and I_{DS} of P-NCFET lowers when V_{DS} decreases. This results in multiple intersections. (c) VTC of NCFET-based inverter for $T_{FE} \geq 7$ nm. (d) VTC of inverter with P-FinFET and N-NCFET ($T_{FE} = 10$ nm).

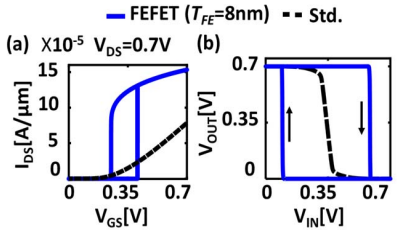

Fig. 3. (a) Hysteretic FEFET transfer characteristics (I_D–V_{GS}). (b) VTC of hysteretic FEFET-based inverter for $T_{FE} = 8$ nm.

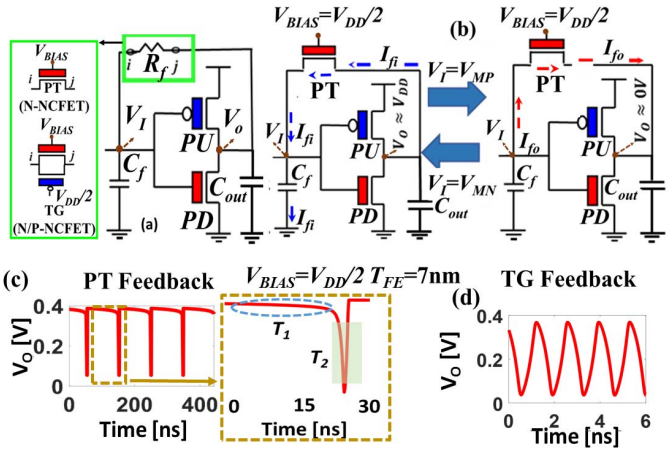

Fig. 4. (a) Schematic of NCFET inverter-based oscillator with PT and TG as R_f. (b) Sequence of operation of oscillatory behavior. (c) and (d) Transient waveform of oscillator with PT-/TG-NCFET as feedback resistor for $V_{BIAS} = V_{DD}/2$ and $T_{FE} = 7$ nm.

NOC occurs for $T_{FE} \geq 7$ nm [Fig. 2(a)] and increases with T_{FE} [12], [23].

NOC in NCFETs leads to hysteretic inverter voltage transfer characteristics (VTC) [12], [13], [22] [Fig. 2(c)] which is explained through multiple intersections in load line of P-/N-NCFET [similar to 1, 2, and 3 as marked in Fig. 2(b) for $T_{FE} \geq 7$ nm]. Enhanced NOC with increase in T_{FE} leads to larger hysteresis window [$\sim \Delta V_M = V_{MP} - V_{MN}$ shown in Fig. 2(c)] [12], [13], [22]. Also, the hysteretic VTC can be obtained in an inverter with 1-NCFET and 1-FinFET, albeit for higher T_{FE} (≥9 nm) [Fig. 2(d) with $T_{FE} = 10$ nm]. This expands the design options for our oscillator depending on the design target and technological capabilities.

B. Hysteretic FEFETs

In addition to NCFETs, FE-based gate stacks can be utilized to obtain hysteretic I_D–V_{GS} [Fig. 3(a)] in FEFETs. Experiments [24], [25] have demonstrated such characteristics, targeted toward memory/synapse designs [15], [16]. This is typically observed for T_{FE} larger than the critical value given by the right-hand side (RHS) of (2). Moreover, the capacitance of the underlying transistor (C_{MOS}) is optimized to reduce the RHS of (2) to achieve hysteresis with reasonable T_{FE}. By proper gate work-function engineering, hysteresis can be shifted to $|V_{GS}| > 0$ region [16], which proves to be helpful in the design of FEFET-based hysteretic inverter. Such an FEFET has been demonstrated experimentally [24], [25]. Here, we analyze an inverter designed with P-/N-FEFET showing hysteretic VTC [Fig. 3(b)]. Such a design can be used for the proposed oscillator design similar to the NCFET inverter-based oscillator design.

To sum up, hysteretic VTCs are exhibited by: 1) NCFET inverter; 2) inverter with 1-NCFET/1-FinFET; and 3) hysteretic FEFET inverters [Figs. 2(c) and (d) and 3(b)]. However, the underlying mechanisms and design windows for T_{FE} are different. While NOC in NCFET leads to hysteresis in VTC in 1) and 2), inherent hysteretic I_D–V_{GS} in FEFETs is the prime reason for the same in 3). Hysteretic VTC is observed in NCFET inverter for $T_{FE} \geq 7$ nm [Fig. 2(c)] and $T_{FE} \geq 9$ nm in 1-NCFET/1-FinFET inverter [Fig. 2(d)]. For FEFET inverter, $T_{FE} \geq 8$ nm [Fig. 3(b)] along with other device optimizations (as described in the previous paragraph) leads to hysteretic inverter characteristics. FEFET inverters show the wider hysteresis compared to NCFET inverter or 1-NCFET and 1-FinFET inverter.

In summary, NOC in NCFETs and hysteresis in FEFETs lead to the Schmitt Trigger action with two transistors compared to six transistors in the CMOS design [27]. This offers compact solutions for designs based on the Schmitt trigger. In this paper, we utilize this feature for the design of low area oscillators.

IV. NCFET Oscillator

With the understanding of hysteretic NCFET inverter behavior, we now present the proposed oscillator. The schematic of the oscillator is shown in Fig. 4(a). Our design utilizes the Schmitt trigger action in NCFET inverter and a feedback between inverter input and output to obtain sustained oscillations. Feedback resistor (R_f) can be implemented with

N-/P-NCFET pass transistor (denoted by PT) or NCFET transmission gate (TG) shown in Fig. 4(a). R_f can be tuned through the gate bias V_{BIAS}. Feedback capacitance C_f shown in Fig. 4(a) consists of two components: 1) input capacitance of the NCFET inverter (C_{INV} which is dependent on T_{FE}) and 2) other components, e.g., wire capacitance/fixed capacitance lumped as C_{DES} that may be added for achieving sustainability of oscillations. Similarly, output capacitance C_{out} is representative of two cumulative capacitances: 1) drain capacitance of transistors in inverter (pull up and pull down) and PT/TG (C_{drain}) and 2) any additional capacitance ($C_{\mathrm{O,DES}}$).

The operation of the proposed oscillator is described as follows and is illustrated in Fig. 4(b). To begin with, let the feedback path (PT/TG) be open ($V_{\mathrm{BIAS}} = 0$ V), input voltage $V_{\mathrm{I}} = 0$ V, and output voltage $V_{\mathrm{O}} = V_{\mathrm{DD}}$. When the feedback path is established ($V_{\mathrm{BIAS}} > 0$), V_{I} starts to increase due to charging of C_f by current I_{fi} [Fig. 4(b)]. This continues till V_{I} reaches V_{MP}, at which point, V_{O} flips to 0 V. Note that, V_{MP} refers to V_{I} for which V_{O} trips from $V_{\mathrm{DD}} \rightarrow 0$ [Fig. 2(c)]. Now, the current direction through the feedback path reverses (I_{fo} flows from V_{I} to V_{O}) and therefore, C_f starts to discharge V_{I}. After V_{I} reaches V_{MN}, V_{O} returns to V_{DD}. V_{MN} refers to the input voltage of the inverter (V_{I}) for which the output voltage (V_{O}) changes from $0 \rightarrow V_{\mathrm{DD}}$. This process repeats to generate sustained oscillations, which is a result of V_{I} transitioning between V_{MP} and V_{MN}.

Fig. 4(c) and (d) shows the waveforms for the PT (N-NCFET) and TG-based implementations of R_f. While Fig. 4(c) shows relaxation-type characteristics, the oscillations shown in Fig. 4(d) are sinusoid-like. To understand this behavior, let us begin our discussion with PT-based R_f. The relaxation-type waveform [Fig. 4(c)] results due to the asymmetry in transition time for $V_{\mathrm{MP}} \rightarrow V_{\mathrm{MN}}$ and $V_{\mathrm{MN}} \rightarrow V_{\mathrm{MP}}$. This can be further explained by analyzing the inset of Fig. 4(c). Let $V_{\mathrm{O}} = V_{\mathrm{DD}}$ and $V_{\mathrm{I}} = V_{\mathrm{DD}}/2$. V_{O} charges C_f with current I_{fi} until $V_{\mathrm{I}} = V_{\mathrm{MP}}$ is reached through PT feedback. It is evident from the inset of Fig. 4(c) (marked as T_1) that a large time constant (τ_f) of PT is involved in this process. Inspection of the bias conditions of the PT suggests that due to small V_{GS} and V_{DS} ($V_{\mathrm{BIAS(G)}} \sim V_{\mathrm{DD}}/2$ (or V_{MN}), $V_{\mathrm{DD}}/2 < V_{\mathrm{I}(S)} < V_{\mathrm{MP}}$, and $V_{\mathrm{O}(D)} \sim V_{\mathrm{DD}}$), it conducts with large R_f. When $V_{\mathrm{I}} = V_{\mathrm{MP}}$, the inverter transitions to low logic output ($V_{\mathrm{O}} = 0$). We refer to this transition ($V_{\mathrm{I}} = V_{\mathrm{MN}} \rightarrow V_{\mathrm{MP}}$) as T_1. Now, the feedback PT will act to discharge V_{I} due to I_{fo} flowing from V_{I} to V_{O}. It is biased at $V_{\mathrm{GS}} = V_{\mathrm{DD}}/2$ and $V_{\mathrm{DS}} \sim V_{\mathrm{DD}}/2$ ($V_{\mathrm{BIAS(G)}} = V_{\mathrm{DD}}/2$, $V_{\mathrm{O}(S)} \sim 0$, and $V_{\mathrm{MP}} < V_{\mathrm{I}(D)} < V_{\mathrm{MN}}$) indicating a low R_f state. Hence, V_{I} transitioning phase ($V_{\mathrm{I}} = V_{\mathrm{MP}} \rightarrow V_{\mathrm{MN}}$) of the oscillator as T_2. Again V_{O} discharges with high R_f and τ_f until V_{I} reaches V_{MP} (T_1 transition phase). Repetition of T_1 and T_2 results in oscillations.

Due to much higher transition time of $V_{\mathrm{MN}} \rightarrow V_{\mathrm{MP}}$ ($t_{\mathrm{MN}\rightarrow\mathrm{MP}}$) than that for $V_{\mathrm{MP}} \rightarrow V_{\mathrm{MN}}$($t_{\mathrm{MP}\rightarrow\mathrm{MN}}$), relaxation oscillations are observed. On the other hand, TG-based implementation of R_f displays symmetric sinusoid-like characteristics. In this configuration, we apply V_{BIAS} at the gate of the N-NCFET of the TG and fix the gate of the P-NCFET to $V_{\mathrm{DD}}/2$ [Fig. 4(a)]. We know from the discussion of PT R_f-based oscillator that in T_1, R_f due to PT only is large. However, in TG implementation due to the bias conditions of P-NCFET: $|V_{\mathrm{GS}}| = |V_{\mathrm{DS}}| = V_{\mathrm{DD}}/2$ ($V_{\mathrm{BIAS}(G)} = V_{\mathrm{DD}}/2$, $V_{\mathrm{O}(S)} \sim V_{\mathrm{DD}}$, and $V_{\mathrm{I(D)}} \sim V_{\mathrm{DD}}/2$), low R_f state is achieved in T_1. During T_2, low feedback resistance condition prevails by virtue of N-NCFET in T_2 (similar to the PT-based design). Thus, TG feedback implementation ensures low R_f during $V_{\mathrm{MN}} \rightarrow V_{\mathrm{MP}}$ and $V_{\mathrm{MP}} \rightarrow V_{\mathrm{MN}}$. This results in almost symmetric transition for input charging and discharging, yielding "sinusoid-like" oscillator [Fig. 4(d)]. The same argument holds in case of an oscillator with purely resistive feedback that shows "sinusoid-like" characteristics.

Note that, the run-time reconfiguration of the oscillation dynamics between the relaxation-type and sinusoid-like can be enabled using bias of P-NCFET in the feedback path. If gate of P-NCFET is $V_{\mathrm{DD}}/2$, the feedback acts as a TG yielding sinusoid-like characteristics while by setting it to V_{DD} (P-NCFET is OFF), the feedback is reduced to PT, leading to relaxation behavior. Thus, the proposed oscillator allows dynamic reconfigurability while offering a more compact implementation compared to standard CMOS designs. The proposed design can also be realized with hysteretic FEFETs (see Section VI) although our focus is on non-hysteretic NCFETs (exhibiting NOC) due to their faster and more energy efficient nature [12].

V. Analysis of NCFET Oscillator

The fundamental frequency (f) for TG and PT is 734 MHz and 13.4 MHz for $V_{\mathrm{DD}} = 0.4$, $V_{\mathrm{BIAS}} = V_{\mathrm{DD}}/2$, $C_f = 5.2$ fF, $C_{\mathrm{out}} = 0.24$ fF, and $T_{\mathrm{FE}} = 7$ nm. Recall from Fig. 2(c) that for $T_{\mathrm{FE}} \geq 7$ nm NCFET inverter shows the hysteretic VTC that is utilized for our oscillator design (refer to Section IV). More details about calculation of C_f and C_{out} are provided in Section V-C. It is noteworthy that TG-based design yields higher f (55X) than PT implementation due to lower charging time ($t_{\mathrm{MP}\rightarrow\mathrm{MN}}$) in the former.

We further explore the performance of the proposed oscillator to understand the impact of various device-circuit characteristics. The oscillation frequency f depends on two factors: 1) time constant ($\tau_f = R_f C_f$) of the feedback path and 2) hysteresis in VTC (ΔV_M) of inverter. An increase in τ_f lowers f due to larger charging/discharging time of V_{I}. Independently, an increase in ΔV_M implies increase in time for $V_{\mathrm{MN}} \rightarrow V_{\mathrm{MP}}$ transition and vice versa due to larger voltage swing, yielding lower f. With these factors in mind, we analyze the oscillator characteristics for different design parameters.

A. Voltage Controllability of Frequency

Here, we discuss voltage (V_{BIAS}) controllability of f for PT- and TG-based designs. By increasing V_{BIAS}, we modulate τ_f(R_f and C_f) while maintaining a constant ΔV_M. An increase in V_{BIAS} leads to: 1) lower R_f and 2) higher C_f. To understand this further, note that, in the NC regime of NCFET, the effective gate capacitance of device (C_{fg}) is a combination of the 1) NC-induced amplification (η) and 2) capacitance of the underlying transistor ($C_{\mathrm{IGD}} + C_{\mathrm{IGS}}$) given

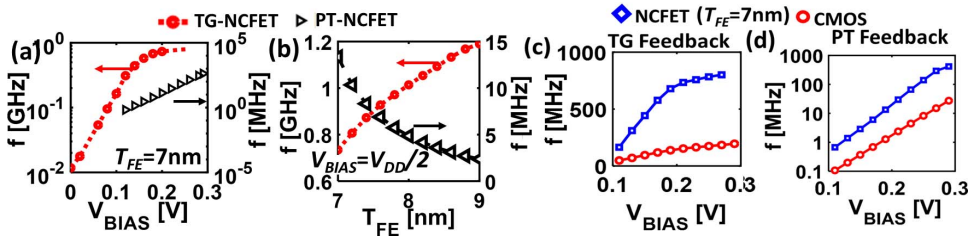

Fig. 5. Variation of NCFET oscillator frequency f with (a) feedback control voltage V_{BIAS}, (b) FE thickness T_{FE}, and (c) and (d) Comparison of f of NCFET oscillator versus CMOS oscillator for varying V_{BIAS}.

by $C_{fg} = \eta \times (C_{IGS} + C_{IGD})$ [12]. As V_{GS} rises, η increases (in the range of V_{GS} = 0–0.4 V for LK coefficients in this paper). Also, $C_{IGD} + C_{IGS}$ increases with V_{GS}. Both these factors yield higher C_{fg}. The details of this are in [12]. But decrease in R_f dominates over increase in C_{fg} in both PT and TG design, since C_f is composed of components other than C_{fg}, e.g., C_{DES} (see Section IV). Note that, C_{fg} contributes to C_{INV} (from Section IV). Hence, an increase in f with increase in V_{BIAS} is achieved.

Having understood the impact of V_{BIAS} on f, let us now analyze the range of V_{BIAS} and corresponding f of successful oscillatory operation [Fig. 5(a)]. The PT oscillator successfully oscillates when 0.12 V $< V_{BIAS} <$ 0.29 V. For $V_{BIAS} <$ 0.12 V, the oscillations cannot be sustained since PT fails to turn on to establish the feedback path. When $V_{BIAS} >$ 0.29 V, τ_f is exceedingly small and the delay associated with the feedback is smaller than the delay in inverter switching. This leads to degradation of the input voltage with oscillations completely damping after some time. On the other hand, for TG design, the range of V_{BIAS} for which oscillations are achieved is 0 V $< V_{BIAS} <$ 0.26 V. We explain the difference between TG and PT oscillator design in this regard as follows. Due to fixed biasing of P-NCFET gate at $V_{DD}/2$ [Fig. 4(a)], a feedback path is present for all V_{BIAS} in the TG. Therefore, even when V_{BIAS} is small (<0.12 V), TG-based design yields oscillation (whereas PT-based oscillator becomes nonfunctional). However, at high V_{BIAS} (>0.26 V), the concerted effect of N-NCFET and P-NCFET in TG makes τ_f comparable to the inverter delay leading to unsustained oscillations in the TG design. On the other hand, the PT design allows greater flexibility in the high V_{BIAS} region due to higher feedback delay. Therefore, while tuning range of PT design is 0.12 V $< V_{BIAS} <$ 0.29 V, for TG implementation, this range is 0 V $< V_{BIAS} <$ 0.26 V. f in the respective ranges can be tuned between 12 MHz and 800 MHz for TG and 0.7 MHz–417 MHz for PT implementations, respectively. It may be reiterated that in addition to V_{BIAS}-controlled f, the oscillation type can also be dynamically reconfigured using the gate bias of the P-NCFET, which could open avenues for new applications.

Finally, we compare the performance of the proposed NCFET oscillator to the CMOS Schmitt trigger-based oscillator (also mentioned in Section III). f of CMOS TG oscillator is ∼5X lower than NCFET TG type [Fig. 5(c)], whereas CMOS PT oscillator is ∼10X lower than NCFET PT-based oscillator [Fig. 5(d)]. Lower f is due to larger ΔV_M in CMOS-based Schmitt trigger and higher R_f of the standard FinFET-based feedback compared to R_f of NCFET feedback.

B. Impact of T_{FE} and C_f on Frequency (f)

Let us begin by analyzing the impact of FE thickness T_{FE} on f. Increase in T_{FE} results in: 1) higher I_D [Fig. 2(a)] or lower R_f; 2) larger ΔV_M [Fig. 2(c)]; and 3) larger gate capacitance of the NCFET due to negative C_{FE} [12], which increases C_f. To explain the overall impact, we compare PT- and TG-based designs [Fig. 4(a)]. While for PT oscillator, increase in T_{FE} reduces f, TG-based design shows an increasing trend [Fig. 5(b)]. We explain these trends as follows.

Let us begin with PT-based feedback. Recall from the prior discussion in Section IV that $V_{BIAS} = V_{DD}/2$ for PT results in low f of the oscillator due to large $t_{MN\rightarrow MP}$. For V_{DD} = 0.4 V, V_{BIAS} = 0.2 V and PT are biased in the near-threshold region, and its drive strength is low. Hence, although I_D increases with increase in T_{FE} [Fig. 2(b)], the increase in ΔV_M [Fig. 2(c)], and C_f is much more impactful. In other words, in PT-based oscillator, the effect of ΔV_M dominates over increase in I_D resulting in decrease in f with increasing T_{FE}.

Considering the case of a TG feedback-based oscillator, for $V_{BIAS} = V_{DD}/2$ either P-NCFET/N-NCFET ensures that R_f is always low (or the feedback NCFET is strong as discussed in Section IV). More specifically, since the feedback transistor is now operating at $V_{DS} \geq V_{DD}/2$, I_D–V_{DS} [Fig. 2(a)] suggests significant increase in I_D with increase in T_{FE} for the said bias condition. Hence, for the same increase in ΔV_M, the reduction in R_f with T_{FE} increase is more effective in TG compared to PT due to the concerted action of P- and N-devices in the former. Thus, for TG design, decrease in R_f dominates over ΔV_M increase leading to an increase in f with increasing T_{FE}.

As T_{FE} increases from 7 nm to 9 nm, f decreases by 5.5X (from 13.3 to 2.4 MHz) in PT implementation, whereas f increases by 1.6X (734 MHz–1190 MHz) as shown in Fig. 5(b).

Since τ_f also affects C_f, (due to C_{INV} described in Section IV), an independent analysis of the dependence of oscillation dynamics on C_f becomes important. This is because C_f not only depends on T_{FE} (the overall effect of which we have already discussed) but may also be tuned by optimizing other components and even adding an additional capacitor (C_{DES}). It may be noted that since the primary driving mechanism for oscillations in our design is repeated

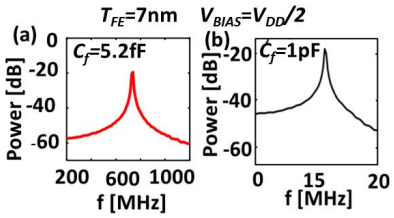

Fig. 6. Power spectrum of NCFET TG oscillator for (a) low (5.2 fF) feedback capacitance C_f and (b) high (1 pF) C_f.

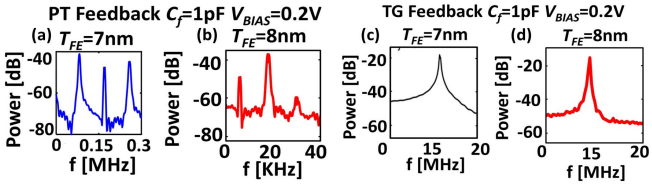

Fig. 7. Power spectrum of oscillator (a) and (b) with PT as R_f and (c) and (d) TG as R_f for $C_f = 1$ pF in both cases.

transitions of V_I between V_{MN} and V_{MP} (which, in turn, depends on charging/discharging of C_f, as explained earlier), C_f plays a more important role in determining the characteristics of voltage-controlled oscillations than C_{out}. Since both C_f and C_{out} show the similar trends with respect to f, we focus on analyzing the dependence of f on C_f. As expected, f decreases from 13.4 MHz to 0.12 MHz as C_f increases from 5.2 fF to 1 pF for TG implementation. For TG, f decreases from 734 MHz to 16 MHz as C_f increases from 5.2 fF to 1 pF. Simultaneously, an increase in C_f leads to better sustenance of oscillations for a wider range of design parameters. Thus, depending on application requirements (higher f/robustness), proper C_f can be chosen. To analyze the impact of C_f on the robustness of oscillator, we examine the power spectrum in Section V-C.

C. Output Power Spectrum

The output power spectrum is a widely accepted measure of robustness to noise [28]. A higher peak indicates more resilience. Here, the robustness of the oscillator is a function of C_f (comprising C_{INV} and C_{DES} described in Section IV). For NCFET TG design at $T_{FE} = 7$ nm and $V_{BIAS} = 0.2$ V, $C_f = 5.2$ fF ($C_{INV} = 0.2$ fF, $C_{DES} = 5$ fF, and $C_f = 5.2$ fF) results in a peak power of -20 dB [Fig. 6(a)] at 734 MHz, while for $C_f = 1$ pF ($C_{INV} = 0.2$ fF, $C_{DES} = 1$ pF, and $C_f \sim C_{DES}$, since $C_{INV} \ll C_{DES}$), the observed peak power is -18 dB at 16 MHz [Fig. 6(b)]. Thus, higher C_f enhances robustness of the oscillator. Note that, oscillations are sustained with desirable power (≤ -20 dB) when fixed capacitances $C_{DES} \geq 5$ fF and $C_{O,DES} \geq 0.1$ fF. In addition, C_{INV} (averaged over voltage) is 0.2–0.25 fF for $T_{FE} =$ 7–8 nm (hence $C_f = 5.2$ fF) and capacitance at the inverter output = 0.14 fF (total $C_{out} = 0.24$ fF).

To reinforce the understanding of power spectrum of the proposed designs, we analyze the power spectrum of the proposed oscillators (PT and TG) for a different T_{FE}. Note that C_{INV} depends on T_{FE}. Fig. 7 shows the sharp and narrow

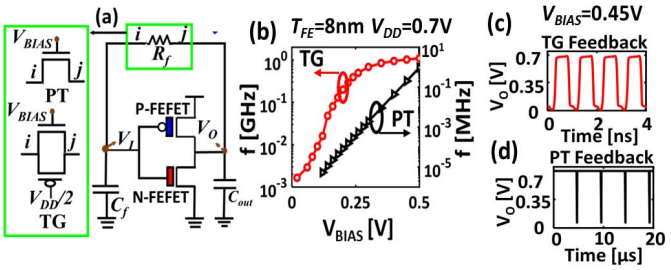

Fig. 8. (a) Schematic of FEFET ($T_{FE} = 8$ nm) inverter-based oscillator with P-/N-FEFET and FinFET-based PT/TG feedback (R_f). (b) Variation of oscillator f with V_{BIAS}. (c) and (d) Transient waveform of FEFET oscillator with PT/TG feedback.

peaks in the spectrum. The maximum peak values are -39 dB and -18 dB for PT and TG ($T_{FE} = 7$ nm) oscillator [Fig. 7(a) and (c)], respectively. Due to the relaxation-type behavior of the PT-based oscillators, distinct sidelobes in the power spectrum are observed [28]. Furthermore, on increasing T_{FE}, the spectrum peaks at lower oscillation frequency (f) for the PT design. For the TG implementation, increasing T_{FE}shows increase in robustness [Fig. 7(c) and (d)]. The discussions in this section related to frequency and power spectrum considering device–circuit parameters can guide optimization of the proposed oscillator depending on the design targets.

To conclude this discussion, we compare this paper with the previous reporting of FEFET oscillator [16]. For proper comparisons, we obtain the coercive field and remnant polarization of FE and capacitances (~8 nF) from [16] and redesign our oscillator with the same parameters. However, since the value of viscosity coefficient (ρ) is not available in [16], we perform simulation for our design using a rather conservative value $\rho = 2.5\ \Omega\cdot$cm (compared to 0.18 $\Omega\cdot$cm reported in [19]). For such a value of ρ, the polarization switching rates of the order of GHz are expected. Since oscillators in this comparative study show f in KHz-MHz (due to nF of capacitance), the influence of ρ on f is negligible. The oscillator in [16] shows maximum $f = 12$ kHz and -20 dB power with 8 nF capacitance. In comparison, at $C_f = 8$ nF, the proposed TG oscillator displays a more robust design with -6.3 dB power at $f = 6.72$ kHz. At iso-power of -20 dB, the TG implementation displays higher f (=15 MHz with $C_f = 1$ pF) compared to 12 kHz in [16]. The referred design does not throw light on its performance at lower capacitance; hence, its high f operation needs to be further examined. On the other hand, our design can work for capacitances of the order of several fF. In terms of voltage controllability, the maximum reported range in [16] is 0.2–0.36 V ($f = 5$ kHz $-$ 12 kHz) compared to 0–0.26 V ($f = 80$ kHz–20 MHz). Moreover, our design displays dynamic reconfigurability between oscillation types while incurring an overhead of two more NCFETs (for the TG design) compared to the referred design in [16]. Finally, the proposed oscillator can be designed with hysteretic FEFETs as well as non-hysteretic NCFETs (exhibiting NOC), and is, therefore, more generic than [16], which is limited to the hysteretic regime. While the focus of this paper is on NCFET-based oscillators, we briefly discuss how the

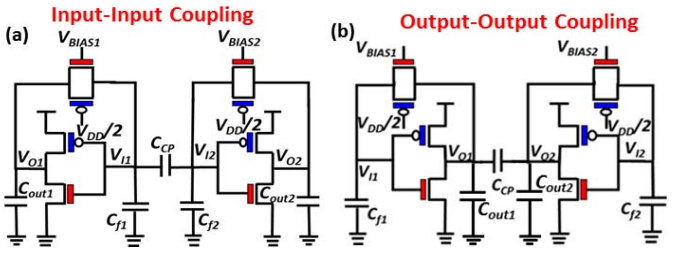

Fig. 9. Schematic of NCFET TG coupled oscillator for (a) input–input coupling and (b) output–output coupling.

proposed technique can also be applied to hysteretic FEFETs in Section VI.

VI. FEFET-Based Oscillator

Hysteretic FEFET-based inverter can show hysteretic VTC [Fig. 3(b)] for $T_{FE} \geq 8$ nm (refer to Section III). Therefore, oscillations can be sustained by providing a feedback from output to input [Fig. 8(a)] similar to that in NCFET oscillator. Here, we analyze the oscillator with FinFET-based feedback designed with PT and TG. Voltage controllability of f is achieved through V_{BIAS} [Fig. 8(b)]. Also, reconfigurability is observed between the pulse-like [Fig. 8(c)] and relaxation characteristics [Fig. 8(d)] for TG and PT designs. The pulse-like waveforms of FEFET TG are seen due to sharp polarization switching as opposed to partial polarization switching in NCFET TG which gives rise to sinusoid-like waveforms. PT implementation shows oscillations for $V_{BIAS} = 0.12$–0.5 V with $f = 5.36$ Hz–0.97 MHz, while for TG design oscillations are observed for $V_{BIAS} = 0.0$–0.5 V with $f = 0.9$ MHz–1.1 GHz [Fig. 8(b)]. Comparing Fig. 8(b) with Fig. 5(a), we observe that both PT and TG NCFET oscillator show higher f (even at lower V_{DD}) than respective PT/TG implementation of FEFET oscillator due to polarization switching in the latter.

VII. Coupling Between NCFET-Based Oscillators

In non-Boolean computation, coupled oscillators provide solution to complex problems like pattern matching [3]. In pattern matching, the extent of synchronization between oscillators is studied to determine the closeness of two patterns. The input of one of the oscillators corresponds to the input pattern, and the input to the other is the pattern to be identified.

Considering the importance of coupled oscillators for such applications, we now discuss the coupling dynamics between the two oscillators (Fig. 9) with a focus on NCFET designs. We consider natural frequencies f_1 and f_2 corresponding to inputs V_{BIAS1} and V_{BIAS2}, respectively.

Coupling is achieved via a coupling capacitor (C_{CP}) in either input–input (V_{I1}–V_{I2}) [Fig. 9(a)] or output–output (V_{O1}–V_{O2}) [Fig. 9(b)] configurations. We show that coupling of V_{I1}–V_{I2} results in out-of-phase (180°) frequency locking. Interestingly, frequency locking is in-phase (0°) for V_{O1}–V_{O2} coupling.

Let us start our discussion with TG oscillators for V_{I1}–V_{I2} coupling. Before coupling, we set the fundamental frequencies $f_1 = 734$ MHz and $f_2 = 760$ MHz corresponding to

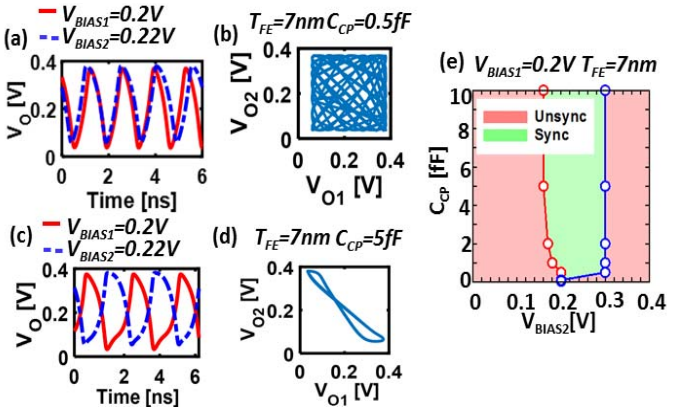

Fig. 10. Transient waveform and phase map for (a) and (b) $C_{CP} = 0.5$ fF and (c) and (d) $C_{CP} = 5$ fF. (e) Synchronization map of the oscillator for V_{I1}–V_{I2} coupling in NCFET TG oscillator.

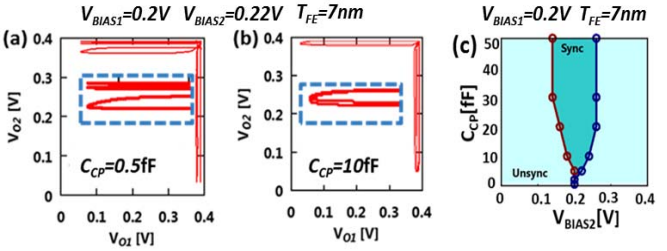

Fig. 11. (a) and (b) Phase map for $C_{CP} = 0.5$ fF and $C_{CP} = 10$ fF. (c) Synchronization map of the oscillator for NCFET PT V_{I1}–V_{I2} coupled oscillator.

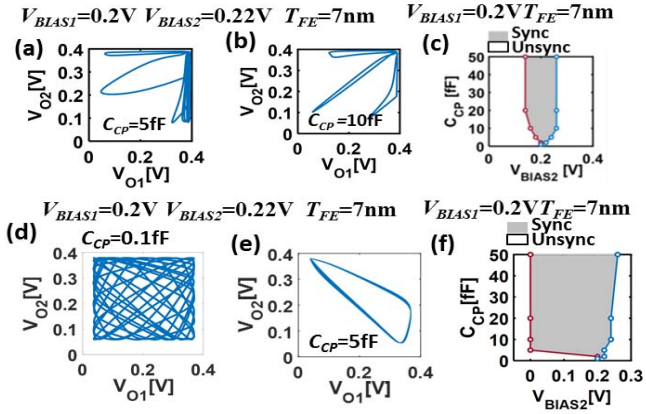

Fig. 12. (a)–(c) V_{O1}–V_{O2} coupling phase map for $C_{CP} = 5$ fF and 10 fF and synchronization map of NCFET PT oscillators. (d)–(f) Phase map for $C_{CP} = 0.1$ fF and 5 fF and synchronization map of NCFET TG oscillators.

$V_{BIAS1} = 0.2$ V and $V_{BIAS2} = 0.22$ V. Hence, both the waveforms are unsynchronized in frequency and phase. By introducing $C_{CP} = 5$ fF, the oscillators become out-of-phase frequency locked with synchronized frequency of $f_S = 360$ MHz [Fig. 10(c)]. Once the synchronization is achieved, the relative phase of the oscillators can be modulated via C_{CP}. Correspondingly, the transition of the lobes in the phase map of the synchronized outputs indicates the modulation in phase [Fig. 10(d)]. When $C_{CP} = 0.5$ fF is small, it represents an unsynchronized state [Fig. 10(a)] without any fixed trajectory in the phase map [Fig. 10(b)]. The extent of synchronization of the two oscillators depends on the strength of the coupling

TABLE I
COMPARISON OF EMERGING OSCILLATORS FOR NON-BOOLEAN APPLICATION

Oscillator characteristics	This work		[16]	[8]	[6]	[9]	[29]
Device	NCFET	Hysteretic FEFET	Hysteretic FEFET	VO_2	$Ta/Cu/Co_{90}Fe_{10}/Cu/Ni_{80}Fe_{20}/Cu/Au$	TaO_x	CMOS
Oscillator mechanism	NOC in NCFET →Hysteretic VTC in inverter	Hysteretic transfer characteristic of FEFET	Hysteretic transfer characteristics in FEFET	Insulator to Metal Transition	Spin torque	Filament formation and dissolution dynamics	Ring oscillator
Oscillator type	Relaxation (PT) and Sinusoid-like (TG)	Relaxation (PT) and Pulse-like (TG)	Relaxation	Relaxation	Sinusoid-like	Relaxation	Sinusoid-like
Reconfigurability in oscillations	Yes	Yes	No	No	No	No	No
Oscillation frequency	12MHz-800MHz (TG)	0.9MHz-1.1GHz (TG)	5KHz-12KHz	10KHz-1MHz	15.1GHz-15.6GHz	10MHz -500MHz	0.25GHz-3.8GHz
	0.7MHz-417MHz (PT)	5.36Hz-0.97MHz (PT)					
Control voltage/current	0V-0.26V (TG)	0V-0.5V (TG)	0.2V-0.36V	0.1-0.8V	6-12mA	-2V–(-4V)	0-1.3V
	0.12-0.29V (PT)	0.12-0.5V (PT)					
Fixed Capacitance used	5fF	5fF	8nF	--	--	10pF	Device capacitance
Compactness	Average (4 Transistors, 2 capacitor)	Average (4 Transistors, 2 capacitor)	High (2 Transistors, 1 capacitor)	High (1 Transistor/ Resistor, VO_2)	--	High (1 Transistor/ Resistor, TaO_x)	Low (12 Transistors)
Power	<-20dB	<-20dB	<-20dB	<-20dB	--	--	--

and how far apart f_1 and f_2 are set. It is already known to the reader that, in this paper, f is the voltage controlled through V_{BIAS}. Hence, we study the limits of synchronization in terms of coupling strength and frequency difference by plotting C_{CP} versus V_{BIAS2}, while V_{BIAS1} is constant in Fig. 10(e). This plot provides the information about the required coupling strength as a function of $\Delta V_{\mathrm{BIAS}} = |V_{\mathrm{BIAS2}} - V_{\mathrm{BIAS1}}|$. The range of $\Delta f (= f_1 - f_2)$ or ΔV_{BIAS} for which synchronization can be achieved also increases with C_{CP}, as shown in Fig. 10(e).

In NCFET PT feedback oscillators, synchronization is achieved for $C_{\mathrm{CP}} \sim 10$ fF which is reflected as fixed lobes in the phase map in the inset of Fig. 11(b). At low coupling strength ($C_{\mathrm{CP}} \sim 0.5$ fF), multiple paths in the phase map [inset of Fig. 11(a)] are observed indicating the unsynchronized state. Fig. 11(c) shows that $C_{\mathrm{CP}} > 20$ fF determines the range of V_{BIAS2} over which synchronization is achieved. In this case, $V_{\mathrm{BIAS2}} = 0.14$–$0.26$ V represents the synchronized state. The range of ΔV_{BIAS} for which frequency synchronization is achieved is smaller for PT oscillator than TG oscillator.

Here, we explore synchronization dynamics of in-phase coupling in V_{O1}–V_{O2}. PT and TG oscillators show the unsynchronized state for $C_{\mathrm{CP}} = 5$ fF (with multiple lobes) and 0.1 fF [Fig. 12(a) and (d)], respectively. By increasing C_{CP} to 10 fF for PT [Fig. 12(b)] and 5 fF for TG [Fig. 12(e)], synchronization is achieved. Synchronization is achieved for $V_{\mathrm{BIAS2}} = 0.14$–$0.26$ V in PT oscillator [Fig. 12(c)] and $V_{\mathrm{BIAS2}} = 0$–0.26 V in TG oscillator [Fig. 12(f)] when $C_{\mathrm{CP}} > 20$ fF for both cases. Again, TG shows greater voltage controllability.

VIII. DISCUSSION

We perform a comparative performance analysis of the proposed design with other emerging nano-oscillators used for non-Boolean application (Table I). CMOS ring oscillator circuits prove as representative systems for exploration of oscillators in the context of non-Boolean computing [29]. Although some of the emerging oscillators show high scalability, they suffer from the requirement of high bias current (mA) [6], low frequency (f) at low sense voltage [8], [9], and provide other challenges with regard to material endurance, thermal stability, and nonlinearity in the electrical behavior [5], [7], [8]. The proposed technique achieves competitive frequencies of oscillation (compared with other emerging technologies) along with low voltage operation. By properly defining a design space involving transistor sizing and T_{FE}, simultaneous control over frequency and operating voltage can be achieved for the proposed oscillator. Our design targets low power compact design of oscillators with voltage tunability and reconfigurable dynamics for non-Boolean computing.

It may be noted that previously negative differential resistance (NDR) which is similar to NOC has been utilized in designs other than oscillators (for instance, SRAMs [30]). In NDR-based SRAMs, there has been discussion on noise and stability challenges. However, such issues and design needs of SRAMs are different from the requirements in oscillator design. The issue of noise affecting storage node and voltage retention in NDR-based SRAMs is not directly applicable for oscillators since in the latter, the ease of switching between states is desirable for oscillations (unlike SRAMs where the state must be stable during read). It may be mentioned, however, that other sources of noise and variations in both NCFET (with NOC) and hysteretic FEFET oscillator need to be properly analyzed (as with oscillator implementations based on other technologies as well). Such noise and variations can affect frequency fluctuation, increasing phase noise. The proposed oscillator is robust to noise since its peak power is < -20 dB at its operating frequency. For FE-based oscillators (such as our design and that in [16]), one technological challenge will be the control of grain/domain variability in the FE, which needs to be addressed not just for oscillator designs but other applications of NCFET/FEFETs as well.

IX. CONCLUSION

In this paper, we proposed a dynamically reconfigurable NCFET/FEFET oscillator. The proposed NCFET oscillator design is based on NOC of NCFETs, while the FEFET oscillator utilizes hysteretic transfer characteristics of FEFETs. Both these features lead to hysteretic inverter characteristics.

Exploiting such Schmitt trigger action in the inverter and with the aid of output–input feedback, sustained oscillations are achieved in the proposed design. We demonstrate reconfigurability and distinct relaxation and sinusoid-like oscillations by employing PT and TG feedback in the NCFET oscillator. Voltage controllability of f is achieved through the gate bias of the feedback transistor. We also show how the proposed oscillators can be coupled to achieve frequency synchronization, which can lead to new applications of FE-based transistors in non-Boolean computing.

REFERENCES

[1] D. S. Modha, R. Ananthanarayanan, S. K. Esser, A. Ndirango, A. J. Sherbondy, and R. Singh, "Cognitive computing," *Commun. ACM*, vol. 54, no. 8, pp. 62–71, Aug. 2011. doi: 10.1145/1978542.1978559.

[2] T. Shibata, R. Zhang, S. P. Levitan, D. E. Nikonov, and G. I. Bourianoff, "CMOS supporting circuitries for nano-oscillator-based associative memories," in *Proc. 13th Int. Workshop Cellular Nanosc. Netw. Appl. (CNNA)*, Aug. 2012, pp. 1–5. doi: 10.1109/CNNA.2012.6331473.

[3] F. C. Hoppensteadt and E. M. Izhikevich, "Pattern recognition via synchronization in phase-locked loop neural networks," *IEEE Trans. Neural Netw.*, vol. 11, no. 3, pp. 734–738, May 2000. doi: 10.1109/72.846744.

[4] C. W. Wu, "Graph coloring via synchronization of coupled oscillators," *IEEE Trans. Circuits Syst. I. Fundam. Theory Appl.*, vol. 45, no. 9, pp. 974–978, Sep. 1998. doi: 10.1109/81.721263.

[5] S. Kaka, M. R. Pufall, W. H. Rippard, T. J. Silva, S. E. Russek, and J. A. Katine, "Mutual phase-locking of microwave spin torque nano-oscillators," *Nature*, vol. 437, pp. 389–392, Sep. 2005. doi: 10.1038/nature04035.

[6] G. Csaba *et al.*, "Spin torque oscillator models for applications in associative memories," in *Proc. 13th Int. Workshop Cellular Nanosc. Netw. Appl.*, Turin, Italy, Aug. 2012, pp. 1–2, doi: 10.1109/CNNA.2012.6331474.

[7] N. Shukla, W.-Y. Tsai, M. Jerry, M. Barth, V. Narayanan, and S. Datta, "Ultra low power coupled oscillator arrays for computer vision applications," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, Jun. 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573439.

[8] A. A. Sharma, J. A. Bain and J. A. Weldon, "Phase coupling and control of oxide-based oscillators for neuromorphic computing," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, pp. 58–66, Dec. 2015. doi: 10.1109/JXCDC.2015.2448417.

[9] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, Dec. 2008. doi: 10.1021/nl071804g.

[10] A. I. Khan *et al.*, "Negative capacitance in a ferroelectric capacitor," *Nature Mater*, vol. 14, no. 2, pp. 182–186, Dec. 2015.

[11] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014. doi: 10.1038/nmat4148.

[12] S. Gupta, M. Steiner, A. Aziz, V. Narayanan, S. Datta, and S. K. Dupta, "Device-circuit analysis of ferroelectric FETs for low-power logic," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3092–3100, Aug. 2017. doi: 10.1109/TED.2017.2717929.

[13] T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance evaluation of 7-nm node negative capacitance FinFET-based SRAM," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1161–1164, Aug. 2017. doi: 10.1109/LED.2017.2712365.

[14] S. L. Miller and P. J. McWhorter, "Physics of the ferroelectric nonvolatile memory field effect transistor," *J. Appl. Phys.*, vol. 72, no. 12, pp. 5999–6010, Sep. 1992. doi: 10.1063/1.351910.

[15] D. Wang, S. George, A. Aziz, S. Datta, V. Narayanan, and S. K. Gupta, "Ferroelectric transistor based non-volatile flip-flop," in *Proc. Int. Symp. Low Power Electron. Design*, Aug. 2016, pp. 10–15. doi: 10.1145/2934583.2934603.

[16] Z. Wang, S. Khandelwal, and A. I. Khan, "Ferroelectric oscillators and their coupled networks," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1614–1617, Nov. 2017. doi: 10.1109/LED.2017.2754138.

[17] T. K. Song, "Landau-Khalatnikov simulations for ferroelectric switching in ferroelectric random access memory application," *J. Korean Phys. Soc.*, vol. 46, no. 1, pp. 5–9, Jan. 2005.

[18] A. Aziz, S. Ghosh, S. Dutta, and S. K. Gupta, "Physics-based circuit-compatible SPICE model for ferroelectric transistors," *IEEE Electron Device Lett.*, vol. 37, no. 6, pp. 805–808, Jun. 2016. doi: 10.1109/LED.2016.2558149.

[19] K. Chatterjee, A. J. Rosner, and S. Salahuddin, "Intrinsic speed limit of negative capacitance transistors," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1328–1330, Sep. 2017. doi: 10.1109/LED.2017.2731343.

[20] (2016). *Arizona State University Predictive Technology Models*. [Online]. Available: http://ptm.asu.edu/

[21] M. Kobayashi, N. Ueyama, K. Jang, and T. Hiramoto, "Experimental study on polarization-limited operation speed of negative capacitance FET with ferroelectric HfO_2," in *IEDM Tech. Dig.*, Dec. 2016, pp. 12.3.1–12.3.4. doi: 10.1109/IEDM.2016.7838402.

[22] J. Seo, J. Lee, and M. Shin, "Analysis of drain-induced barrier rising in short-channel negative-capacitance FETs and its applications," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1793–1798, Apr. 2017. doi: 10.1109/TED.2017.2658673.

[23] G. Pahwa *et al.*, "Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance—Part II: Model validation," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4986–4992. Dec. 2016. doi: 10.1109/TED.2016.2614436.

[24] S. Dasgupta *et al.*, "Sub-kT/q switching in strong inversion in $PbZr_{0.52}Ti_{0.48}O_3$ gated negative capacitance FETs," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, pp. 43–48, Dec. 2015. doi: 10.1109/JXCDC.2015.2448414.

[25] A. I. Khan *et al.*, "Negative capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 111–114, Jan. 2016. doi: 10.1109/LED.2017.2754138.

[26] A. K. Saha, P. Sharma, I. Dabo, S. Datta, and S. K. Gupta, "Ferroelectric transistor model based on self-consistent solution of 2D Poisson's, non-equilibrium Green's function and multi-domain Landau Khalatnikov equations," in *IEDM Tech. Dig.*, Dec. 2017, pp. 13.5.1–13.5.4. doi: 10.1109/IEDM.2017.8268385.

[27] J. M. Rabaey. *Digital Integrated Circuits: A Design Perspective*. Upper Saddle River, NJ, USA: Prentice-Hall, 1996.

[28] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar. 1996. doi: 10.1109/4.494195.

[29] Y. Fang, C. N. Gnegy, T. Shibata, D. Dash, D. M. Chiarulli and S. P. Levitan, "Non-Boolean associative processing: Circuits, system architecture, and algorithms," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, pp. 94–102, Dec. 2015. doi: 10.1109/JXCDC.2015.2507863.

[30] J. P. A. van der Wagt, "Tunneling-based SRAM," *Proc. IEEE*, vol. 87, no. 4, pp. 571–595, Apr. 1999. doi: 10.1109/5.752516.