Modeling and Comparative Analysis of Hysteretic Ferroelectric and Anti-ferroelectric FETs

Atanu K. Saha[1] and Sumeet K. Gupta[1, 2]

[1]*Purdue Univ., W. Lafayette, IN,* [2]*Penn State Univ.,Univ. Park, PA,USA, Email:saha26@purdue.edu / Ph: 8148628544*

Introduction: In this paper, we analyze ferroelectric (FE) and anti-ferroelectric (AFE) field effect transistors (FETs) (shown in Fig. 1(a)) and compare their subthreshold characteristics and hysteretic behavior. To facilitate this analysis, we develop a Preisach based [1] circuit compatible model for FE/AFE. Whereas in FE capacitor the two stable polarization (P) states are $-P_R$ and $+P_R$, in case of AFE capacitor, non-volatility can be achieved within $0 \leftrightarrow +P_R$ by imposing a built-in potential through work-function engineering (Fig, 1(b)). However, in FE/AFEFETs, FE/AFE can be partially polarized (forming minor P-V loop), which we analyze in this paper. Finally, correlating the negative capacitance (NC) effect in FE/AFE with domain-wall propagation [2], we explore the steep subthreshold swing (SS) characteristics of FE/AFE-FET and analyze their transient nature and dependence on flat-band voltage (V_{FB}) and maximum applied gate voltage (V_{GS}).

Modeling: To perform FE/AFE-FET simulations, we have developed a model for FE/AFE based on Miller's analytical equations (Fig. 3) [1]. We calibrated (Fig. 2(a-b)) the model parameters with experimental results [3] obtained for HZO (FE:$Hf_{0.5}Zr_{0.5}O_2$ & AFE:$Hf_{0.3}Zr_{0.7}O_2$). Considering the lag between P and applied voltage (V_{FE}) through τ parameter (which can be attributed as the delay associated with domain wall propagation in FE/AFE), the model can capture the NC effect in FE/AFE [2]. Furthermore, the model can capture major/minor loop formation of FE/AFE (Fig. 2(c-d)) depending on the peak applied voltage through dynamic capacitance calculation (Fig. 3). In this paper, we have used 45nm high-k planar FET as the baseline transistor and FE/AFE with a thickness ($T_{FE/AFE}$)=3nm.

Analysis and Discussion: The I_{DS}-V_{GS} characteristics of FEFET (Fig. 4(a)) shows non-volatile hysteretic behavior with ~0.6V hysteresis. At the same time, SS in the reverse (R) sweep direction of V_{GS} shows steeper than 60mv/decade at 300K (Fig. 4(b)), whereas in the forward (F) sweep, SS is similar to the baseline FET (min SS=70.16 mV/decade). Fig.4 (c) shows the internal voltage amplification (dV_{INT}/dV_{GS}, where V_{INT} is the voltage at the interface of FE/AFE and the gate of the underlying FET). This amplification, which is due to NC effect, is higher in R-sweep compared to F-sweep in FEFETs. Similar to FEFET, I_{DS}-V_{GS} characteristics of AFEFET (Fig. 5(a)) shows non-volatile hysteretic behavior, but now, steeper SS and higher dV_{INT}/dV_{GS} occurs in F-sweep direction compared to R-sweep (Fig. 5(b-c)). To understand the asymmetry in dV_{INT}/dV_{GS} and SS of FE/AFE-FET, let us first discuss the physical origin of NC effect. According to our FE/AFE model, NC effect is the outcome of two-step process: (i) overshoot of FE/AFE voltage ($V_{FE/AFE} = E_{FE/AFE} \times T_{FE/AFE,}$ solid line in Fig. 6(a)) beyond the steady-state P-$V_{CFE/AFE}$ (where $V_{CFE/AFE} = E_{CFE/AFE} \times T_{FE/AFE}$, dashed line in Fig. 6(a)) and (ii) snap-back towards the steady state P-$V_{CFE/AFE}$. These two phenomena are directly related with the delay parameter τ and large change in FE/AFE capacitance ($C_{FE/AFE}$) i.e. large $dC_{FE/AFE}/d|V_{CFE/\mathrm{AFE}}|$ near the coercive voltage. According to [2], $V_{FE/AFE}$ overshoot increases with the increase in ramp rate of the applied V_{GS} (dV_{GS}/dt) and increase in τ, whereas the snap-back increases as $dC_{FE/AFE}/d|V_{CFE/\mathrm{AFE}}|$ increases. That means for a constant τ, NC effect can be increased by (i) increase in $dC_{FE/AFE}/d|V_{CFE/AFE}|$ or (ii) increase in dV_{GS}/dt. Now, in general, $dC_{FE/AFE}/d|V_{CFE/AFE}|$ is comparatively lower in minor P-$V_{CFE/AFE}$ path than major path. Therefore, in FEFET, as FE traverses a path closer to the major loop in R-sweep than F-sweep (Fig. 6(a)), NC effect and hence, dV_{INT}/dV_{GS} is higher in R-sweep. Similarly, in AFEFET, AFE traverses major path in F-sweep and minor path in R-sweep resulting higher dV_{INT}/dV_{GS} in F-sweep. However, NC effect or $dV_{INT}/dV_{GS} > 1$ may not guarantee the observation of SS<60mV/decade, rather it depends on the region of operation of the FET or the range of P where NC occurs. In a FET, minimum (min.) SS occurs in sub-threshold or weak-inversion region, whereas SS is quite high in near accumulation and strong inversion region. For FEFET (Fig. 6(a)), we observe that NC effect occurs in moderate positive (+ve) P region (R-sweep) and low negative (-ve) P region (F-sweep) of the FE. This, respectively, corresponds to the weak-inversion and near-accumulation region of the FEFET. Therefore steeper SS is visible only in R-sweep, even though $dV_{INT}/dV_{GS} > 1$ occurs in both R and F-sweeps (Fig. 4(c)). In contrast, for AFEFET, NC effect occurs in moderate +ve P region (F-sweep) and high +ve P region (R-sweep) of the AFE. This respectively corresponds to the strong-inversion and weak-inversion region of the AFEFET. Hence steeper SS is visible only in F-sweep direction. In addition, as NC effect is a transient phenomenon, SS also depends on the rise/fall time (T) of the applied V_{GS}. For very fast ramp input ($T \approx \tau$), FE/AFE polarization does not switch completely, and therefore, NC effect vanishes. On the other hand, for very slow ramp input ($T >> \tau$), voltage overshoot becomes negligible and so does the NC effect. Min. SS of FE/AFE-FET for different T have been plotted in Fig. 6(b). SS<60mV/decade is observed only for certain value of *T (4ns ~ 0.1us),* which is in agreement with our discussion that NC effect occurs within a range of T ($\tau < T < 100\tau$).

Now, we will analyze the impact of flat-band voltage (V_{FB}) and maximum (max.) applied V_{GS} on SS characteristics of FE/AFEFET. By tuning V_{FB}, it is possible to change the polarization range of NC effect and by changing V_{GS} swing, it is possible to control major/minor loop traversal of FE/AFE. First, to analyze the impact of V_{FB}, P-$V_{FE/AFE}$ loop of FE/AFE-FET for different V_{FB} have been plotted in Fig. 7(a-b) showing that the range of P where NC occurs, shifts towards +ve P with the decrease in V_{FB}. Therefore, in FEFET, the min. SS for F-sweep decreases while for R-sweep, it increases with a decrease in V_{FB}. Min SS for F- and R- sweeps become equal at $V_{FB} \approx$-0.4V. However, for AFEFET, min. SS in both sweep directions decrease with a decrease in V_{FB} and cross each other at $V_{FB} \approx$-0.3V. Now, we will analyze the impact of V_{GS}. From Fig. 8(a-b), we can observe that with an increase in V_{GS} swing, P-$V_{FE/AFE}$ becomes closer to the major loop and therefore $dC_{FE/AFE}/dV_{CFE/AFE}$ increases. Therefore, NC effect increases both in FE/AFE-FET with the increase in V_{GS} and hence, min SS also decreases with the increase in applied V_{GS} swing (Fig. 8(c)).

Conclusion: We discussed the SS characteristics of FE/AFE-FETs and analyzed their dependence on flat-band and applied gate voltage swing. Our analysis concludes that with V_{FB} reduction, symmetric SS characteristics can be achieved in FE/AFE-FETs.

Acknowledgement: This work was supported in part by DARPA YFA, SRC-GRC and NSF.

References: [1] S. L. Miller *et al.*, *J. Appl. Phys.,* vol. 70, p. 02849, (1991) [3] J. Muller *et al., Nano Lett.*, vol. 12, p. 4318, (2012).
[2] A. K. Saha *et al.*, *J. Appl. Phys.*, vol. 123, p. 105102, (2018),

978-1-5386-3028-0/18/$31.00 ©2018 IEEE

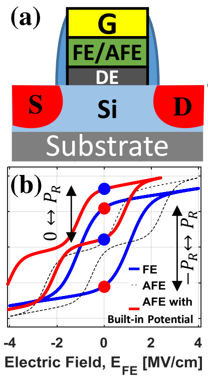

Fig.1:(a) FE/AFE-FET. (b) Stable P-state of FE/AFE.

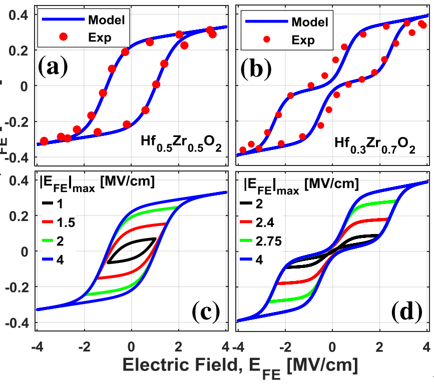

Fig. 2: (a) FE and (b) AFE P-E loop (model calibration). (c) FE and (d) AFE major/minor loop formation.

FE: Major Loop $P_S = 0.25C/m^2, P_R = .19C/m^2, E_C = 1.1MV/cm$

$$P_M^{\pm} = Ps\left[\tanh\left(\frac{E_{C_{FE}} \mp E_C}{2\delta}\right)\right] + C_0 E_{C_{FE}}; \quad \delta = \alpha \times \left[ln\left[\frac{P_S + P_R}{P_S + P_R}\right]\right]^{-1}$$

AFE: Major Loop $P_S = 0.29C/m^2, P_R = .22C/m^2, E_c^{1,2} = 2.5, 0.5MV/cm$

$$P_M^{\pm} = \frac{Ps}{2}\left[\tanh\left(\frac{E_{C_{AFE}} - E_c^{2,1}}{2\delta}\right) - \tanh\left(\frac{-E_{C_{AFE}} - E_c^{1,2}}{2\delta}\right)\right] + C_0 E_{C_{AFE}}$$

FE/AFE Minor Loop: $\alpha = 0.5, \beta = 2, \eta = 2, C_0 = .01F/m^2, \tau = 1ns$

$$\frac{dP_m}{dE_{C_{FE/AFE}}} = \frac{\Gamma \times dP_M}{dE_{C_{FE/AFE}}}; \quad \Sigma = \left[\sqrt{\frac{P_m - P_M}{\pm\eta P_S - P_m}}\right]; \quad \Gamma = 1 - \tanh[\beta \times \Sigma]$$

Transient characteristics:

$$\frac{dE_{C_{FE/AFE}}}{dt} = \frac{1}{\tau}\left[E_{FE/AFE} - E_{C_{FE/AFE}}\right]$$

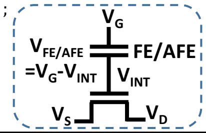

Fig. 3: FE/AFE Model Equations for major/minor P-E loop formation. Calibrated FE and AFE parameters are shown. The schematic model of FE/AFE-FET is shown in inset.

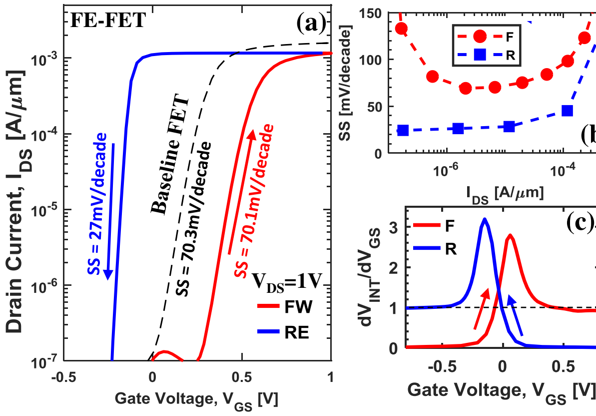

Fig. 4: (a) I_{DS}-V_{GS} (b) subthreshold swing (SS) and (c) internal voltage amplification characteristics for FE-FET showing stepper SS in forward (F) sweep. [T_{FE}=3nm].

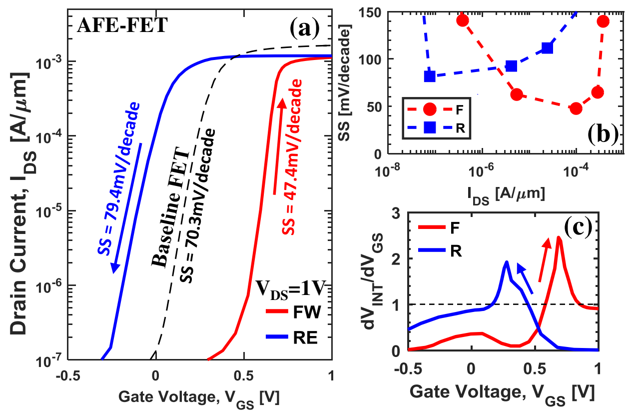

Fig. 5: (a) I_{DS}-V_{GS} (b) subthreshold swing (SS) and (c) internal voltage amplification characteristics for AFE-FET showing stepper SS in reverse (R) sweep. [T_{AFE}=3nm].

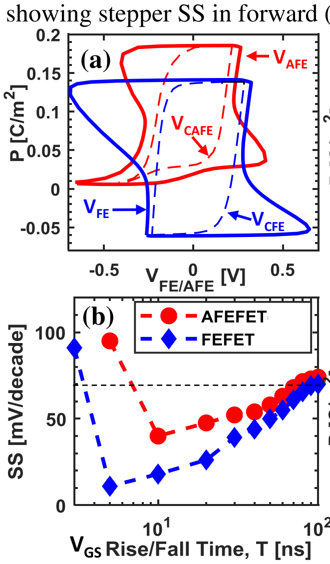

Fig. 6: (a) P-$V_{FE/AFE}$ loop of FE/AFE in FE/AFE-FET showing NC effect (b) min. SS for different rise/fall time of V_{GS} showing non-monotonic dependence on T.

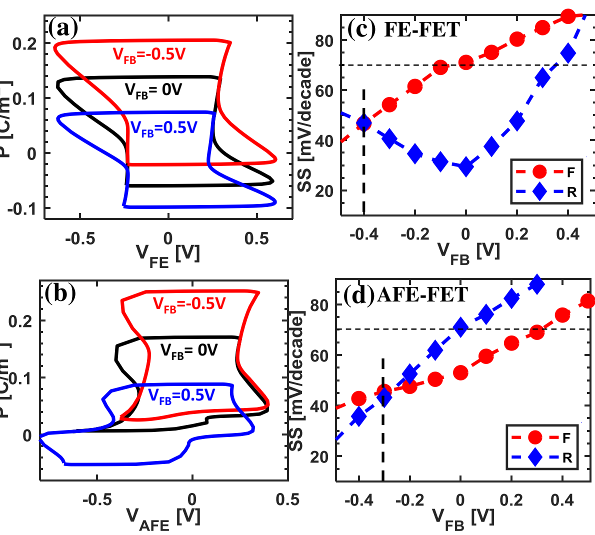

Fig. 7: (a-b) P-$V_{FE/AFE}$ loop of FE/AFE in FE/AFE-FET for different flat band voltage (V_{FB}) showing the P-$V_{FE/AFE}$ loop moves towards +ve P with the decrease in V_{FB}. (c-d) Minimum SS of FE/AFE-FET for different V_{FB} showing that symmetric SS can be achieved @V_{FB}= - 0.4V and - 0.3V respectively.

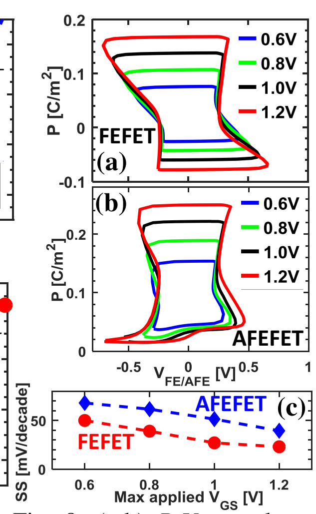

Fig. 8: (a-b) P-$V_{FE/AFE}$ loop and (b) min. SS of FE/AFE-FET for different applied V_{GS} showing increase in NC effect and hence decrease in SS with the increase in V_{GS}. [dV_{GS}/dt =constant, V_{FB}=0V].