A Hybrid Cockcroft-Walton / Dickson Multiplier for High Voltage Generation

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***Abstract*—This paper presents a voltage multiplier topology that is a hybrid between a Cockcroft-Walton multiplier and a Dickson charge pump. The Cockcroft-Walton structure exhibits significant output voltage drop under load as the number of multiplier stage increases. This is because all coupling capacitors are connected in series. Dickson charge pump mitigates this issue by connecting all capacitors in parallel. But this solution comes at the expense of large capacitor voltage stress at the last multiplier stage. The proposed hybrid structure arranges some capacitors in parallel and others in series, thereby achieving low output voltage drop and low capacitor voltage stress at the same time. We develop a model that predicts hybrid multiplier's performance and validate it experimentally. We also demonstrate a 60 V-to-2.25 kV dc-dc converter based on a 16-stage hybrid voltage multiplier which achieves a voltage gain of 12.8 while keeping the highest capacitor voltage stress to 660 V.**

I. Introduction

High-voltage power supplies are crucial in many medical and industrial applications. Applications include X-ray imaging [1], neutron radiography [2], particle acceleration [3], and electrostatic air filtering [4]. This paper presents a new voltage multiplier topology that is suitable for high-voltage dc generation.

Cockcroft-Walton multiplier [5] (also known as Greinacher multiplier [6] and Villard cascade) is a switched-capacitor circuit that generates a high-voltage dc from a low-voltage ac. This circuit comprises many units of half-wave voltage doublers stacked in series. Those cascaded voltage doublers form a long string of diodes which is tapped from intermediate nodes via coupling capacitors. Besides Marx generator, Cockcroft-Walton is arguably the most popular solid-state high-voltage generator topology [7]–[10].

The ideal case is when the coupling capacitance is large enough so that negligible voltage drop occurs on the capacitor. In that case, the output voltage is simply the peak-to-peak amplitude of the input ac voltage multiplied by the number of cascaded voltage doublers, or simply the number of *stages*. Since all capacitors and diodes are under the same voltage stress, it is easy to make full use of every device's voltage limits. Unfortunately, the output voltage of a Cockcroft-Walton multiplier quickly 'sags', i.e., deviates from the ideal value, as the number of stage increases [11]. This is because the output impedance adds up rapidly as more coupling capacitors are connected in series.

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The rapid increase of the Cockcroft-Walton multiplier's output impedance was one of the main motivations for the development of Dickson charge pump [12]. (Some like to reserve the name 'Greinacher' for this topology [13] since the circuit appears alongside the Cockcroft-Walton structure in Greinacher's paper [6].) Dickson is widely used both in integrated circuits to generate a voltage that is several times higher than the supply voltage [12], [14], and in discrete power converters [15], [16]. Coupling capacitors are connected to the diode chain in parallel instead of series. Therefore, only one capacitor exists between the input port and each intermediate node of the diode chain, regardless of the number of stages. The main shortcoming of Dickson topology is, however, that the coupling capacitor at the last stage (closest to the output port; farthest from the input port) needs to withstand voltage stress that is equivalent to the charge pump output voltage.

Oftentimes, high-voltage capacitors are more readily available than high-voltage diodes. In such cases, it is better to choose Dickson topology over Cockcroft-Walton topology. If the output voltage needs to be higher than the coupling capacitors' voltage rating, one may consider stacking multiplier stages in Dickson structure until the output voltage reaches the capacitor voltage limit, then switch to Cockcroft-Walton structure and continue stacking additional stages. This idea is the inspiration of our study.

The paper proceeds as follows. Section II analyzes a well-known two-stage Cockcroft-Walton multiplier example in order to help readers understand discussions throughout the paper. Readers who are familiar with the operation of a voltage multiplier may skip this section without loss of continuity. Section III presents a topology that is a hybrid of a Cockcroft-Walton multiplier and a Dickson charge pump. The achievable output voltage is higher compared to Dickson topology for a given capacitor voltage limit. At the same time, the output impedance is lower than that of Cockcroft-Walton topology. Section IV analyzes the proposed voltage multiplier and develop a general model. We also design a hybrid voltage multiplier as an example. Section V experimentally validates the analysis and the design example of the previous section. Section VI concludes the paper.

II. Review of a Cockcroft-Walton Multiplier

In this section, we review the operation of a two-stage Cockcroft-Walton multiplier. The purpose is to familiarize readers with definitions of terms used throughout the paper. In this and the following sections we assume ideal diodes; i.e., zero reverse current, zero forward voltage drop, and zero capacitance between two terminals.

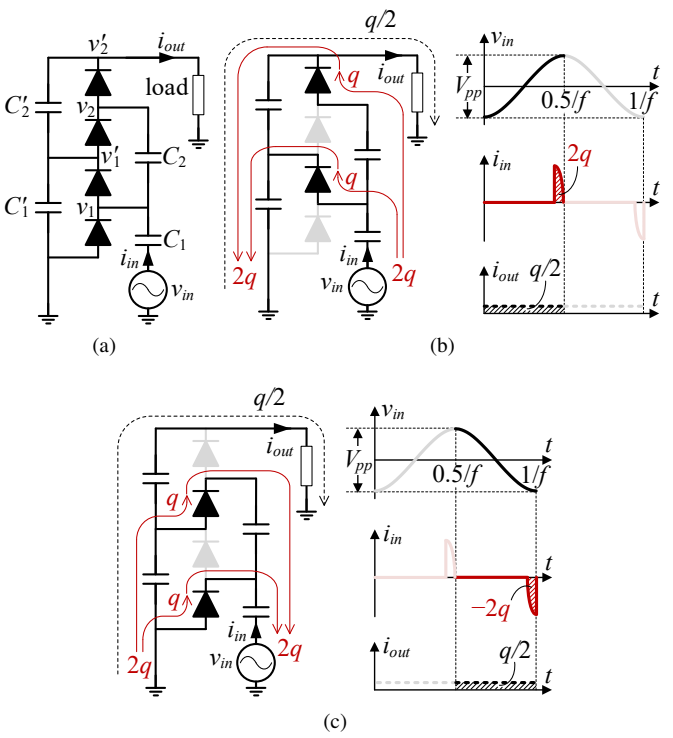


Fig. 1. Two-stage Cockcroft-Walton voltage multiplier and its operation. (a) Schematic. (b) Charge flow during the *push* phase. (c) Charge flow during the *pull* phase.

Fig. 1 describes the voltage multiplier (Fig. 1a) and its operation during the *push* phase (Fig. 1b) and the *pull* phase (Fig. 1c). Here we assume large enough C_1' and C_2' to maintain relatively constant output voltage across the load, so that the output current i_{out} remains continuous with only a small ripple. The amount of charge delivered to the load during one switching cycle $1/f$ is denoted by q and is found as $\langle i_{out}\rangle/f$ where $\langle i_{out}\rangle$ is the average value of i_{out}.

The *push* phase (Fig. 1b) is the interval between $t = 0$ and $t = 0.5/f$, when the ac voltage source v_{in} ramps up from $-V_{pp}/2$ to $V_{pp}/2$. Similar to the well-known case of a half-wave rectifier, a current spike occurs in i_{in} at the end of the *push* phase to recharge capacitors C_1, C_1', C_2, and C_2'. This sharp injection of charge is marked with red arrows, and the amount of charge flowing through each branch is marked next to the arrow. Meanwhile, i_{out} remains relatively constant, delivering the charge of $q/2$ to the load. This charge flow is marked with a black dotted arrow. A similar analysis applies to the *pull* phase (Fig. 1c), the interval when v_{in} ramps down from $V_{pp}/2$ to $-V_{pp}/2$, with the charge flow directions reversed.

Fig. 2 shows voltage waveforms of intermediate nodes v_1, v_1', v_2, and v_2'. Black solid lines indicate v_1, and v_2. Orange dotted lines indicate v_1' and v_2'. On the left-hand side of the figure is the ideal case waveforms when capacitors are so large that the voltage drop across them is negligible. In this case, the peak-to-peak swing of v_1 and v_2 is the same as the input peak-to-peak swing V_{pp}, and the level of v_1' and v_2' remains unchanged throughout the switching cycle.

On the right-hand side of Fig. 2 is the realistic case where

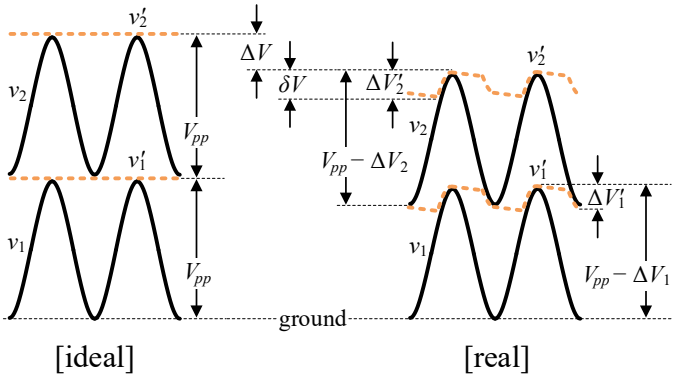


Fig. 2. Ideal versus real waveforms of v_1, v_2 (black solid lines) and v_1', v_2' (orange dotted lines) during the voltage multiplier operation. One can find the definition of $\Delta V_1, \Delta V_1', \Delta V_2, \Delta V_2', \Delta V$, and δV from this figure.

the voltage drop across capacitors is non-negligible. Due to those voltage drops, peak-to-peak swings of v_1 and v_2 are reduced by ΔV_1 and ΔV_2, respectively. Also, peak-to-peak ripples of $\Delta V_1'$ and $\Delta V_2'$ occur in v_1' and v_2', respectively. From the charge flow map of Fig. 1, one can find that $\Delta V_1 = 2q/C_1$, $\Delta V_1' = 2q/C_1'$, $\Delta V_2 = 2q/C_1 + q/C_2$, and $\Delta V_2' = 2q/C_1' + q/C_2'$.

Let us define the output voltage drop ΔV as the difference between the ideal output $2V_{pp}$ and the peak output in the realistic case $v_{2,max}'$ as indicated in Fig. 2. (We use the same definitions of ΔV and δV throughout the rest of the paper.) Then, $v_{2,max}'$ is equal to $2V_{pp} - \Delta V$ where ΔV is equal to $\Delta V_1 + \Delta V_1' + \Delta V_2$. Also, the peak-to-peak ripple of the output voltage, δV, is the same as $\Delta V_2'$ by definition.

III. Four-Stage Hybrid Voltage Multiplier

A. Operating Principle

Fig. 3 shows voltage multipliers in three different topologies, namely Cockcroft-Walton (Fig. 3a), Dickson (Fig. 3b), and the proposed hybrid (Fig. 3c). All three circuits are four stage multipliers where the first stage consists of C_1, C_1', and two diodes at the bottom, the second stage consists of C_2, C_2', and the next two diodes, and so on. Those three voltage multipliers are functionally identical provided that capacitors are sufficiently large to serve the purpose of a dc-blocking ac-coupling capacitor. Ideally, capacitors $C_1, \ldots, C_4$ isolate nodes $v_1, \ldots, v_4$ at dc and short them at ac, specifically at the switching frequency of diodes. The same argument applies to capacitors $C_1', \ldots, C_4'$ and $v_1', \ldots, v_4'$. (A general discussion on this type of capacitor-diode voltage multipliers can be found in [17].)

When capacitors are sufficiently large, voltages $v_1, \ldots, v_4$ swing by the peak-to-peak amplitude equal to that of the input voltage v_{in}. Similarly, if $C_1', \ldots, C_4'$ are large enough, voltages $v_1', \ldots, v_4'$ remain steady with no ripple. Due to such behaviors, the column of capacitors $C_1, \ldots, C_4$ is known as an *oscillating column* (also known as *coupling column*), and the column of $C_1', \ldots, C_4'$ is called a *smoothing column* [18]–[21].

Provided that the dc output current i_{out} and the switching frequency f are the same in three multipliers, the amount of

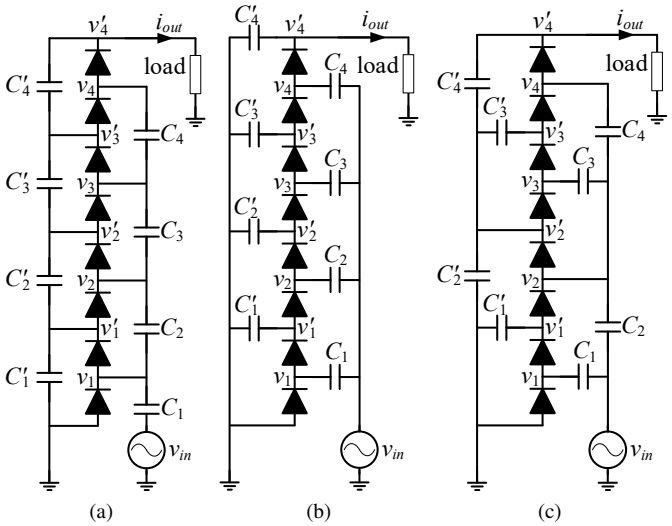


Fig. 3. Four-stage voltage multipliers in three different topologies. (a) Cockcroft-Walton. (b) Dickson. (c) The proposed hybrid.

charge flowing through each wire for every switching cycle is also the same. Fig. 4 illustrates how much charge flows in each branch during the *push* phase (Fig. 4a) and the *pull* phase (Fig. 4b). Here we define charge q as the charge delivered to the load for one switching cycle, i.e.,

$$q = \langle i_{out} \rangle / f \tag{1}$$

where $\langle i_{out} \rangle$ is the average value of i_{out}. Dotted wires indicate dc-open ac-short connections realized by coupling capacitors. Assuming approximately equal output voltage at each multiplier stage, during the *push* and *pull* phases the input voltage source v_{in} either sources or sinks the charge $4q$, respectively. The corresponding current spikes are marked with red arrows. The output dc current i_{out}, marked with a black dotted arrow, is provided by the capacitor network of the smoothing column.

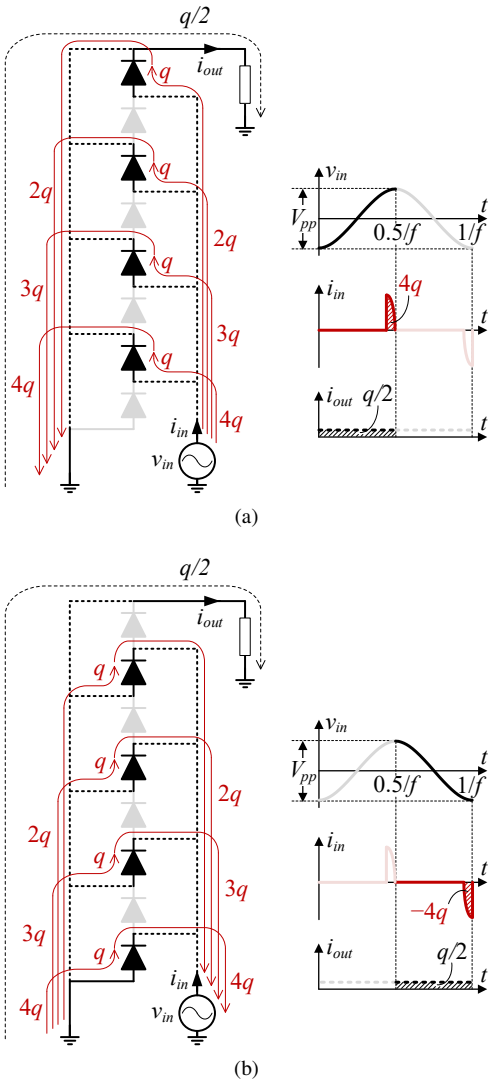


Fig. 4. Charge flow map of three circuits in Fig. 3. (a) Charge flow during the *push* phase. (b) Charge flow during the *pull* phase.

B. Voltage Drop and Ripple at the Output

Capacitors $C_1, \ldots, C_4$ and $C'_1, \ldots, C'_4$ in Fig. 3 are not infinitely large in reality. Charge flowing as indicated in Fig. 4 causes voltage drop across capacitors. Those voltage drops are depicted in Fig. 5. Black solid lines indicate v_1, v_2, and v_3 waveforms whereas orange dotted lines are for v'_1 and v'_2 waveforms (from bottom to top). When the input voltage peak-to-peak swing is V_{pp}, the peak-to-peak swing of v_1 is a bit smaller than V_{pp} due to the capacitor voltage drop. Let us define ΔV_1 as the difference between V_{pp} and the peak-to-peak amplitude of v_1. $\Delta V_2, \ldots, \Delta V_4$ are defined in an identical manner. Also, let us define $\Delta V'_1, \ldots, \Delta V'_4$ as the peak-to-peak ripple of $v'_1, \ldots, v'_4$.

Fig. 5 indicates that the peak value of the output voltage v'_4, denoted by $v'_{4,max}$, can be expressed as

$$v'_{4,max} = 4V_{pp} - \Delta V \tag{2}$$

where

$$\begin{aligned} \Delta V &= \Delta V_1 + \Delta V'_1 + \Delta V_2 + \Delta V'_2 + \Delta V_3 + \Delta V'_3 + \Delta V_4 \\ &= \sum_{k=1}^{4} (\Delta V_k + \Delta V'_k) - \Delta V'_4. \end{aligned} \tag{3}$$

The output peak-to-peak ripple which we denote by δV is, by definition,

$$\delta V = \Delta V'_4. \tag{4}$$

The average output voltage V_{out} is

$$V_{out} = v'_{4,avg} \approx 4V_{pp} - \Delta V - \frac{1}{2}\delta V. \tag{5}$$

Table I lists voltage drops at each node in four-stage multipliers of Fig. 3. Among those three topologies, Cockcroft-Walton has the highest voltage drop in every node. This is because all capacitors are located on vertical branches. Vertical branches carry larger amount of charge than horizontal branches, as illustrated in Fig. 4, resulting in a higher voltage

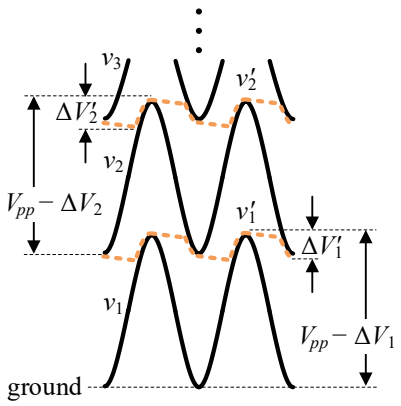


Fig. 5. Waveforms of $v_1, v_2, \ldots$ (black solid lines) and $v_1', v_2', \ldots$ (orange dotted lines) during the voltage multiplier operation.

drop. Also, influences of capacitors on vertical branches accumulate with the number of stages because vertical branches of lower stages constitute the ground return path for upper stages.

To make the comparison of Table I more meaningful, let us assume that all capacitor values are equal to C. Using Equations (3) and (4), we calculate ΔV and δV of three topologies. The results are shown in Table II. Also shown in the table is the highest voltage stress on capacitors $V_{C,max}$.

As shown for four-stage multipliers in Table II, the proposed hybrid topology in general exhibits $V_{C,max}$, ΔV, and δV that are in between those of Cockcroft-Walton and Dickson. If it is desired to reduce the output voltage drop and ripple at the expense of increased capacitor voltage stress, switching the topology from Cockcroft-Walton to hybrid may be considered. Similarly, if one wants to reduce the capacitor voltage stress of a Dickson multiplier, he may consider switching to a hybrid topology provided that the increased voltage drop and ripple at the output are acceptable.

C. Power Conversion Efficiency

The sagging phenomenon of the output voltage described in (5) is intrinsically related to power conversion efficiency. Power loss occurs even in our ideal analysis because we assume that it is a voltage source that abruptly charges and discharges capacitors. Fig. 4 indicates that for every switching cycle, the input ac source provides energy of $4qV_{pp}$ to the multiplier, which in turn provides the energy of qV_{out} to the load. Dividing the output energy by the input energy per cycle gives the efficiency

$$\eta = \frac{qV_{out}}{4qV_{pp}} = 1 - \frac{\Delta V + \delta V/2}{4V_{pp}}. \tag{6}$$

This equation, together with ΔV and δV values in Table II, indicates that the proposed hybrid topology has an efficiency that is lower than Dickson's, but higher than Cockcroft-Walton's.

Note that this argument is valid only when the multiplier circuit is driven by a voltage source (a low-impedance inverter). When driven by a current source (e.g., through a series inductor, like in the experiment of section V-B), no energy is lost when capacitors are charged and discharged. Thus, ideally, the multiplier can achieve the efficiency of 100 % even with a non-zero output voltage drop.

D. Energy Stored in Coupling Capacitors

In some cases, the size of coupling capacitors are determined by the energy they need to store, rather than by the type of discrete packages predetermined by capacitor manufacturers. For example, each on-chip capacitors in an integrated-circuit voltage multiplier can be sized differently. Also, high voltage generators of tens of kilovolts or higher often uses custom-designed capacitors. In such cases, the total amount of energy stored in coupling capacitors, denoted by E_{cap}, may be of interest because it has implication on the size of the circuit. Ignoring the voltage drop by capacitors and assuming every multiplier stage equally generates the voltage V_{pp}, we calculate E_{cap} for three topologies by summing all energies stored in eight individual capacitors:

$$\text{C-W: } \frac{1}{2}CV_{pp}^2 \times 8 = 4CV_{pp}^2 \tag{7}$$

$$\text{Dickson: } \frac{1}{2}CV_{pp}^2(1^2 + 2^2 + 3^2 + 4^2) \times 2 = 30CV_{pp}^2 \tag{8}$$

$$\text{Hybrid: } \frac{1}{2}CV_{pp}^2(1^2 + 2^2 + 1^2 + 2^2) \times 2 = 10CV_{pp}^2 \tag{9}$$

As is the case for ΔV and δV, E_{cap} of the hybrid topology also sits between Dickson's and Cockcroft-Walton's.

E. Influence of Diode Non-Ideality

This section discusses the influence of the diode's forward voltage drop $V_{D,on}$ and the diode's parasitic capacitance $C_{D,j}$ on the voltage multiplier's performance. When $V_{D,on}$ is non-zero, V_{out} is reduced by $8V_{D,on}$. This reduction occurs because the voltage added by each multiplier stage is reduced by $2V_{D,on}$. Analyses in [12], [22], [23] draw the same conclusion for Dickson topology.

The influence of non-zero $C_{D,j}$ depends largely on whether $C_{D,j}$ is much smaller than or comparable to C. When $C_{D,j}$ is much smaller than C, the output voltage is mostly unaffected, and merely the amount of charge that enters or exits the multiplier input during half a cycle is increased by $8C_{D,j}V_pp$. This increase in charge is because the voltage across every diode has to be either increased or decreased by V_{pp} before any diode turns on. Consequently, the inverter circuit that drives the multiplier needs to provide a larger ac current, which may negatively impacts the inverter size or efficiency.

When $C_{D,j}$ is comparable to C, not only the input current is increased as explained above, but also C now exhibits non-negligible voltage drop when the input current is charging and discharging $C_{D,j}$. The effective ac input voltage seen by the multiplier circuit is reduced, and as a result, V_{out} is decreased. How much V_{out} is decreased depends on the multiplier topology, i.e., the location of coupling capacitors that causes this voltage drop, but as can be readily inferred, Cockcroft-Walton will be most, and Dickson will be least affected.

TABLE I
VOLTAGE DROPS AT EACH NODE IN FOUR-STAGE MULTIPLIERS OF FIG. 3.

k	Cockcroft-Walton		Dickson		Hybrid	
	ΔV_k	$\Delta V_k'$	ΔV_k	$\Delta V_k'$	ΔV_k	$\Delta V_k'$
1	$\frac{4q}{C_1}$	$\frac{4q}{C_1'}$	$\frac{q}{C_1}$	$\frac{q}{C_1'}$	$\frac{q}{C_1}$	$\frac{q}{C_1'}$
2	$\frac{4q}{C_1}+\frac{3q}{C_2}$	$\frac{4q}{C_1'}+\frac{3q}{C_2'}$	$\frac{q}{C_2}$	$\frac{q}{C_2'}$	$\frac{3q}{C_2}$	$\frac{3q}{C_2'}$
3	$\frac{4q}{C_1}+\frac{3q}{C_2}+\frac{2q}{C_3}$	$\frac{4q}{C_1'}+\frac{3q}{C_2'}+\frac{2q}{C_3'}$	$\frac{q}{C_3}$	$\frac{q}{C_3'}$	$\frac{3q}{C_2}+\frac{q}{C_3}$	$\frac{3q}{C_2'}+\frac{q}{C_3'}$
4	$\frac{4q}{C_1}+\frac{3q}{C_2}+\frac{2q}{C_3}+\frac{q}{C_4}$	$\frac{4q}{C_1'}+\frac{3q}{C_2'}+\frac{2q}{C_3'}+\frac{q}{C_4'}$	$\frac{q}{C_4}$	$\frac{q}{C_4'}$	$\frac{3q}{C_2}+\frac{q}{C_4}$	$\frac{3q}{C_2'}+\frac{q}{C_4'}$

TABLE II
PERFORMANCE COMPARISON OF THREE MULTIPLIERS IN FIG. 3. HERE WE ASSUME THAT ALL CAPACITOR VALUES ARE EQUAL TO C.

	Cockcroft-Walton	Hybrid	Dickson
$V_{C,max}$	V_{pp}	$2V_{pp}$	$4V_{pp}$
ΔV	$50(q/C)$	$20(q/C)$	$7(q/C)$
δV	$10(q/C)$	$4(q/C)$	(q/C)

Detailed analysis regarding the effect of $C_{D,j}$ on the output voltage of a Cockcroft-Walton multiplier can be found in [24]–[27].

IV. GENERAL MODEL FOR THE HYBRID TOPOLOGY

A. Derivation

In order to generalize the hybrid topology, let us define parameters m and n that determines a $(m\times n)$ hybrid structure. Fig. 6 describes the structure. Parameter m is the number of capacitors that appear on vertical branches of either an oscillating column or a smoothing column. Parameter n is the number of stages in each *block* as described in Fig. 6 (or, equivalently, the number of total multiplier stages divided by m).

Fig. 7 illustrates charge flow at the k-th stage of an $(m\times n)$ hybrid multiplier. Note that this picture is an approximation since the charge flows in this manner only when voltages of each multiplier stage are identical. In reality, as the number of multiplier stages increases so does the voltage drop at each stage, which results in a lower amount of charge drawn by higher stages. A more thorough discussion that takes this effect into consideration can be found in [28].

The first $(n-1)$ voltage multiplier stages have a coupling capacitor on the horizontal branch, similar to Dickson topology. The n-th stage has its capacitor on the vertical branch, similar to Cockcroft-Walton topology. Then the whole n-stage structure repeats m times to constitute mn multiplier stages.

In fact, this definition of $(m\times n)$ hybrid topology includes Cockcroft-Walton and Dickson topologies. A $(m\times 1)$ topology corresponds to an m-stage Cockcroft-Walton topology, and a $(1\times n)$ topology corresponds to an n-stage Dickson topology. For example, three multipliers depicted in Fig. 3a, 3b, and 3c can be called a (4×1), (1×4), and (2×2) multiplier, respectively.

Now let us find the voltage drop in each intermediate node of an $(m\times n)$ hybrid multiplier. Voltage drops in intermediate nodes v_k and v_k' are denoted by ΔV_k and $\Delta V_k'$, respectively, where k is an integer from 1 to mn. Table III lists ΔV_k and $\Delta V_k'$ in terms of charge q and capacitance C. Here, for the sake of simplicity, we assume that all capacitor values are equal to C. The charge q is defined in the same manner as (1).

To obtain the output voltage drop ΔV and the peak-to-peak

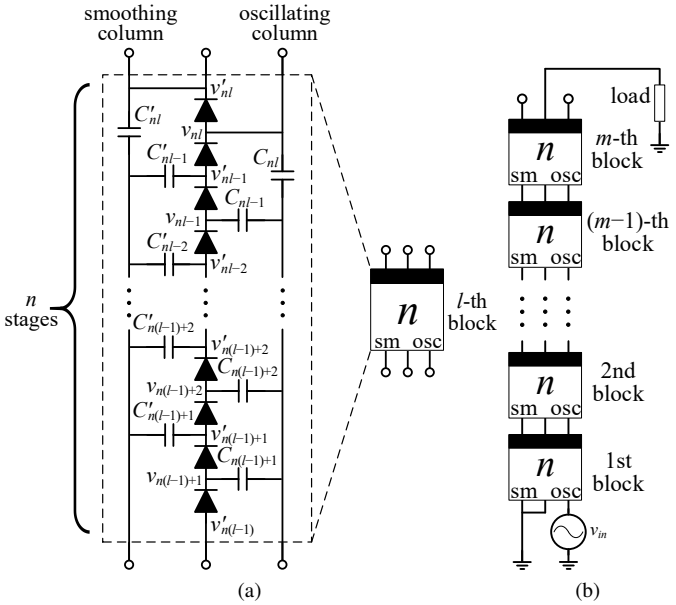


Fig. 6. The general model of a $(m\times n)$ hybrid multiplier. (a) The basic building block in which the first $(n-1)$ stages have a coupling capacitor on the horizontal branch, and the n-th stage has its capacitor on the vertical branch. (b) The entire voltage multiplier structure consisting of m blocks.

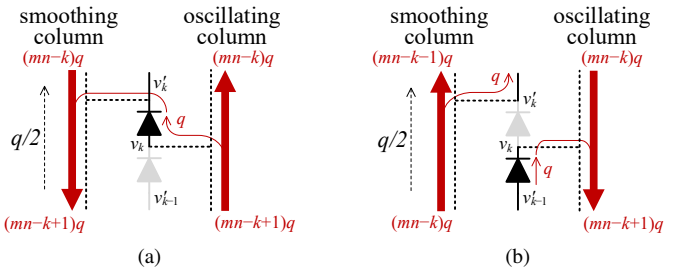
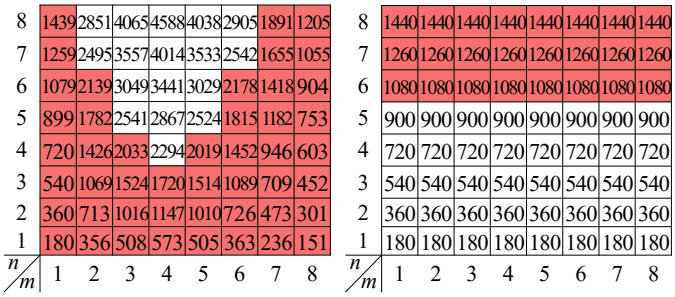


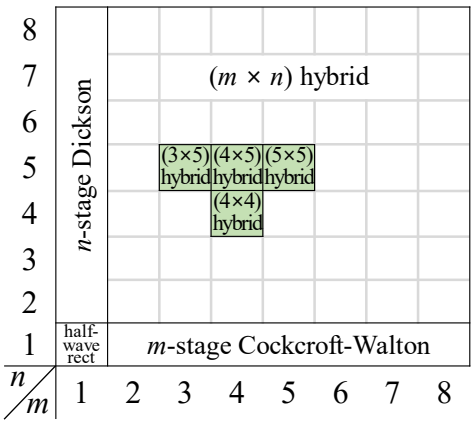
Fig. 7. Charge flow at the k-th stage of a $(m\times n)$ hybrid multiplier. The input spike current (red arrow) and the dc output current (dotted arrow) have a temporal profile similar to those in Fig. 1 and 4. (a) Charge flow during the *push* phase. (b) Charge flow during the *pull* phase.

TABLE III
THE VOLTAGE DROP IN EACH INTERMEDIATE NODE OF AN $(m \times n)$ HYBRID MULTIPLIER.

k	ΔV_k (same for $\Delta V'_k$)
1	q/C
$\vdots$	$\vdots$
$n-1$	q/C
n	$q/C[(m-1)n+1]$
$n+1$	$q/C[\{(m-1)n+1\}+1]$
$\vdots$	$\vdots$
$2n-1$	$q/C[\{(m-1)n+1\}+1]$
$2n$	$q/C[\{(m-1)n+1\}+\{(m-2)n+1\}]$
$2n+1$	$q/C[\{(m-1)n+1\}+\{(m-2)n+1\}+1]$
$\vdots$	$\vdots$
$\vdots$	$\vdots$
$ln-1$	$q/C[\sum_{z=1}^{l-1}\{(m-z)n+1\}+1]$
ln	$q/C[\sum_{z=1}^{l}\{(m-z)n+1\}]$
$ln+1$	$q/C[\sum_{z=1}^{l}\{(m-z)n+1\}+1]$
$\vdots$	$\vdots$
$\vdots$	$\vdots$
$mn-1$	$q/C[\sum_{z=1}^{m-1}\{(m-z)n+1\}+1]$
mn	$q/C[\sum_{z=1}^{m}\{(m-z)n+1\}]$



(a) (b)



(c)

Fig. 8. Colored tables to highlight the design procedure in section IV-B. (a) The average output voltage for 180 V peak-to-peak input and a 100 kΩ resistive load. (b) Capacitor voltage stress. The unit is volt. (c) Topology names that correspond to each combination of m and n.

ripple δV, we generalize Equations (3) and (4) as follows:

$$\Delta V = \sum_{k=1}^{mn} (\Delta V_k + \Delta V'_k) - \Delta V'_{mn} \tag{10}$$

$$\delta V = \Delta V'_{mn}. \tag{11}$$

Substituting entries of Table III into Equations (10) and (11), we obtain

$$\Delta V = \frac{q}{C}\left[m^3\left(\frac{2}{3}n^2\right) + m^2\left(-n^2+\frac{3}{2}n\right) + m\left(\frac{1}{3}n^2+\frac{1}{2}n-1\right)\right] \tag{12}$$

and

$$\delta V = \frac{q}{C}\left[m^2\left(\frac{n}{2}\right) + m\left(1-\frac{n}{2}\right)\right]. \tag{13}$$

The average output voltage V_{out} is

$$V_{out} = v'_{mn,avg} \approx mnV_{pp} - \Delta V - \frac{1}{2}\delta V. \tag{14}$$

The highest voltage stress on capacitors $V_{C,max}$ is

$$V_{C,max} = nV_{pp}. \tag{15}$$

As a sanity check, evaluating Equations (12) and (13) for $(m,n) = (1,4)$, $(4,1)$, and $(2,2)$ yields entries of Cockcroft-Walton, Dickson, and hybrid columns in Table II, respectively.

Also, putting $n = 1$, we get

$$\Delta V = \frac{q}{C}\left[\frac{2}{3}m^3 + \frac{1}{2}m^2 - \frac{1}{6}m\right] \tag{16}$$

and

$$\delta V = \frac{q}{C}\left[\frac{1}{2}m^2 + \frac{1}{2}m\right] \tag{17}$$

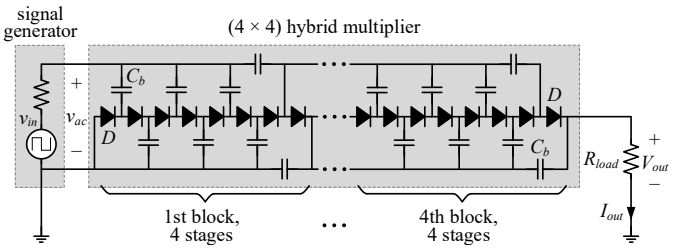
which are the same results as those found in many academic papers (e.g., [5], [28]) and textbooks [19]–[21] regarding an m-stage Cockcroft-Walton multiplier.

B. Design Example

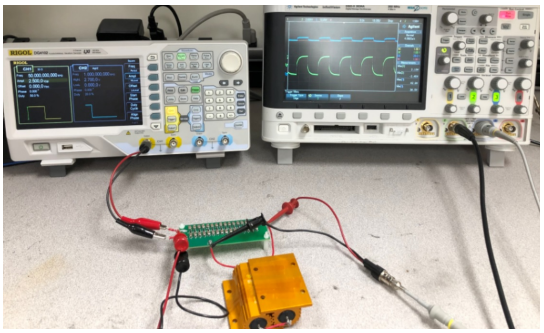
We give a design example to illustrate the practical use of the proposed topology. The goal is as follows: *Using a 10 MHz (f), 180 V peak-to-peak ac voltage (V_{pp}) as the input, design a voltage multiplier that delivers at least 50 W to a 100 kΩ (R_{load}) resistive load. Available capacitors have a value of 2.2 nF (C) and are rated at 1 kV, i.e., the capacitor voltage stress should be 1 kV or less.*

First, we calculate the output voltage V_{out} of an $(m \times n)$ multiplier. Since the load is resistive, from (1) it follows that

$$q = \frac{\langle i_{out} \rangle}{f} = \frac{V_{out}}{R_{load} f}. \tag{18}$$



(a)



(b)

Fig. 9. Experimental setup for the model verification. (a) Schematic. V_{out} and I_{out} denotes the output voltage and current, respectively. (b) Photograph.

Substituting (18) for q in (12) and (13), and plugging in these two expressions for ΔV and δV into (14), we obtain a first-order equation that can be solved for V_{out}.

Values of V_{out} solved for m and n from 1 to 8 are summarized in Fig. 8a. For 50 W power to be delivered to 100 kΩ, the output voltage should be 2236 V or larger. Subsequently, cells where V_{out} is less than 2236 V are shaded red. Capacitor voltage stress is calculated by (15) and shown in Fig. 8b. Again, cells where the voltage stress is larger than 1 kV are shaded red.

Fig. 8c shows topology names that correspond to each combination of m and n. Combinations that survived the filtering process of Fig. 8a and Fig. 8b are highlighted in green. Among those four topologies, namely (4×4), (3×5), (4×5), and (5×5), we choose (4×4) topology because the capacitor voltage stress is well below 1 kV and its parts count is close to minimal. (The minimal parts count is achieved by (3×5).)

V. Experimental Results

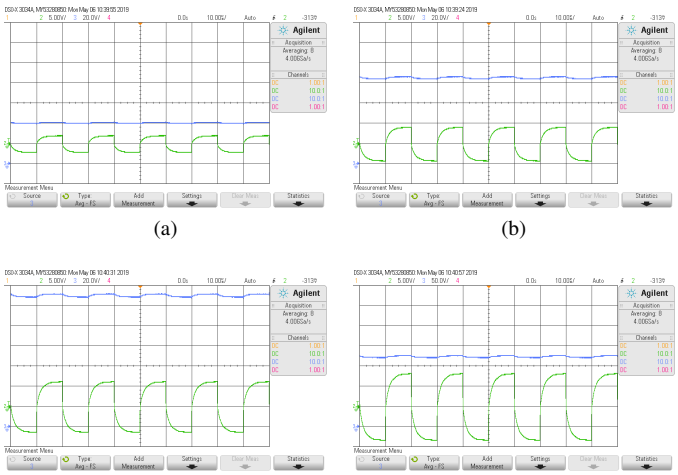
A. Model Verification

The first experiment is to validate general model equations (12) regarding the output voltage drop, and (13) regarding output ripple. We build a (4×4) hybrid voltage multiplier, measure the output voltage and its ripple, and compare those values with theoretical and simulated values. Fig. 9a and Fig. 9b are the schematic and the photograph of the test setup.

We design the experiment so that the test condition is close to ideal. For that purpose, we use large coupling capacitors (0.2 µF), small silicon Schottky diodes with low parasitic capacitance (10 to 20 pF), light load (100 kΩ), and low switching frequency (50 kHz). Table IV lists parameters relevant to the test condition.

TABLE IV
Test condition for the model verification.

Item	Description
v_{in}	square wave, 50 kHz
D	BAT240A, Infineon
C_b	0.2 µF, C0G
R_{load}	100 kΩ



(a) (b) (c) (d)

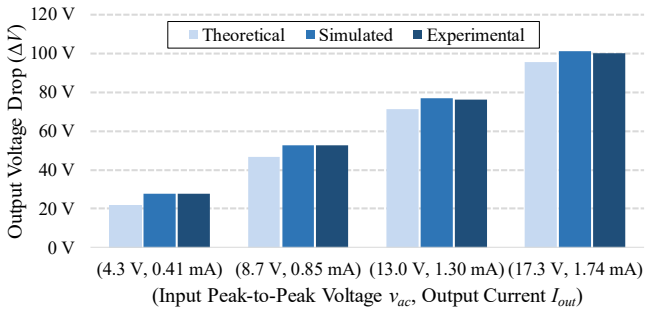
Fig. 10. Input voltage v_{ac} (green curves) and output voltage V_{out} (blue curves) measured for the model verification. Horizontal scale is 10 µs/div. Vertical scale is 5 V/div for v_{ac}, 20 V/div for V_{out} in a to c, and 50 V/div for V_{out} in d. (a) $(v_{ac}, I_{out}) = (4.3\ \mathrm{V}_{pp}, 0.41\ \mathrm{mA})$. (b) $(v_{ac}, I_{out}) = (8.7\ \mathrm{V}_{pp}, 0.85\ \mathrm{mA})$. (c) $(v_{ac}, I_{out}) = (13.0\ \mathrm{V}_{pp}, 1.30\ \mathrm{mA})$. (d) $(v_{ac}, I_{out}) = (17.3\ \mathrm{V}_{pp}, 1.74\ \mathrm{mA})$.

We measure the output voltage at four different sets of input voltage and output current. Fig. 10 shows measured waveforms. Fig. 11 summarizes the test results. Theoretical values in those plots are obtained by (12) and (13). Simulated values are obtained by using the diode SPICE model from manufacturer's website, which includes the parasitic capacitance and forward voltage drop. Results show that measured values match theoretical predictions by difference of 25 % or less. Also, half or more of those differences are predicted from simulation and thus can be explained by the influence of diode parasitic capacitance and forward voltage drop.

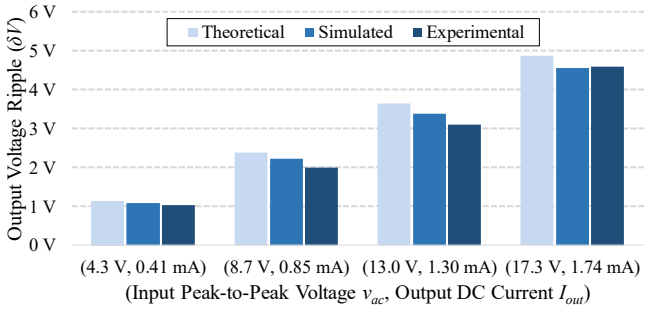
B. 60 V-to-2.25 kV DC-DC Converter Demonstration

The second experiment's goal is twofold: to verify the voltage multiplier design from section IV-B, and to demonstrate a dc-dc converter that is more relevant to real-world applications. First, we build a 60 V input, 10 MHz class-E resonant inverter to create a 180 V peak-to-peak ac voltage. Next, we implement the previously designed (4×4) hybrid multiplier and connect it to the inverter. We then measure the output voltage and capacitor voltage stress to verify the general model in section IV-A.

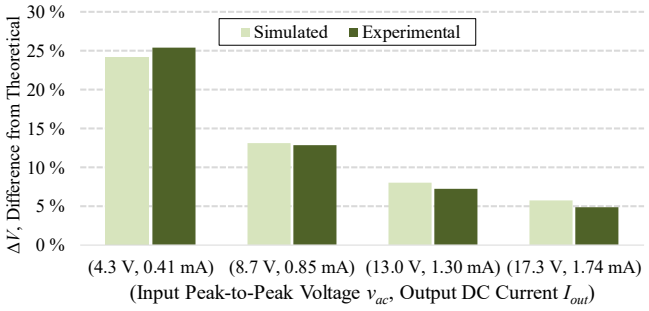
Fig. 12a and Fig. 12b are the schematic and the photograph of the test setup. Table V specifies the test condition.



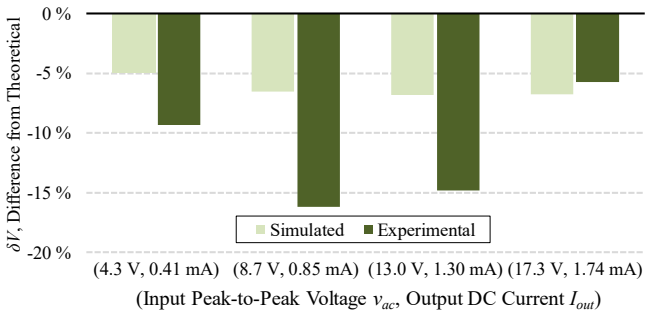
(a)



(b)

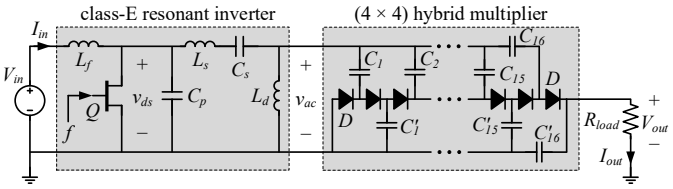


(c)

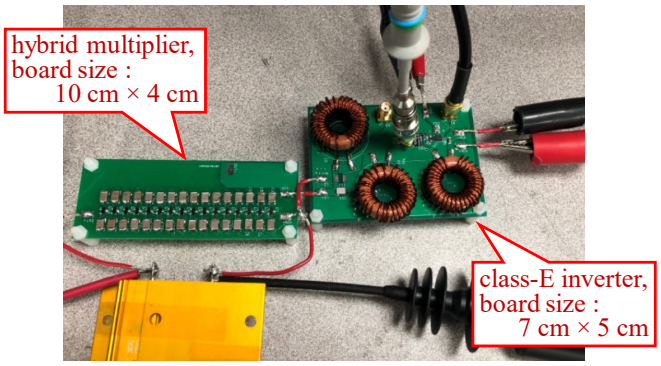


(d)

Fig. 11. Measured data compared to simulated and theoretical values at four different input and output conditions. (a) Output voltage drop. (b) Output peak-to-peak ripple. (c) Percent difference of the output voltage drop from theoretical prediction. (d) Percent difference of the output ripple from theoretical prediction.



(a)



(b)

Fig. 12. Experimental setup for the 60 V-to-2.25 kV dc-dc converter test. (a) Schematic. (b) Photograph.

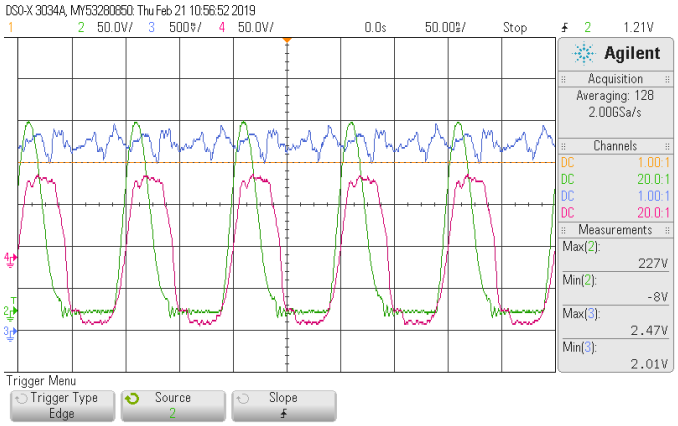


Fig. 13. Voltage waveforms captured when the dc-dc converter is in operation. The horizontal scale is 50 ns/div. channel 2 (green): v_{ds}, 50 V/div; channel 3 (blue): V_{out}, 500 V/div; channel 4 (pink): v_{ac}, 50 V/div. The ripple in channel 3 is due to the noise coupled to the differential probe and does not represent the ripple at the converter output.

Fig. 13 shows voltage waveforms captured during the circuit operation. The class-E inverter generates a 0 V-to-230 V ac voltage at its transistor drain node (v_{ds} in Fig. 12a, green curve in Fig. 13), which after filtration by L_s and C_s become a 176 V peak-to-peak ac voltage (v_{ac} in Fig. 12a, pink curve in Fig. 13) that drives the (4×4) multiplier. The multiplier output is measured to be 2.25 kV dc (V_{out} in Fig. 12a, blue curve in Fig. 13). This experimental result is close to the intended multiplier design of section IV-B where the input is 180 V ac and the output is 2.29 kV dc. Note that the ripple of the output voltage waveform is due to the noise coupled to the differential probe and does not represent the ripple at the converter output. Table VI summarizes the test result. The dc-dc converter achieves efficiency of 90.9 % and a voltage gain of 37.5.

TABLE V
TEST CONDITION FOR THE DC-DC CONVERTER.

Item	Description	Item	Description
V_{in}	60 V	C_s	2.2 nF
L_f	1.2 µH	L_d	1.3 µH
Q	GS66502B, GaN Systems	D	BAT240A, Infineon
f	10 MHz	$C_1, \cdots, C_{16}$	2.2 nF
C_p	100 pF	$C'_1, \cdots, C'_{16}$	2.2 nF
L_s	1 µH	R_{load}	100 kΩ

TABLE VI
DC-DC CONVERTER TEST RESULT.

I_{in}	v_{ac}	$V_{C,max}$	V_{out}	efficiency
928 mA	176 V_{pp}	660 V	2.25 kV	90.9 %

The highest capacitor voltage stress is measured 660 V as shown in Fig. 14. This value matches the prediction of 720 V from Fig. 8b within 10 % difference. Therefore, we conclude that the experiment validates the model and its ability to yield practical results.

Interestingly, experimental data in Fig. 14 show less sagging as the number of multiplier stages increases, compared to simulated values with ideal capacitors. We believe this phenomenon is caused by parasitic series inductance in real capacitors. We confirmed through measurement that 2.2 nF capacitors used in the voltage multiplier have an equivalent series inductance (ESL) of 2.8 nH, thereby presenting a lower impedance than ideal capacitors over the frequency range of 10 MHz to 90 MHz. Indeed, simulation produces a better match with the experiment when ESL is included in the model.

VI. CONCLUSION

This paper presented a voltage multiplier topology that is a hybrid of Cockcroft-Walton and Dickson topologies. The Cockcroft-Walton topology puts relatively low voltage stress on its blocking capacitors, but it suffers from a significant output voltage drop as the number of multiplier stages increases. The Dickson topology is the opposite of Cockcroft-Walton, having a low output voltage drop but at the expense of high capacitor voltage stress. The reason is that Cockcroft-Walton structure has all coupling capacitors in series and Dickson structure has all of them in parallel.

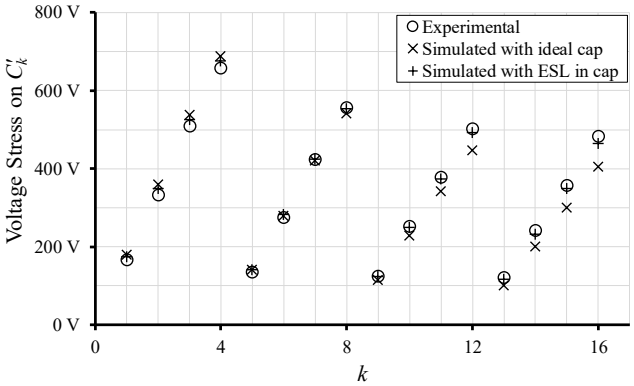


Fig. 14. Capacitor voltage stress measured from the hybrid voltage multiplier in Fig. 12a. The highest voltage stress is 660 V on C'_4. Simulation with an equivalent series inductance (ESL) of 2.8 nH in coupling capacitors produces a better match with the experiment, compared to the one with ideal capacitors.

Based on this observation, we proposed a voltage multiplier topology that has both series and parallel blocking capacitors that are put together in a pattern so that it takes advantage of both Cockcroft-Walton and Dickson structures. We analyzed a voltage multiplier with m series capacitors in total and n parallel capacitors between them, which we named a $(m \times n)$ hybrid multiplier. The analysis shows that $(m \times n)$ hybrid structure reduces the capacitor voltage stress by m times compared to Dickson while at the same time significantly reducing the output voltage drop compared to Cockcroft-Walton.

Experiments with a (4×4) hybrid multiplier verified that the model we developed accurately predicts the output voltage drop and ripple. Also, experiments with a 2 kV (4×4) voltage multiplier showed that the proposed topology indeed reduces the capacitor voltage stress as predicted by the analysis. Finally, we demonstrated the relevance of the proposed topology to real-world applications by building a 90.9 % efficient, 60 V in, and 2 kV out dc-dc converter.

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