Investigation of Electrostatic Gating in Two-Dimensional Transitional Metal Dichalcogenide (TMDC) Field Effect Transistors (FETs)

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***Abstract*—In the active and growing explorations of the rapidly emerging two-dimensional (2D) electronic and optoelectronic devices based upon atomically thin semiconductors and their heterostructures, developing better understanding of electrostatic gating is very important, especially for realizing logic and switching devices by employing 2D field effect transistors (FETs) with low subthreshold swing (SS) and high on-off ratio (I_{On}/I_{Off}). In this study, we propose and demonstrate a method that includes a combination of two-probe and four-probe *I-V* measurements on 2D transition metal dichalcogenide (TMDC) FETs to uncover the evolution of resistance of channel and contacts separately, upon change of gate voltage during switching between On and Off states. In 2D TMDC FETs with Schottky barrier (SB) contacts, we demonstrate that switching between On and Off states is primarily attained by modulating SBs due to change of electric field via electrostatic gating. Therefore, transistor characteristics is mostly determined by the contact resistance change upon the application of gate voltage. We present our method for 2D TMDC (MoS_2, $MoTe_2$) FETs. In addition, we also perform *C-V* measurements to investigate the presence of interface trap states and quantum capacitance in TMDC FETs.**

Keywords—2D materials, atomic layer semiconductors, field effect transistor (FET), transition metal dichalcogenide (TMDC), MoS_2, $MoTe_2$, Schottky barrier, capacitance, electrostatic gating

I. Introduction

Two-dimensional (2D) transition metal dichalcogenide (TMDC) materials have generated great interest at frontiers in the field of nanoelectronics for realizing future electronic and optoelectronic devices [1]. Due to the ultrathin nature of atomic layers of TMDCs and lower dielectric constants compared to that of silicon (Si), it is possible to realize 2D ultrathin body (UTB) field effect transistors (FETs) with greater immunity to short channel effects [2]. This shows great promise to extend Moore's law by attaining sub 5-nm channel length FETs, which is extremely challenging for traditional Si and even modern III-V MOSFETs [2].

In traditional, mainstream metal-oxide-semiconductor field effect transistors (MOSFETs), the On state of the transistor is defined by the formation of thin inversion layer at the surface of the semiconductor under gate for certain positive gate voltage, through which electrons can flow from source to drain (n-channel MOSFET). On the other hand, in 2D TMDC FETs, which are essentially metal-semiconductor FETs, transistor characteristics is dictated by the majority carriers unlike minority carriers in conventional MOSFETs. Therefore, in some studies, it is reported that 2D TMDC FETs are turned On at the accumulation regime under gate voltage [3]. Again, as these FETs generally exhibit metal-semiconductor SB contacts, it is also demonstrated that transistor characteristics are only controlled by modulation of SBs under the gate voltage [4]. In addition to that, it is also claimed that a metal-insulator transition (MIT) can happen due to carrier density modulation under gate voltage, which can contribute to the attained transistor characteristics [5, 6]. To date, however, there is no systematic experimental study to investigate the device physics pertaining to the electrostatic gating of 2D TMDC FETs.

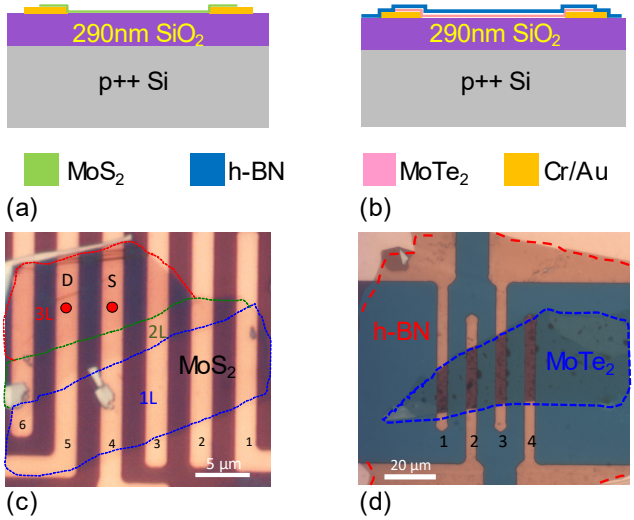

Fig. 1. (a)-(b) Cross-section-view illustrations of the 2D FETs. (c)-(d) Optical images of typical fabricated MoS_2 and $MoTe_2$ FETs, respectively.

In this paper, we aim to address the underlying device physics behind electrostatic gating by incorporating systematic *I-V* and *C-V* measurements. We perform these measurements on 2D molybdenum disulfide (MoS_2) and molybdenum ditelluride ($MoTe_2$) FETs. Our measurements show that SB barrier modulation plays a primary role in the transistor characteristics of 2D TMDC FETs with back gate geometry. Furthermore, operating 2D FETs in the accumulation regime is

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not a necessary condition for turning on these FETs. Moreover, we demonstrate that, in addition to intrinsic doping type, carrier polarity can also be determined by the SB heights. With the facilitation of *C-V* measurements, important insights of electrostatic gating have also been uncovered.

II. Fabrication and Measurement

A. Device Fabrication

2D TMDC FETs are fabricated by dry transferring mechanically exfoliated MoS_2 (1-3L) and $MoTe_2$ (~10L) flakes onto 290nm SiO_2-on-Si substrate with pre-patterned electrodes (5 nm Cr for adhesive layer followed by 40 nm Au for contact electrode) [7]. Here, heavily p-doped Si substrate is used as the back gate for the FETs (Fig. 1a and 1b). For $MoTe_2$ FETs, a hexagonal boron nitride (h-BN) flake is transferred on top of $MoTe_2$ to prevent oxidation, as $MoTe_2$ tends to oxidize in air over time, which could severely degrade the performance of FETs. The channel lengths of MoS_2 and $MoTe_2$ FETs are 2 µm and 7.5 µm, respectively (Fig. 1c and 1d). After fabrication, we employ thermal annealing in moderate vacuum (15 mTorr) with furnace temperature up to 150˚C ($MoTe_2$) and 250˚C (MoS_2) for 1 hour in dry N_2 gas flow environment [7].

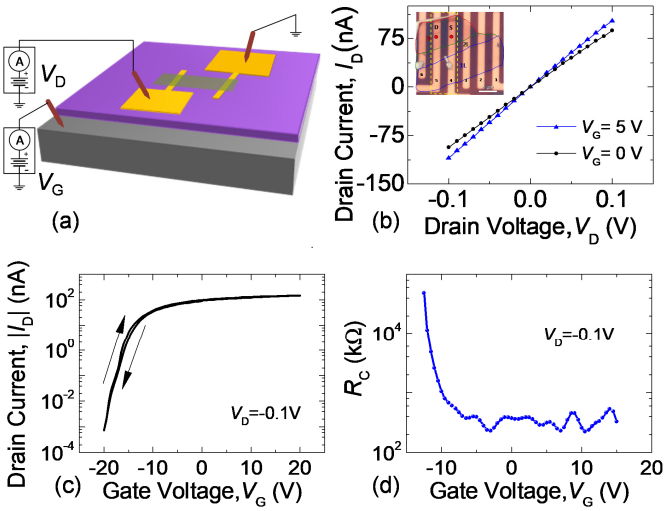

Fig. 2. (a) Two-probe measurement setup for MoS_2 FET. (b) Transport (I_D-V_D) characteristics of MoS_2 FET. (c) Transistor (I_D-V_G) characteristics of the MoS_2 FET. (d) Extracted R_C from two-probe measurement by the YFM method.

B. Electrical Measurement

We perform *I-V* measurement on the FETs using a Keithley 4200A-SCS semiconductor parameter analyzer. During two-probe measurement, two source measurement units (SMU) are connected to the drain (D) and gate (G) for obtaining transport (I_D-V_D) and transistor transfer (I_D-V_G) characteristics (Fig. 2a). On the other hand, for four-probe resistance measurement, a constant current is flowed between the two outer electrodes by using one SMU as a current bias (I_{bias}) and another as a ground. Two SMUs are employed to measure voltage difference between the two inner electrodes (Fig. 3a). In addition to these, we also perform *C-V* measurement using Keithley 4210-CVU capacitance-voltage unit at different AC frequencies.

III. Results and Discussions

At first, we perform *I-V* measurement on a MoS_2 FET (electrodes labelled 4 and 5 in Fig. 1c). I_D-V_D characteristics in Fig. 2b show linear behavior, which indicates the presence of low contact resistances at the contacts. Figure 2c shows n-type transistor behavior with very good I_{On}/I_{Off} ~10^6 and threshold voltage (V_{th}) of -5V. We extract the contact resistance (R_C) of the MoS_2 FET under different gate voltage (V_G) by using the Y-function method (YFM) [8] from two-probe measurement (Fig. 2d). Interestingly, it shows that although transport characteristics exhibit linear behavior, there is a significant SB and R_C, which also increases at Off state. This leads us to further perform four-probe measurement, in order to determine the channel resistance (R_{Ch}) and the R_C directly.

Figure 3 presents the four-probe measurement results of the MoS_2 FET mentioned in the last paragraph. I_{bias} is applied between 3 and 6, where voltage difference is measured between 4 and 5 (Fig. 1c). Figure 3b shows the four-probe resistance or R_{Ch} of MoS_2 with respect to V_G. It is obvious from this measurement that R_{Ch} increases only 3 times when FET is switched from On to Off state, whereas previous two-probe I_D-V_G measurement demonstrates I_{On}/I_{Off} ~10^6. We can calculate, $R_C = 0.5(R_{two\text{-}probe}\text{-}R_{Ch})$. R_C exhibits about four orders of magnitude increase (it can be even more as the measured resistance at Off state is limited by the compliance settings) when FET is turned Off from On state (Fig. 3c). This clearly demonstrates that transistor characteristics of MoS_2 FET is dictated by V_G induced contact resistance change due to SB modulation, as contacts are under control of back gate.

We also perform two-probe measurements on $MoTe_2$ FETs (electrodes labelled 1-2 and 3-4) (Fig. 1d). Unlike MoS_2 FETs, these FETs do not show clear linear characteristics in I_D-V_D measurements, which indicates that R_C is considerably higher compared to MoS_2 FETs (Fig. 4a and 4c). Due to higher R_C, four-probe measurement cannot reliably determine R_{Ch} [9]. These FETs also show unipolar n-type behavior with comparatively lower I_{On}/I_{Off} ~10^4 compared to MoS_2 FETs (Fig. 4a and 4c). However, interestingly, V_{th} for $MoTe_2$ FETs is found at positive voltage (8-10V) in contrast to the negative V_{th} of MoS_2 FET. From literature, it has been found that MoS_2 and $MoTe_2$ are intrinsically n-type [10] and p-type [11] doped, respectively, due to defects or vacancies. However, the carrier polarity of 2D SBFET is also determined by the SB height for electrons and holes. If SB height for electrons (SBH_e) is lower than that for holes (SBH_h), $SBH_e < SBH_h$, then n-type behavior is observed from the 2D SBFET. Alternatively, for $SBH_h < SBH_e$, p-type behavior is obtained [4]. In 2D SBFETs, V_{th} is defined as the gate voltage value at which majority carriers can start to tunnel through the SB. As a result, provided that $SBH_e < SBH_h$, for n-type semiconductor (MoS_2), V_{th} is usually negative; or in other words, the device is 'normally On'. Conversely, for p-type semiconductor ($MoTe_2$), the device is 'normally Off', and it requires some positive V_G to achieve the threshold condition, in order to turn On. These are explained by using band diagrams in Fig. 5. When $V_G<V_{th}$, electrons are blocked at the metal-semiconductor SB contacts. At $V_G=V_{th}$, electrons start to overcome the barrier by thermionic emission. Finally, at $V_G>V_{th}$, electrons tunnel through the SB as the SB becomes sufficiently narrow (Fig. 5b and 5d).

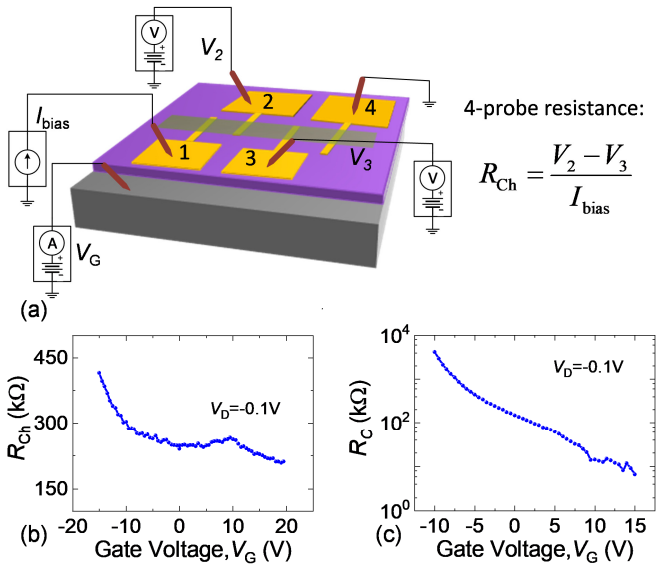

Fig. 3. (a) Four-probe measurement setup for MoS_2 FET. (b) and (c) Channel resistance (R_{Ch}) and contact resistance (R_C) obtained from the MoS_2 FET.

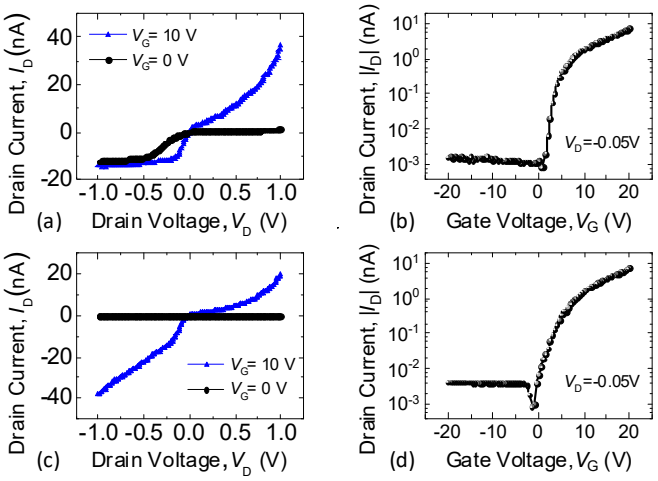

Fig. 4. (a)-(b) Transistor transport and transfer characteristics obtained from the $MoTe_2$ FET (electrodes labelled 1 and 2 in Fig. 1d). (c)-(d) Similar results obtained from the $MoTe_2$ FET with electrodes labelled 3 and 4 in Fig. 1d.

Next, we perform *C-V* measurements on both MoS_2 and $MoTe_2$ FETs. Figure 6b presents the equivalent circuit model for the capacitors related to 2D TMDC FETs, where C_{OX}=gate oxide capacitance, C_Q=quantum capacitance, and C_{It}=interface trap charge capacitance. C_Q is originated from the necessity of additional kinetic energy to induce carriers in the channel of 2D TMDC FETs due to low density of states (DOS) of 2D materials. It can be expressed as $C_Q = e^2 DOS_{2D}$, where e = electron charge [12]. C_{It} is the capacitance originated from interface trap charges between 2D semiconductors and dielectrics, which can be formulated as $C_{It} = \frac{e^2 D_{It}}{2\pi f \tau_{it}} \tan^{-1}(2\pi f \tau_{it})$, where D_{It} is interface trap charge density ($cm^{-2}eV^{-1}$) and τ_{It} is the time constant for D_{It}. The total capacitance (C_{Total}) expression can be written as below [12]:

$$\frac{1}{C_{Total}} = \frac{1}{C_{OX}} + \frac{1}{C_Q + \frac{e^2 D_{It}}{2\pi f \tau_{it}} \tan^{-1}(2\pi f \tau_{it})} . \quad (1)$$

This capacitor model indicates that C_{Total} decreases with the increasing frequency, as C_{It} is unable to respond at higher frequency and $\frac{1}{C_{Total}}$ reduces to $\frac{1}{C_{Total}} = \frac{1}{C_{OX}} + \frac{1}{C_Q}$.

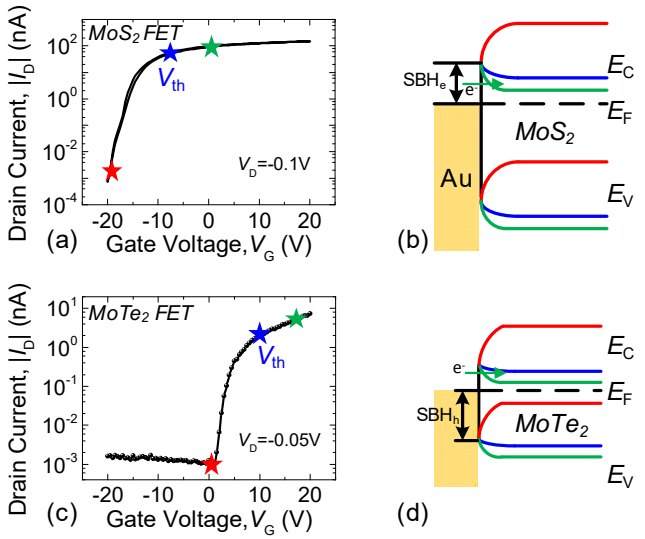

Fig. 5. (a) Measured I_D-V_G characteristics and (b) band diagrams from the MoS_2 FETs showing Schottky barrier modulation under different gate voltage, where blue, green and red colors indicate the corresponding points on the I_D-V_G curve. (c)-(d) Similar I_D-V_G curve and band diagrams from the $MoTe_2$ FETs.

Figure 6c and 6d show *C-V* characteristics measured from the MoS_2 and $MoTe_2$ FETs, respectively. We observe a clear difference between the *C-V* characteristics of MoS_2 and $MoTe_2$ FETs. For MoS_2 FET, at On state (V_G > -5V), C_{Total} approaches the value of oxide capacitance (C_{OX}) (~11 nF/cm^2). It indicates that MoS_2 FET operates near the accumulation regime, where C_Q becomes larger ($C_Q > C_{OX}$), as Fermi level (E_F) approaches the conduction band. As C_{Total} is dictated by the value of the smaller capacitance, C_{Total} is close to C_{OX}. On the other hand, for $MoTe_2$ FET, C_{Total} is about 5 to 6 times smaller than C_{OX} at On state (V_G > 10V). It means that C_Q is still lower, due to the fact that E_F is located deep inside the bandgap, as $MoTe_2$ is intrinsically p-doped. As a result, it also indirectly supports that for 2D SBFETs, it is not always necessary to operate the FETs in accumulation regime or inversion regime, in order to switch On the transistor. However, at much higher positive V_G (>30V), C_{Total} starts to increase, which indicates that channel starts to enter inversion regime. Alternatively, C_Q starts to increase as E_F approaches E_C.

We also investigate the frequency dependence of C_{Total} at the On state of FETs. Figure 7a shows that for both FETs, C_{Total} decreases with increasing frequency, which is consistent with

Eq. (1). It is also worth mentioning that at low frequency, C_{Total} for MoS_2 FET is close to C_{OX} (~11 nF/cm^2), which indicates that C_{It} or D_{It} is quite high and makes the second term of Eq. (1) smaller. Figure 7b presents the *C-V* characteristics of the $MoTe_2$ FET at different AC frequencies, which shows the decline of C_{Total} at higher frequency. However, the explanation of the increase in C_{Total} at Off state of $MoTe_2$ FET at higher frequency requires further investigation (Fig. 7b).

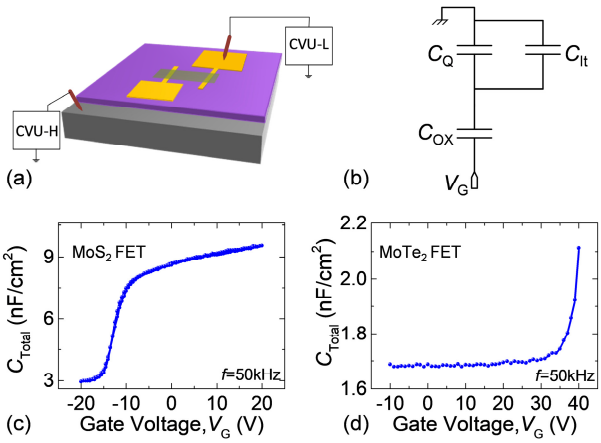

Fig. 6. (a) *C-V* measurement setup. (b) Equivalent model of the capacitors. (c)-(d) Measured *C-V* characteristics of MoS_2 and $MoTe_2$ FETs, respectively.

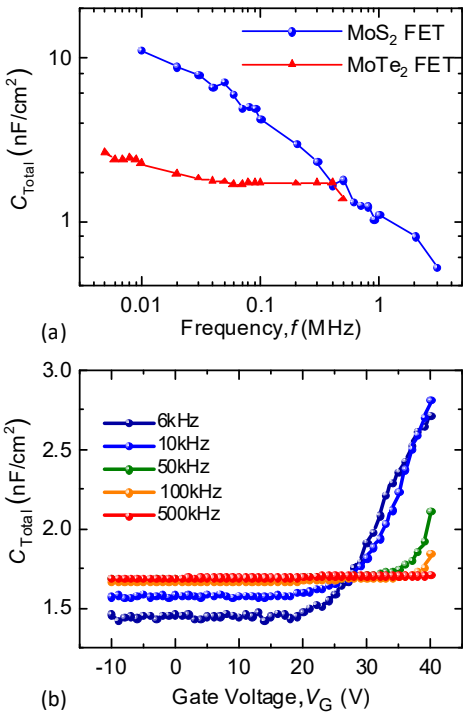

Fig. 7. (a) Change of C_{Total} with respect to frequency for both MoS_2 and $MoTe_2$ FETs operating at the On state. (b) Measured *C-V* characteristics of the $MoTe_2$ FET at different probing frequencies.

IV. Conclusions

In summary, we have made experimental studies to shed light on better understanding of the electrostatic gating of 2D TMDC FETs in switching operations. From experiments, we can conclude that transistor characteristics in 2D TMDC FETs with Schottky contacts and back gate geometry are dictated by Schottky barrier modulation under electrostatic gating. In comparison to the change in contact resistance under gating, channel resistance changes in very small amount. We also point out that Schottky barrier height can play an important role in determining carrier polarity of FETs, irrespective of the initial doping types of the 2D semiconductors. Finally, we demonstrate that *C-V* measurement can provide important insights into understanding the electrostatic gating.

Acknowledgments

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