Velocity-Controlled Oscillators for Hippocampal Navigation on Spiking Neuromorphic Hardware

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***Abstract*—Grid, place, and border cells in the mammalian hippocampus and entorhinal cortex perform highly sophisticated navigational tasks with an extremely low power budget. While previous algorithms for simultaneous localization and mapping (SLAM) in robotics have used these cells for inspiration, they have sacrificed the robust, low-power gains achieved with bioplausible models for ease of implementation. This paper presents steps towards robotic navigation with biologically realistic hippocampal models by implementing velocity-controlled oscillators, a basis for any spatially-tuned neuron, on mixed-mode neuromorphic spiking hardware.**

I. Introduction

Robotic navigation requires learning new environments, or changes to a known environment, concurrent with real-time localization of the robot within said environment; this methodology, known as Simultaneous Localization And Mapping (SLAM), typically requires mathematically complex computation and the fusion of input data across many sensory modalities. Thus, prototypical SLAM implementations are often realized as over-sensored, power hungry devices. This becomes an unsuitable navigation paradigm for low-power mobile robotics applications, where algorithms must be executed at low costs, often in the presence of high noise. Animals, however, are able to navigate new environments and learn salient features with extremely low energy costs and limited sensory information. Accordingly, neurally-inspired approaches to SLAM are quite promising for providing robust, power-starved performance.

Previous neural SLAM implementations [1]–[4] take inspiration from general models of spatial coding and navigation in rat hippocampus and parahippocampal regions. These implementations, while brain-inspired, do not explicitly model navigational cells in the brain or include biologically-plausible spiking neurons. The algorithmic organization reflects general principles of rodent navigation, but lower-level representations, transformations, and computations eschew neural implementations for traditional computational techniques. By failing to seek bioplausibility, these models fail to take advantage of the power saving nature of neuromorphic systems, on both a software and hardware level [5]. In this paper, we present an implementation of biologically faithful spatial coding cells in neuromorphic hardware.

A. Spatial Coding in the Hippocampus

Neurons in the hippocampus and parahippocampal regions of mammalian brains demonstrate surprisingly complex and stable spatial firing patterns, remarkable enough to merit two Nobel prizes. These cells, which fire selectively at particular spatial locations in both novel and familiar environments, are organized into several categories by the particular spatial pattern which they encode. Grid cells fire when the animal is at one of multiple discrete locations that form a hexagonal lattice within an environment; place cells fire when the animal is at one (or a few) specific location(s); "border cells" fire when the animal is near or at the border of an environment [6], [7]. The spatial responses of these neurons develop within weeks of birth [8], respond differently in different environments [9], and persist even without visual input [10]. Taken together, these cells form complex, feature-rich, and stable cognitive maps of physical space. Additionally, they track instantaneous animal location in allocentric space by integrating velocity over time, a process referred to as path integration. By performing localization while building and maintaining environmental maps, this suite of cells provide a low power, sensor-deprived, robust SLAM implementation.

II. Computational Models

A number of models exist to describe the neural dynamics that underlie the stable spatial firing maps of hippocampal neurons; one such class of model is the Oscillatory Interference (OI) model. The OI model arises from the experimental observation that spatial navigation cells are modulated by a theta-rhythm (4-12 Hz) oscillation in neural spiking dynamics. Fundamentally, OI models propose that stable spatial firing maps emerge from interference patterns between neural oscillators whose spiking frequency depends on animal velocity. Integrating frequency over time produces phase, just as integrating velocity over time produces location; thus, OI models encode location through path integration in the relative instantaneous phases of multiple oscillators. Many OI models of hippocampal navigation cells use idealized, rate-based methods for computation; however, spiking networks are both more faithful to neuroanatomy and computationally elegant [11], [12].

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A. Generalized Integrate-and-Fire Neuron Model

These spike-based networks require a computational model for spiking neurons; in this paper, we utilize a generalized integrate-and-fire neuron model [13]. This model provides a computationally simple implementation of many types of spiking neuron behavior, all within a small, biophysically motivated parameter space. The model implemented for this work is a simplified version of the original Mihalas-Niebur model, retaining much of the functionality at reduced computational cost and with successful neuromorphic hardware implementations [14]–[16]. While the simplified model can produce multiple neuronal behaviors, this work implements simple Class I spiking leaky integrate-and-fire neuron dynamics [17].

B. Oscillatory Interference Model

Many OI models exist that, with varying levels of complexity and robustness, give rise to spatial navigation cells. In this paper, we focus on a subset of OI models that create a Fourier-like representation of space by modelling spatial cells as some linear combination of a basis set of oscillators [18], [19].Like OI models more generally, these oscillators can be oscillatory spiking networks or ideal sinusoids.

The model implemented in this work consists of a basis of ring oscillators with angular frequency modulated by animal/robot velocity (direction and speed) around a base theta rhythm. The simple linear combination of some subset of these velocity-controlled oscillators (VCOs) can encode any arbitrary stable spatial activity map, including replicating the activity patterns of experimentally-observed grid, place, and border cells [20]. Each VCO activates maximally (i.e. has greatest angular frequency) when animal velocity moves in its preferred direction, and minimally in its anti-preferred direction.

In this model, a VCO is constructed of two interconnected neuron populations each of size M (as in Fig. 1). One group consists of excitatory neurons which synapse onto the other group, consisting of inhibitory cells. The inhibitory cells synapse recurrently as well as onto the excitatory group. All synaptic weights are assigned via Gaussian functions; excitatory-to-inhibitory and inhibitory-to-inhibitory weights are symmetric, while inhibitory-to-excitatory weights are asymmetric, causing unidirectional oscillation of an activity bump around the ring. The oscillation frequency is then controlled by the center frequency of a Poisson spike input to the excitatory group; the rate of this Poisson spike train is determined by modulating around a baseline of 3kHz with a scaled dot product of animal/robot velocity and VCO preferred direction.

III. Model Implementation

A. Integrate-and-Fire Array Transceiver

The Integrate and Fire Array Transceiver (IFAT) is a custom mixed mode chip implementing an array of neurons as capacitor pairs [21]–[23]. The chip, designed in 500nm CMOS technology, implements 2040 modified Mihalas-Niebur neurons, as

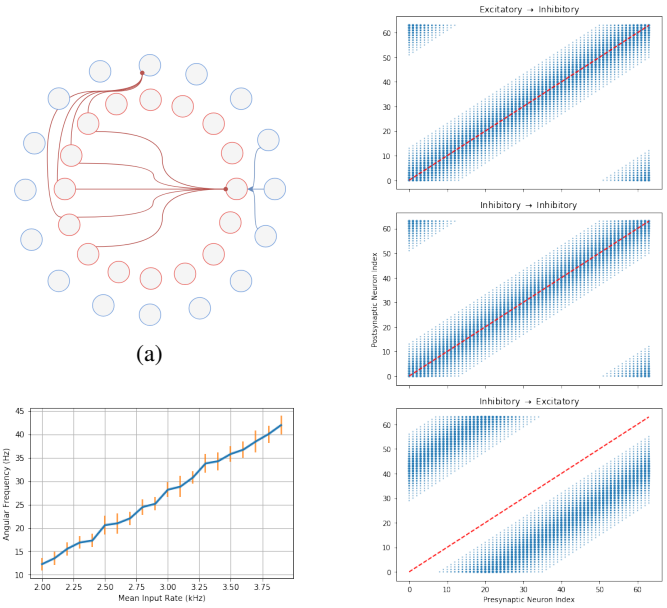


Fig. 1: Velocity-controlled oscillators in simulation. **(a)** Two equally-sized groups of neurons interact to form a single VCO; excitatory neurons (blue) project to inhibitory neurons (red), and vice versa. Inhibitory neurons also have recurrent connections. All weights are symmetric Gaussian distributions, except for the asymmetric inhibitory-to-excitatory projections. **(b)** Average tuning curve of VCO for 5 seconds of oscillation (error bars indicate standard deviation); synaptic connectivity of VCO **(c)**, where point size indicates relative weight of synapse, and red dotted line indicates symmetry.

described above. To maximize the density of the neuron array and minimize both power consumption and process variation-induced mismatch, all neurons in the array share a single synapse and soma. The synapse provides variable dynamic input events to neurons via a switch-capacitor circuit [24]; the soma consists of a comparator that creates an output spike when the membrane potential of a neuron exceeds its threshold potential. While leakage (both parasitic and intentional) occurs in parallel across all neurons in the array, input and output events are processed serially, as the entire array shares a single synapse and soma. The IFAT is currently operated at 48 MHz (USB communication clock), many orders of magnitude faster than a typical neural circuit; this allows events that are processed in close temporal proximity to be considered simultaneous.

Early versions of the IFAT control scheme consisted of an open loop system, sufficient for simple image processing tasks but not more general neural computation. This work represents the first example of general purpose neural processing on the IFAT. To achieve the necessary generality and robustness, a number of important features have been implemented, including feedback between neurons and time-stamping of registered spikes to allow for spike-time based computation.

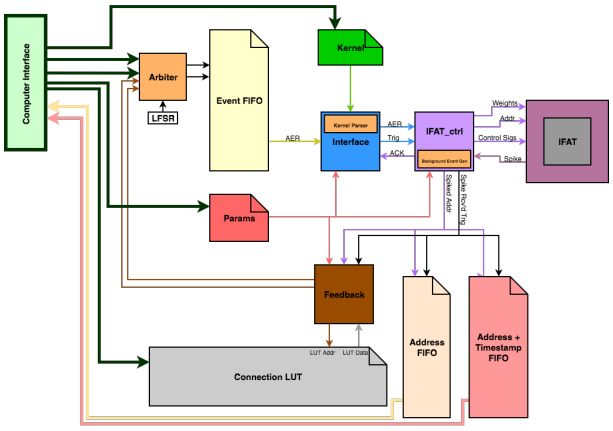


Fig. 2: Block diagram of the complete IFAT system, demonstrating significant digital control architecture to enable low-power, high-speed analog computation in the neuron array. One FPGA can control multiple IFATs in parallel and multiple FPGA-IFAT systems can interact, allowing for much larger and more complex networks than that of a single chip.

Feedback networking between neurons on chip is accomplished with a look-up table of connections, implemented as RAM and addressed indirectly, using the address of a neuron to compute the memory address at which a pointer to a list of events are stored. In this way, a single neuron can have many input and output connections with arbitrary excitatory or inhibitory magnitudes. An arbitrary number of connections can exist between an arbitrary number of neurons, limited only by the depth of the memory implemented.

As the system is asynchronous, a sensor or computer interface may attempt to write data to the event FIFO at the same time as the feedback module. In order to avoid both lock-up conditions and behavioral bias of a network, an arbiter was developed to randomly select data from either source (using the lowest bit of an appropriately sized LFSR) when there is contention. Even in cases of collision, all events are preserved and the system does not exhibit a bias for data from the sensor/computer or feedback module.

A pair of cascaded counters was implemented in order to provide a time-stamp for each spike that is recorded. The availability of this information makes it possible to calculate the inter-spike interval and spiking frequency of a neuron, providing other mechanisms for the encoding of data which can be used instead of, or in conjunction with, a rate-coding model focused entirely on mean spiking frequency [25]. This data is combined with the address of the spiking neuron to form an address event representation (AER) of a spike, which is then stored in memory for later retrieval and propagation.

B. Spiking Neuron Model Simulation

To allow for implementation of spiking VCO-based models in both software and hardware, we have developed a simulation of the IFAT neural hardware (see III-A) using the Brian Neural Simulator [26], [27]. The simulation assumes that the event-rate through the serial synaptic circuit is sufficiently greater than typical neuron firing rates such that synapses can be considered parallel, except in cases of multi-synapse connections between two neurons (where a realistic time delay is included). This assumption holds for VCO OI models, as maximum neuron firing rate is on the order of kHz, while the IFAT functions at MHz frequency. The simulator additionally models the parasitic leakage currents inherent in the hardware that are not described by the Mihalas-Niebur model dynamics. The simulator allows for rapid, programmed exploration of the parameter space for a spiking neural network to be implemented on the IFAT.

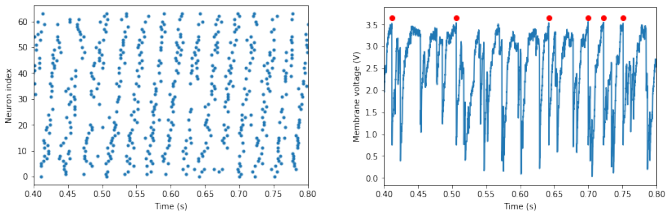
C. IFAT Model Implementation

Event streams, loaded in to a 32-bit FIFO, are used to provide input to the network implemented. Each event contains a magnitude and destination in AER, with connectivity patterns stored in RAM as described above. When an event causes a neuron to spike, the corresponding connections are loaded into an auxiliary FIFO, to be processed later. Events are sent in bursts, with a controllable burst frequency defined by a counter. During the time between bursts, if an event caused a neuron to spike and have connections loaded in to the auxiliary FIFO, these events are processed until either the auxiliary FIFO is empty or the next event burst is sent. Essentially the feedback and input event streams are merged to enable effectively parallel processing through a single synapse circuit. As spikes occur, the associated locations and timestamps are stored in an output FIFO. After all events in the input queue have been processed, this output queue is read and the relevant metrics of the resultant spike train (i.e. inter-spike interval, mean firing rate per neuron) are computed.

IV. Results

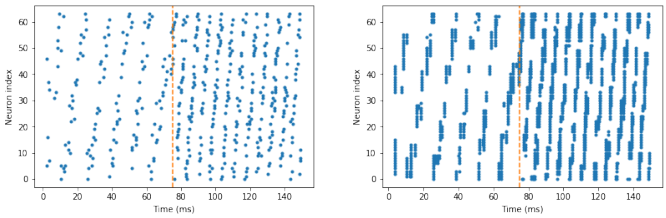
Spiking VCOs were initially demonstrated in the Brian simulator. The VCO size was empirically selected to be $M = 64$ (i.e. total size of $2M = 128$) neurons; this was the minimum size that retained robustness and oscillation. Example functionality of a VCO driven with a 3kHz Poisson spike input can be seen in Fig. 3. The angular frequency band achieved by the VCOs was approximately 12-42 Hz, roughly triple the theta band. Since oscillatory frequency relates to spatial frequency in grid cells, this higher frequency would lead to a finer grid pattern in a true navigational system [28]. However, as a proof of concept, this higher frequency is acceptable; in future designs, it could easily be accommodated by changing scaling factors.

VCOs were also implemented on the IFAT neural hardware, by mapping the spiking VCO model described above onto physical neuron circuits in the IFAT array. In particular, the connectivity matrices of the simulation were written into the feedback LUTs described above, and Poisson spike train inputs were applied to all excitatory neurons. Transferring from simulation to mixed-mode physical hardware, due to additional parasitic leakage currents, leads to slight and unpredictable changes in VCO angular velocity. Even so, the average rate



(a) (b)

Fig. 3: Example of Brian simulation of working VCO. (a) Spike patterns of the excitatory neuron group, where $M = 64$. (b) Voltage trace for a single excitatory neuron; red points indicate spike events. The Poisson input induces noise in network firing patterns, but the connectivity imposes a predictable and stable oscillation of activity around the ring.



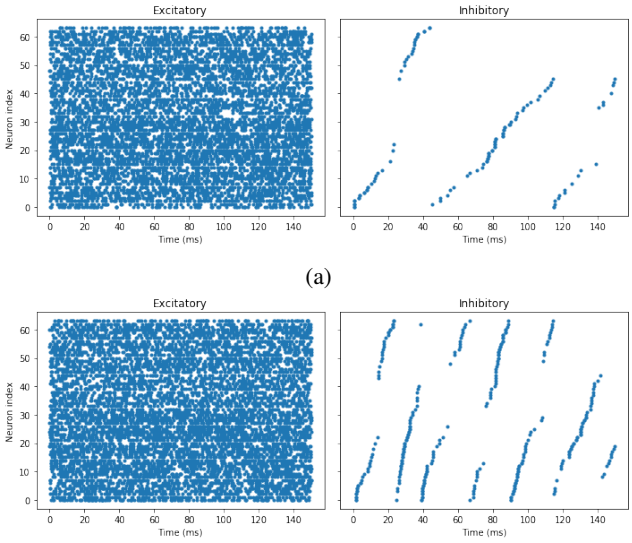
(a) (b)

Fig. 4: Simulated VCO implementation. Dotted line indicates transition from 2kHz to 4kHz Poisson input spike-train. Simulation in Brian simulator demonstrating increased oscillatory frequency after change in input. **(a)** Excitatory neuron population activity is sparser, while **b)** inhibitory neuron population is denser, with multiple neurons firing in a single simulated time step (vertically stacked points). This behavior is less often seen in hardware implementation, where spikes are always and necessarily processed serially.

of a Poisson input spike train to excitatory IFAT neurons is qualitatively proportional to the angular velocity of the inhibitory population of the VCO, as seen in Fig. 5.

In current IFAT architecture, only spike-based inputs to neurons are permitted, rather than the current-based inputs common to many computational models of neurons, including the original Mihalas-Niebur model [13]. In physically realizing the spiking VCO model on the IFAT, we see a potential drawback of this architectural choice; spike density in the excitatory population, which receives the velocity-dependent Poisson input, must be extremely high to induce oscillatory spiking in the inhibitory population. Parasitic currents are much higher in hardware, so porting networks from simulation to hardware requires lowering the threshold voltage of the neuron membrane. As such, the excitatory population fires far more frequently than in simulation (compare Figs. 4 and 5), increasing the power demands of the system. This remains a problem to be addressed in future architecture versions.

Grid cells may also be implemented by cross-coupling three or more VCOs, as described in [20]. Current IFAT technology



(a)

(b)

Fig. 5: VCO functionality on IFAT hardware. Poisson spike train with variable mean rate and timestep of $10\mu s$ was generated in Python ahead of runtime. **(a)** Mean Poisson stimulation rate of 1 kHz produces much slower inhibitory oscillation than **b)** a mean rate of 4 kHz. Spike rate of the excitatory population is quite stable, regardless of changes to input rate (7322 spikes at 1 kHz input rate; 7874 at 4 kHz).

does not support large enough connectivity matrices or fast enough input/output operations; however, these limitations are largely imposed by FPGA hardware, so future versions of the IFAT can implement more complex spatial navigation neurons. Conversely, the implementation of VCOs might be better suited to specialized hardware combining analog oscillators with AER spike generators, leaving the general-purpose IFAT to implement grid, place, and border cells. Such potential multi-chip architectures would reduce the feedback event load and FPGA-moderated inter-IFAT communication, circumventing the limitations described above.

V. Discussion

In this paper, we present an implementation of an oscillatory interference model of hippocampal spatial navigation cells on a spiking neuromorphic chip. This work also represents the first application of a complex spiking neural network on the IFAT hardware, showing its capacity for general-purpose neural computation beyond simple image processing. Implementing such complex spatial networks on low-power neuromorphic hardware is a necessary and important step towards low-power, robust, and bioplausible neurally-inspired navigation in such applications as mobile robotics.

Acknowledgments

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