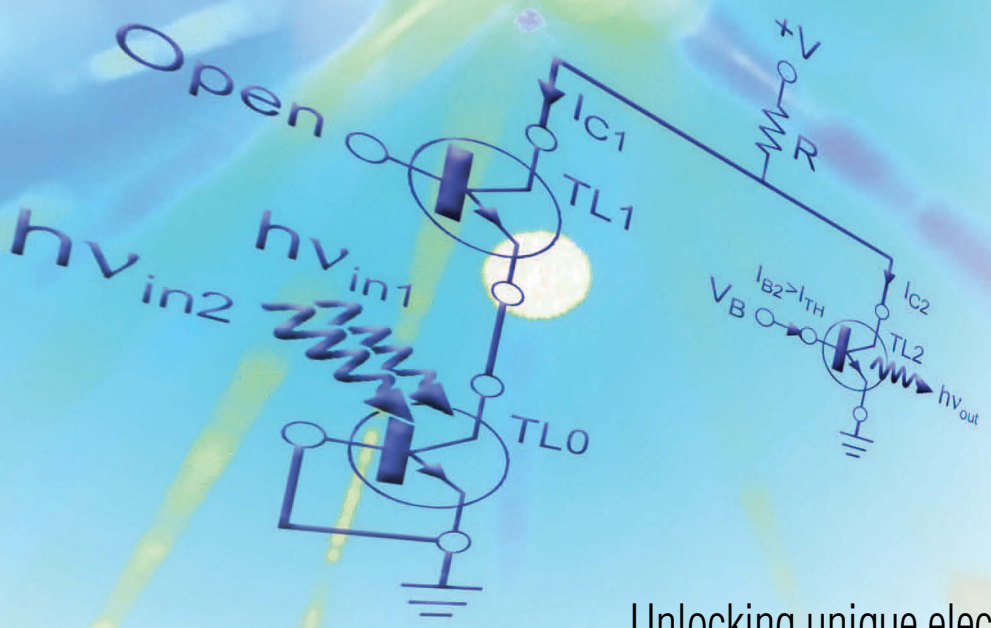
Transistor Laser–Integrated Photonics for Optical Logic



BACKGROUND ©ISTOCKPHOTO/KEMSAB

Unlocking unique electro-optical integration potential to open up new possibilities for logic processors.

THE TRANSISTOR LASER BENEFITS FROM A FAST electron-hole recombination lifetime in the base due to its heterojunction bipolar transistor (HBT)–like operation and can be modulated using the base current or the collector voltage through intracavity photon-assisted tunneling (ICPAT). Both modulation processes are inherently high speed and put the transistor laser at a direct advantage over the diode laser as an optical transmitter. However, the true potential of the technology is the natural coexistence of transistor and laser on the same epitaxial structure, enabling monolithic integration of electrical and optical functions on the same wafer without the need for hybrid methods, such as wafer bonding and regrowth. As such, the transistor laser device structure is the ideal platform for integrated photonics. A transistor laser circuit combined with an optical receiver can process signals without the need for discrete electronic processing and electro-optical conversion components. This unique trait opens the possibility for a transistor laser-based all-optical logic processor, as demonstrated using a transistor laser all-optical NOR gate.

The transistor laser, invented by Feng and Holonyak [1], [2], is based on an n-p-n HBT with a quantum well (QW) inserted in the base along with an optical cavity for the transistor base stimulated recombination process and coherent light output. Unlike a diode laser, which traps carriers in the active region of

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the QW, the transistor laser has a tilted charge distribution because of its HBT-like operation. Carriers that are slow to recombine, instead of waiting in the QW, like in a diode laser, get swept by the electric field toward the collector. Without the carrier pile-up effect, the recombination lifetime of the transistor laser can be reduced to the picosecond range compared to the nanosecond range for the vertical cavity surface-emission laser resulting in a resonance-free frequency response and a high optical modulation bandwidth [3].

With the demand for higher-performance electronic devices, conventional technologies, such as CMOS, face scaling challenges both from intrinsic device scaling [4] and from the scalability of metal interconnects. As the operating frequency of circuits increases, the conventional metal electrical interconnect experiences major problems in terms of loss, crosstalk, and reflections [5]. One solution that has been proposed is the use of on-chip optical interconnects, allowing for minimal crosstalk and loss. So far, optical interconnects have been constrained to the board-to-board or rack-to-rack level in large-scale computing applications, such as high-performance computers and data centers. On-chip optical interconnects have been demonstrated commercially but only in long-haul applications in large-scale photonic integrated circuits (PICs), such as by Infinera [6], [7]. Integrated photonics on a large scale for mainstream applications require a platform that accommodates both active and passive electronic and photonic components.

Compared to transistor integrated circuit (IC) technologies, such as CMOS or BiCMOS, the transistor laser possesses two innate advantages for electro-optical integration. First, unlike a diode laser, the transistor laser light output can be modulated without an external driver, which greatly reduces the complexity of the transmitter circuitry. Second, the epitaxial layer structure readily contains both an optical transmitter as well as a regular transistor because the transistor laser can be operated as a normal HBT. An optical receiver can be implemented using an additional intrinsic layer or using the base–collector junction of the transistor laser. An example of a transistor laser IC is illustrated in Figure 1. Passive elements, such as optical waveguides of thin-film silicon nitride, can also be defined using more advanced techniques to allow for a purely monolithic PIC.

A novel application for transistor lasers beyond electro-optical logic is all-optical logic, which requires either a very efficient on-chip electro-optical conversion method or a device that can process signals purely in optical form. To efficiently realize an all-optical logic processor, an all-optical logic gate is required as a fundamental building block. Previous attempts to realize such a device include logic gates based on optical interference phenomena in waveguides using microring resonators, semiconductor optical amplifiers, electro-absorption modulators, and Mach–Zender modulators [8], [9]. The major disadvantage of these devices is their large size, which limits their integration potential. The second category is semiconductor optical logic gates. A laser-photothyristor implementation [10], [11] has been demonstrated, but it has extremely slow switching speed that is typically in the megahertz range. This fundamental limitation is due to the saturated nature of the p-n-p-n switch, which accumulates large quantities of charge in the base and can take a long time to turn off. Another demonstration is a cascadable laser logic device [12], which uses a diode laser grown on a phototransistor, creating a p-i-n-p-n structure. This device suffers from a very complex layer structure, resulting in extremely complex device fabrication that is not suitable for large-scale integration.

Because of its inherent potential for integrated photonics, the transistor laser has previously been proposed for all-optical logic [3]. In this article, we explore the transistor laser's unique modulation properties that make it a suitable candidate for high levels of integration. An optical logic gate has been designed and fabricated on the existing transistor laser platform as proof of concept for all-optical logic. Finally, we discuss required improvements to push transistor laser-based integrated photonics toward higher levels of integration and performance.

TUNNELING MODULATION OF A TRANSISTOR LASER

The transistor laser's HBT-like operation and tilted base charge distribution allows for a lower recombination lifetime and higher bandwidth over the diode laser. The light output of a transistor laser can be modulated directly using the base current as demonstrated in [13]. Another unique characteristic of the transistor

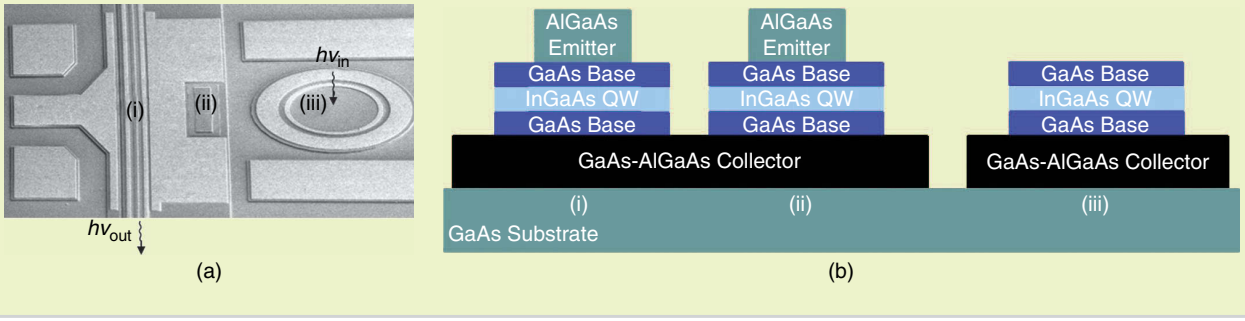


FIGURE 1 The top view (a) and a cross-section diagram (b) of a transistor laser IC containing a transistor laser with (i) an optical cavity and cleaved facets, (ii) an HBT without an optical cavity, and (iii) a vertical p-i-n photodiode.

laser is the dependence of the light output on the base–collector junction reverse bias. This phenomenon gives the transistor laser two distinct advantages. First, it enables pure voltage modulation of the light output, which is not possible in a diode laser. Second, collector voltage modulation potentially holds the key to extending the bandwidth of the transistor laser even more because it is based on a very fast tunneling process.

To understand the mechanism behind the tunneling modulation of a transistor laser, it is helpful to consider the excess carrier distribution in its base, as illustrated in Figure 2 [14]. Electron injection from the emitter forms the emitter current I_{En} with a triangular tilted charge distribution Δn_1 and Δp_1 due to the boundary condition set by the base QW and the base–collector junction. Electrons that recombine inside the base form the primary base recombination current I_{r1}, and electrons that diffuse to the base–collector junction will then drift toward the collector and form the primary base transport current I_{t1}. Meanwhile, electrons in the base tunnel toward the collector assisted by photons inside the cavity, called ICPAT. The tunneling electrons form the tunneling current I_{ICPAT} and leave an excess hole concentration Δp_2 in the base. The charge is compensated by the electron concentration Δn_2 through dielectric relaxation with an approximated time constant of 4.9 fs. The diffusion of Δn_2 near the base–collector junction forms the secondary base transport current I_{t2}, and diffusion near the QW forms the secondary stimulated base recombination current I_{r2}.

A typical *L-I-V* curve for a transistor laser with ICPAT is shown in Figure 3. When the device is biased with I_B above the lasing threshold, high collector–emitter bias voltage leads to increased tunneling probability, resulting in reduced light output with simultaneously increased collector current. This direct voltage dependence, along with the conventional base current modulation of the transistor laser, adds a degree of freedom in the design of an electro-optical or all-optical IC. Moreover, the nonparasitic limit of the

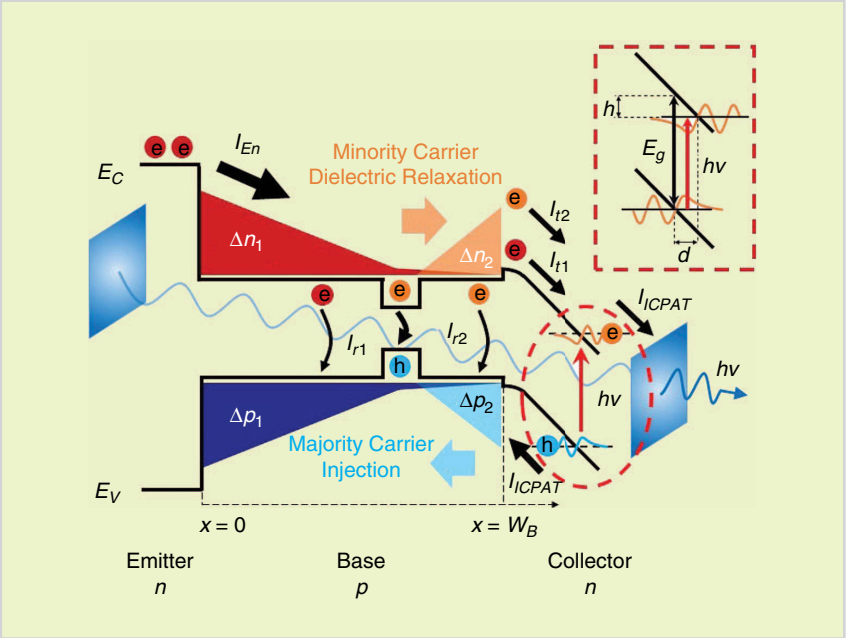


FIGURE 2 The excess carrier distribution in the base of a transistor laser with ICPAT [14]. Electrons tunneling from the cavity toward the collector form a tunneling current I_{ICPAT}, which increases with stronger base–collector junction reverse bias. As a result of the tunneling electrons, a hole concentration Δp_2 accumulates in the base and must be compensated by an electron concentration Δn_2 through dielectric relaxation. Diffusion of electrons in Δn_2 toward the junction forms an additional base transport current I_{t2}. The tunneling process reduces the total light output, and the additional current components result in increased electrical gain.

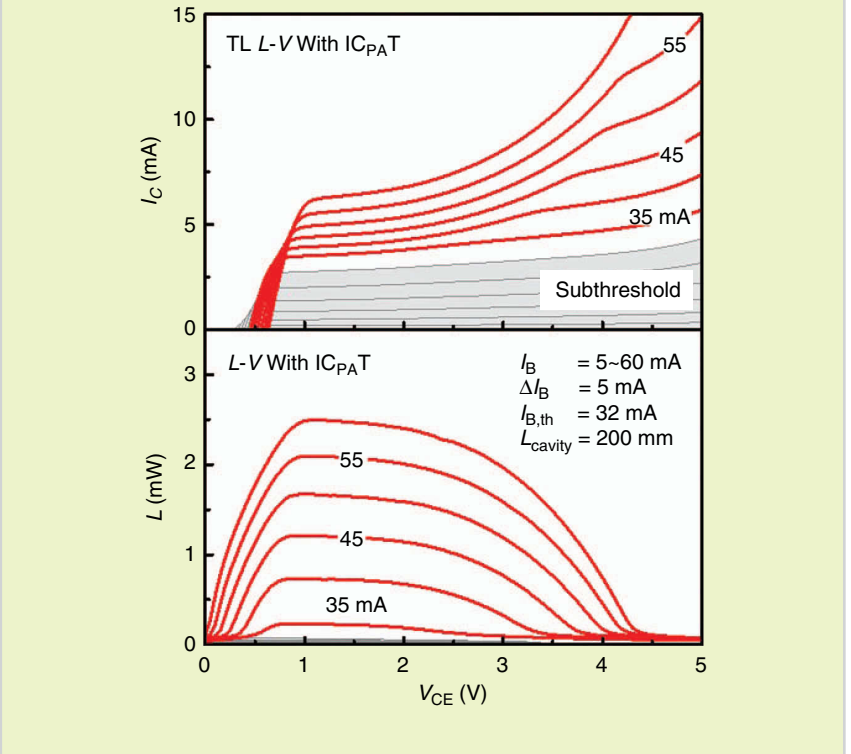
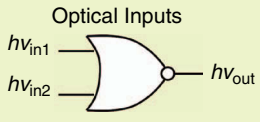


FIGURE 3 Typical *L-I-V* curves of a transistor laser with ICPAT. Above threshold, the transistor laser shows reduced light output and increased collector current at high collector bias.

collector voltage modulation is dictated by the tunneling process and dielectric relaxation, both faster than the recombination lifetime limit of the base current modulation. To date, collector modulation has shown simultaneous electrical and optical output at 20 and 40 Gb/s [15]. In this article, collector voltage modulation using ICPAT is used as the main switching method for an all-optical logic gate.

TRANSISTOR LASER ALL-OPTICAL NOR GATE

As a proof of concept for transistor laser integrated photonics, a NOR gate has been selected. The block diagram and logic table for the all-optical NOR gate is shown in Figure 4. Because it is a universal logic gate, the NOR gate can act as a very simple building block for more advanced logic circuits.



hv_{in1}	hv_{in2}	hv_{out}
0	0	1
1	0	0
0	1	0
1	1	0

FIGURE 4 A block diagram and logic table for a two-input all-optical NOR gate.

DESIGN AND THEORY OF OPERATION

The circuit implementation of the all-optical NOR gate is shown in Figure 5, as previously proposed in [16]. The circuit consists of three transistor lasers (TLs) divided into two branches, sharing a constant voltage supply V and resistor R. The right branch contains TL2, which acts as a normal transistor laser biased at a fixed base–emitter voltage and a collector current I_{C2}. When the base current exceeds the lasing threshold, the output of TL2 will be on. The left branch provides the control structure to regulate the right branch collector current I_{C2}. TL0 acts as a photodiode with its collector tied to the emitter of TL1, which acts as an active load. The functionality of the all-optical NOR gate is explained as follows. In a logic 1 case, no optical input is applied to TL0. This causes no current to conduct on the left branch ($I_{C1} = 0$), and the right branch operates as a conventionally biased transistor laser. In a logic 0 case, a nominal optical input is applied to TL0. The resulting photocurrent sets the collector current I_{C1} of the left branch, inducing a nonzero collector–emitter voltage on TL1. The induced voltage causes the total voltage on the combined node to rise, increasing the collector–emitter bias of TL2. The operating point of TL2 will shift along the load line set by the supply voltage V and the load resistor R, causing the light output from TL2 to vanish.

The operation of the all-optical NOR gate is simulated in Keysight advanced design system using a black box model of a previously reported edge-emitting transistor laser with a 200-μm cavity width [17] that describes the electron-photon interaction inside the laser cavity. A nominal photocurrent of 0.1 mA is assumed to be generated by each individual light source hv_{in1} and hv_{in2}. The photodiode capacitance is assumed to be 100 fF, and the load resistor is set to 50 Ω. Figure 6 shows the simulated timing diagram for a two-input optical NOR gate at 1 Gb/s. It should be noted that the optical NOR gate design can theoretically function with more than two inputs since each additional input only serves to increase the collector–emitter voltage of the output transistor laser and further diminish the light output. However, as seen in the output plot in Figure 6, the logic 0 threshold must be set at the output level corresponding to a single active input for the gate to function properly.

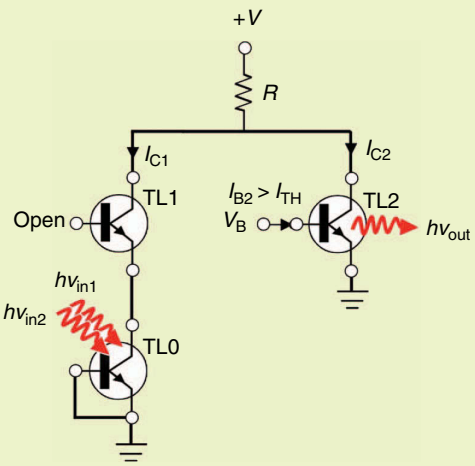


FIGURE 5 A circuit diagram for the transistor laser all-optical NOR gate. TL2 acts as a regular transistor, TL1 acts as an active load, and TL0 acts as a photodiode. TL2 is biased as a regular transistor laser with I_{B2} above threshold to maintain an on state when no light is incident on TL0. In an off state, the photocurrent I_{C1} generated by an optical input induces a voltage drop on TL1, increasing the shared collector node voltage for TL1 and TL2. The increase in base–collector junction bias of TL2 results in more electrons tunneling toward the collector, increasing the collector current and decreasing the light output.

FABRICATION PROCESS

The material and fabrication process for the all-optical NOR gate is similar to previous transistor laser work [15]. The epitaxial wafer is grown using metal-organic chemical vapor deposition on a semi-insulating GaAs substrate. It contains a high-bandgap n-type AlGaAs emitter and a p-type GaAs base. The base contains an InGaAs QW that acts as a carrier trap for the radiative recombination process. The collector is low-doped n-type GaAs followed by a highly doped n-GaAs subcollector on which the collector contacts are placed. Under the subcollector is an AlGaAs optical confinement layer to constrain the optical field between the emitter and collector.

The device layout and cross-section diagrams for the all-optical NOR gate is shown in Figure 7. TL2 is a regular transistor laser with a 5 × 400–μm optical cavity to maximize gain and with its collector pad shared with TL1. TL1 is an HBT without an optical cavity in a floating base configuration to act as an active load. TL0 is implemented as a p-i-n photodiode at the base–collector junction of the transistor laser. The n-contact of the TL0 photodiode is connected to the emitter of TL1. To establish the metal interconnects, the device is fabricated using a two-step planarization using benzocyclobutane and subsequent dry-etching processes to define double vias. After processing, the wafer is thinned down to 150 μm and cleaved into bars to form edge-emitting facets. Each individual bar is then indium bonded to a copper block for testing.

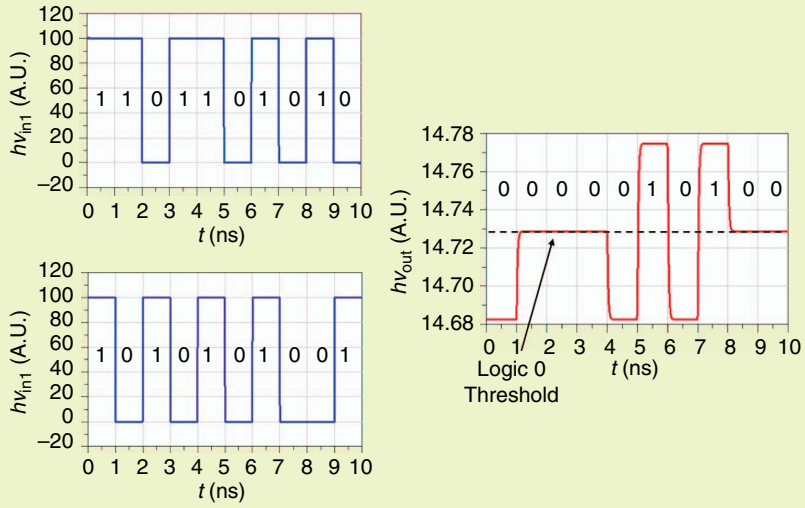


FIGURE 6 A simulated logic diagram for a two-input optical NOR gate at 1 Gb/s.

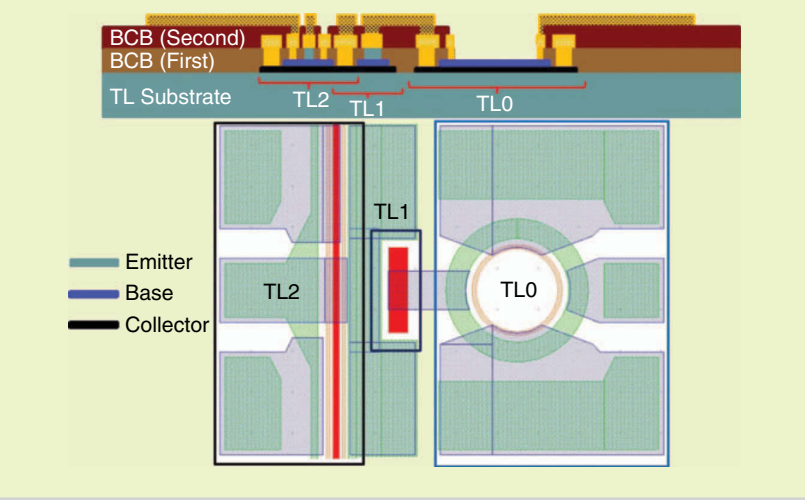


FIGURE 7 Lateral cross-section and top view diagrams of the transistor laser all-optical NOR gate.

CHARACTERIZATION

The finished devices are measured on a dc station equipped with a modular laser source and a photodetector. The testing configuration is shown in Figure 8. The base current bias is provided using a coplanar ground-signal-ground probe. The collector is biased using a dc probe in series with a variable load resistor to define the load line of TL2. A second dc probe grounds the n contacts of the TL0 photodiode and the modular laser source provides the input optical signal to TL0 via a fiber probe. Finally, the light output from the facet is free-space coupled to the optical fiber into a photodiode.

Before testing the logic functionality, the individual components of the NOR gate are characterized. The responsivity of the TL0 photodiode is measured using an 850-nm oxide-confined VCSEL similar to [18] (see Figure 9). The average responsivity of the photodiode is 0.0346 A/W. The low responsivity is caused by limited light absorption in the base–collector junction of the transistor laser material, which only contains 60 nm of depleted GaAs.

The family *L-I-V* curves of the output transistor laser TL2 biased at a maximum base current of 50 mA (ΔI_B = 5 mA) is shown in Figure 10. The collector current exhibits relatively large electrical gain compared to a typical

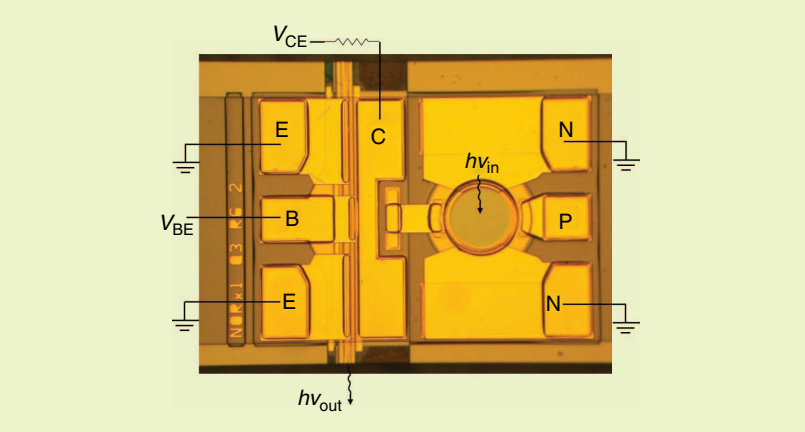


FIGURE 8 The testing configuration for the transistor laser all-optical NOR gate.

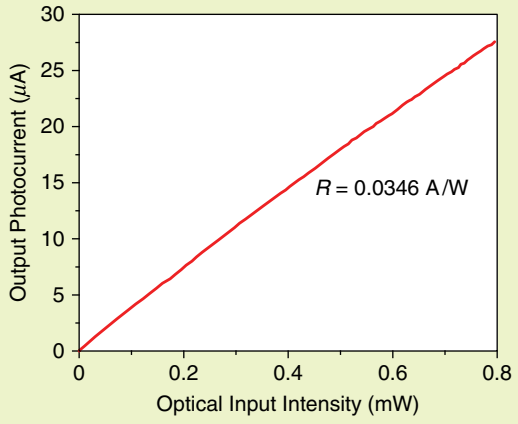


FIGURE 9 The responsivity of the TL0 photodiode measured using an 850-nm VCSEL.

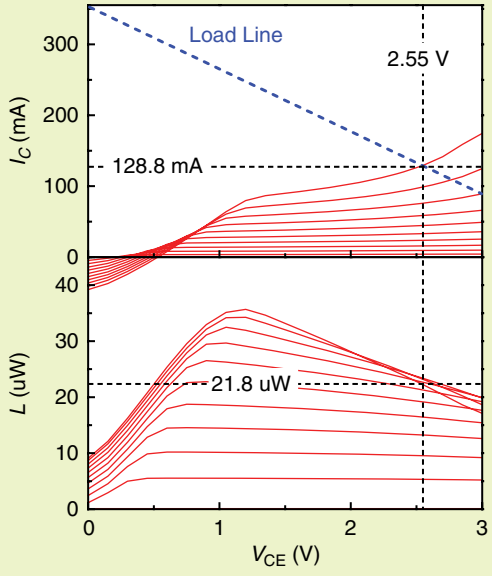


FIGURE 10 Family *L-I-V* curves of the output transistor laser TL2 showing spontaneous light emission. The blue line indicates the load line set by the voltage supply (V = 4 V) and the load resistor (R = 11.3 Ω).

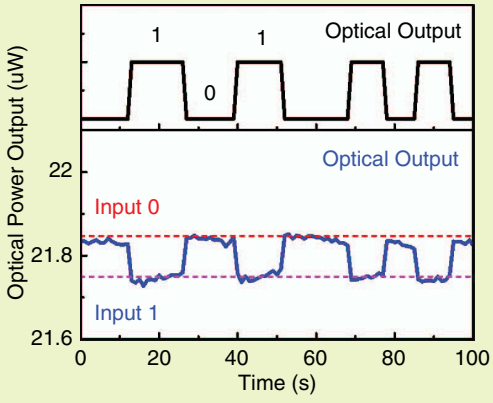


FIGURE 11 A logic timing diagram for the optical NOR gate. The input signal comes from a modular laser coupled through a fiber probe. The logic 1 threshold is 21.85 μW, and the logic 0 threshold is 21.75 μW.

transistor laser without showing gain compression, which signals the transition from spontaneous to stimulated light emission. The measured light output of the transistor laser is very weak because of the spontaneous nature of the light emission, similar to a light-emitting transistor. It is suspected that the transistor laser suffers from a prohibitively high lasing threshold caused by poor heat conduction or added resistance from the double via process. Because the structure of the transistor laser is designed for light collection from the cleaved facet, only a very small amount of light can be collected using the free-space coupling method.

The logic function of the all-optical NOR gate is characterized as follows. First, TL2 is biased at a base current of 50 mA to maximize optical output. The voltage supply is set at 4 V with a load resistor R of 11.3 Ω, yielding a TL2 collector–emitter voltage of 2.3 V, which correctly places TL2 in the tunneling modulation region. Simultaneously, the modular laser is coupled to the TL0 aperture and is switched on and off to provide a square wave input optical signal. The generated photocurrent shifts the operation of TL2 along the load line as indicated by the blue line in Figure 10. Note that in this case, the NOR gate acts as an inverter, but testing for the NOR functionality can be done by coupling two different light sources into the fiber or by using a multilevel input signal. The optical logic timing diagram for the optical NOR gate is shown in Figure 11. It shows a logic 1 threshold of 21.85 μW and a logic 0 threshold of 21.75 μW.

DEVICE SCALING AND FUTURE WORK

The demonstrated all-optical NOR gate is the first step toward transistor laser integrated photonics. Currently, the demonstrated device is limited in high-speed performance dye to the parasitics of the large transistor laser device as well as resistance–capacitance loading from the large-area vertical photodetector. However, the unique transistor operation and tunneling modulation properties are not limited by the size of the device and should be well suited to aggressive scaling as long as the system

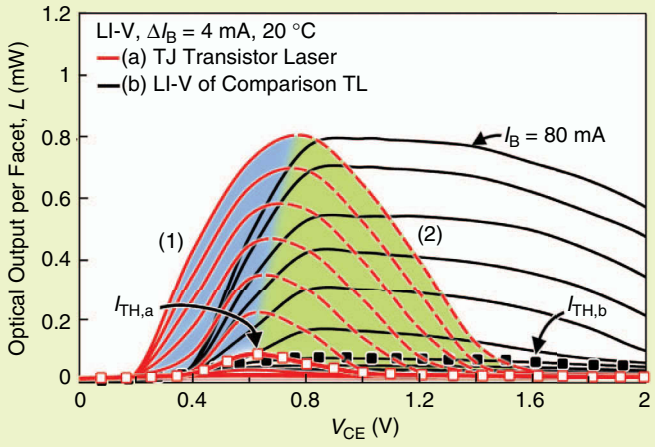


FIGURE 12 *L-V* curves of a TJTL (red) and a regular transistor laser [19]. The tunnel junction enhances ICPAT in the base–collector junction. This results in stronger collector voltage modulation, and a smaller voltage swing is required to completely turn off the transistor laser output.

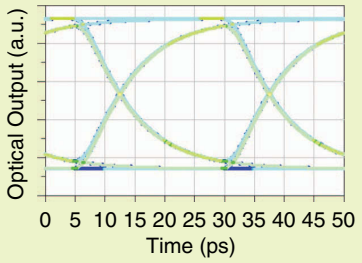


FIGURE 13 A simulated eye diagram for an optical NOR gate at 40 Gb/s operation assuming a junction capacitance of 200 fF, 1-mA photodiode current, 100-fF photodiode capacitance, 5-Ω load resistance, and 2-V supply voltage.

can provide enough gain to sustain stimulated emission. Since tunneling modulation is an inherently fast process with terahertz-range bandwidth, a transistor laser-based device with well-controlled parasitic elements is a great candidate for future high-performance electro-optical applications.

To achieve a higher level of integration, several modifications can be made to the existing transistor laser technology. On the epitaxial side, incorporating a highly doped collector layer to achieve a sharper base–collector junction enhances ICPAT resulting in a tunnel junction [19]. In a tunnel junction TL (TJTL), light output dependence on the collector voltage is greatly increased. Figure 12 compares typical *L-V* curves of a regular transistor laser and a TJTL. Optical switching in a TJTL requires a lower voltage swing, allowing for a higher signal-to-noise ratio and lower power consumption, and it enables smaller device dimensions to reduce parasitics for high-speed performance. The addition of a larger dedicated intrinsic or low-doped layer can also help to define better photodiode or waveguide structures. Finally, optical facet definition by dry etching instead of cleaving can allow for monolithic optical transmit–receive operations.

Using the same model as in the section "Transistor Laser All-Optical NOR Gate," simulations were done to predict the potential performance of a transistor laser-based optical logic gate when it is not hindered by excessive parasitics. The simulation assumes a 5 µm × 200 µm transistor laser with a junction capacitance of 200 fF and a reduced load resistance of 5 Ω. The photodiode capacitance is limited to 100 fF with an assumed photocurrent of 1 mA. On the basis of these parameters, the power consumption is estimated to be 26.6 mW. Figure 13 shows an eye diagram of the gate simulated at 40 Gb/s. Using the same parameters, different logic gate configurations were simulated using both base current and collector voltage modulation, as shown in Table 1.

Because the NOR gate is a universal logic gate, more complicated logic circuits can be constructed using the current design. One such example is the optical bistable latch [16] shown in Figure 14. The optical bistable latch consists of two cross-coupled NOR gates with the corresponding logic function described in Table 2. The bistable latch is a basic optical in, optical out memory device, which provides complementary optical outputs that are preserved whenever both optical inputs are off.

CONCLUSION

ICPAT-based collector voltage modulation of the transistor laser provides the ideal switching mechanism to enable a transistor laser all-optical logic gate. Using this scheme, an all-optical NOR gate has been fabricated and characterized. The logic functionality of the device has been demonstrated in the case of a single optical input, acting as an inverter. NOR functionality can be achieved using a different optical input, so the device can act as a logic processing building block in more complex devices, such as the optical bistable latch. This work is the first instance of a transistor laser-based IC and the first all-optical logic gate using the transistor laser platform. With device scaling and

TABLE 1 **A simulated performance of transistor laser-based all-optical logic gates at 40 Gb/s with different configurations and modulation schemes.**

	INVERTER	NAND	AND	OR/NOR
Delay (ps)	14.5	14.5	3.5	3.5
Rise/fall time (ps)	14.2/14.5	14.2/14.5	7.6/7.7	7.6/7.7
Jitter root mean square (ps)	0.14	0.14	0.02	0.02
Data rate (Gb/s)	40			
Power consumption (mW)	16.8	16.8	26.6	26.6
Modulation method	Base		Collector	

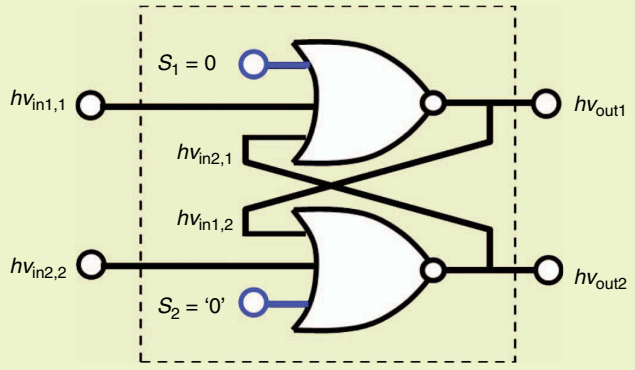


FIGURE 14 An optical bistable latch constructed using two cross-coupled optical NOR gates. The latch is as a basic optical in, optical out memory device.

TABLE 2 **A logic table for the optical bistable latch. The bistable latch preserves its output whenever both inputs are a logic 0.**

$hv_{in1,1}$	$hv_{in2,2}$	hv_{out1}	hv_{out2}
0	0	No change	No change
0	1	0	1
1	0	1	0
1	1	Forbidden	Forbidden

addition of passive components to the transistor laser process suite, a transistor laser-based optical logic processor with a higher degree of functionality can be realized.

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