# Natural Balancing of Flying Capacitor Multilevel Converters at Nominal Conversion Ratios

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***Abstract*—This work explores the mechanisms and limitations of natural voltage balancing in flying capacitor multilevel (FCML) DC-DC converters. A simple discrete-time state space model is used to explore the fundamental conditions that will lead to (or prevent) natural balance of flying capacitor voltages, along with the balancing dynamics. The treatment is used to highlight straightforward ways to alleviate problems with natural imbalance by adjusting the switching scheme. The model is compared against circuit simulations and the proposed switching scheme is verified in a hardware prototype.**

***Index Terms*—flying capacitor multilevel, DC-DC converter, state space model, natural balancing**

## I. Introduction

Flying capacitor multilevel (FCML) DC-DC converters have gained interest in recent years due to a number of favorable characteristics. The FCML architecture leverages a switched capacitor network to generate a multilevel, stepped-down voltage waveform which can reduce the energy-storage requirements and therefore overall volume of the inductor [1], [2]. The FCML circuit also multiplies the effective switching frequency seen by the inductor, significantly improving trade-offs among voltage ripple, size, and efficiency. However, the issue of maintaining voltage balance on the flying capacitors remains challenging.

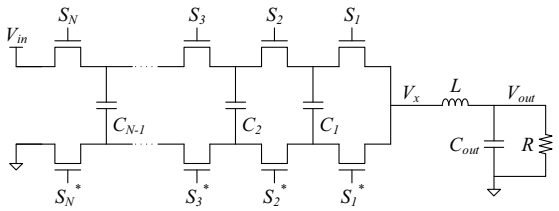


Fig. 1. General $N+1$ level FCML converter.

An $N$+1 level FCML converter consists of $N$ pairs of switches and $N$-1 flying capacitors, as shown in Fig. 1. Flying capacitor $C_i$ ($i = 1, 2, \ldots, N$-1) should ideally operate with a balanced voltage of $i \cdot V_{in}/N$, however, the actual voltage can deviate from its balanced value. Voltage imbalance causes increased current ripple in the inductor and higher voltage stress on switches, and is a major factor that limits the application of this topology. The conversion ratio of an $N$+1 level FCML converter can be expressed as $m/N$, where $m$ is a real number bounded by 0 and $N$. Cases where $m$ is an integer will herein be referred to as nominal conversion ratios. Past work has shown that an inherent mechanism, natural balancing, keeps the capacitor voltages at their balanced values, but it fails to function at certain nominal conversion ratios, specifically when $m$ and $N$ share a common divisor greater than one (they are not co-prime) [3]. While various control techniques have been reported to deal with capacitor voltage imbalance caused by nonidealities [4]–[7], few works have explored solutions to natural imbalance at nominal conversion ratios where $m$ and $N$ are not co-prime. Furthermore, [8] showed that under phase-shifted pulse width modulation (PSPWM) operation, in any naturally imbalanced case, flying capacitor voltages cannot be regulated by tuning the gate drive timing: they are neither controllable nor observable. This implies that a new switching scheme is necessary to solve the natural imbalance problem of FCML converters.

In this work, we will expand the state space model proposed in [8] to investigate the mechanism of natural balancing. It will be shown that the inductive impedance at the output provides inherent feedback, similar to an integral controller, that regulates the voltage levels of the flying capacitors to their balanced values. Intuitively, natural balancing does not work when the switched capacitor stage is not controllable. We will also propose a new switching scheme, modified PSPWM, that makes FCML converters naturally balanced at any conversion ratio. The new scheme is verified by a hardware prototype.

## II. Discrete-Time State-Space Model

A discrete-time state-space model for FCML converters was developed in [8] and led to the state equation:

$$\boldsymbol{V_C}(k+1) = \boldsymbol{A}\boldsymbol{V_C}(k) + \boldsymbol{B}\boldsymbol{q}(k), \tag{1}$$

where $\boldsymbol{V_C}$ is the state vector, containing individual flying capacitor voltages; $\boldsymbol{q}$ is the input vector, containing charge transferred through the inductor in each phase; $k$ represents the period index. It describes the dynamics of flying capacitor voltages assuming arbitrary charge transfer through the inductor. Importantly, [8] described conditions for controllability and observability of the flying capacitor voltage states. Specifically, flying capacitor voltages were shown to be observable (their

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voltages can be estimated from measurements of the switching node voltage, $V_x$) and controllable (their voltages can be regulated arbitrarily by adjusting inductor charge flow via PSPWM timing) only if the matrix $\boldsymbol{B}$ in (1) is full-rank.

In the treatment that follows here, the relationships between controllability, observability and natural balancing will be further investigated. Consider an FCML converter already under balanced operation, then an instantaneous disturbance is applied to flying capacitor voltages. According to the superposition theorem of linear circuits, the overall response equals the sum of responses caused by individual excitations. Therefore, the dynamics of the converter can be decomposed into two parts: the balanced dynamics and the disturbance dynamics. Take the voltage on capacitor $C_1$ as an example:

$$V_{C1} = V_{C1,balanced} + \Delta V_{C1}, \tag{2}$$

where $V_{C1,balanced}$ represents the dynamics of $V_{C1}$ under ideally balanced operation; $\Delta V_{C1}$ represents the dynamics of $V_{C1}$ when only excited by the disturbance. This treatment applies to other electrical quantities as well. The disturbance dynamics of inductor current, $\Delta I_L$, is defined as the portion of inductor current that is excited only by the disturbance, and it obeys the same superposition rule:

$$I_L = I_{L,balanced} + \Delta I_L. \tag{3}$$

In our analysis, charge flow (integral of current) is important as it directly impact capacitor voltage change. Since integral is a linear operator, superposition still holds:

$$q = q_{balanced} + \Delta q. \tag{4}$$

This consideration provides significant simplification as it isolates the effect of the disturbance from large-signal dynamics of the converter, and it is sufficient to determine whether the convreter is naturally balanced: if the deviation dynamics approach zero in steady state (the effect of the disturbance decays), the converter is naturally balanced; if the deviation dynamics have a non-zero steady state (the effect of the disturbance persists), the converter is subject to imbalance.

Going forward, the model will be derived for a 5-level FCML converter at a conversion ratio of 2/4, but the method is general and applies to any level and nominal conversion ratio. Shown in Fig. 2, the switched capacitor stage and the inductor stage are treated as two subsystems. The switching node voltage, $\Delta V_x$, is the switched capacitor system output and the inductor system input. Similarly, the charge transferred through the inductor, $\Delta q$, is the inductor system output and the switched capacitor system input.

### A. Switched Capacitor Model

A common way to operate FCML converters is phase shifted pulse width modulation (PSPWM): all top switches share the same duty cycle, and each bottom switch is complementary with its top counterpart. For an $N$+1 level FCML converter ($N = 4$ in this example), there is a delay of $T/N$ between two adjacent switches, where $T$ is the switching period. As a result, at nominal conversion ratios, each period splits into

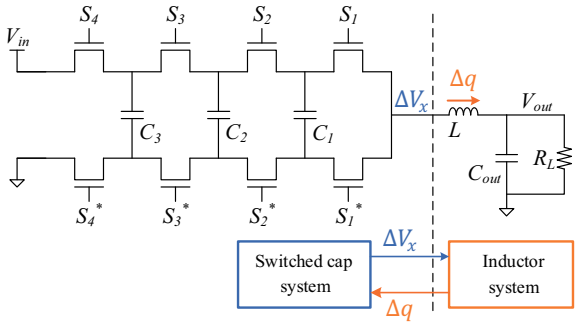


Fig. 2. FCML converter modeled as a closed-loop system.

$N$ phases, in which the flying capacitors are connected in different configurations between the switching node and the power supply (or ground).

For the switched capacitor system, the state variables are defined as initial flying capacitor voltages in each period, $[\Delta V_{C1}, \Delta V_{C2}, \Delta V_{C3}]^T$. As mentioned previously, we are treating their deviation from the balanced dynamics. At 2/4 conversion ratio, the equivalent circuits in each phase are shown in Fig. 3 to highlight capacitor connections. Quantity $\Delta V_{xj}$ and $\Delta q_j$ represent the initial switching node voltage and the charge transferred to the switching node (which is the same as charge transferred through the inductor) in phase $j$ ($j = 1, 2, 3, 4$), respectively.

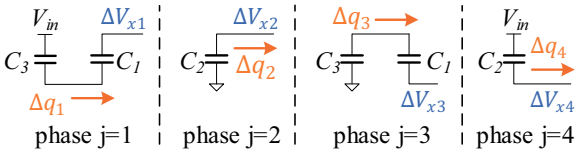


Fig. 3. Flying capacitor connections in each period.

Take flying capacitor $C_1$ as an example: it is charged in phase 3 and discharged in phase 1. Therefore, its charge increases by $\Delta q_3 - \Delta q_1$ in one period. To keep equations brief and clear, we will assume that all flying capacitors have the same capacitance, $C_{fly}$; violation of this assumption does not affect the conclusions. The change of $\Delta V_{C1}$ from period $k$ to period $k$+1 can be expressed as:

$$\Delta V_{C1}(k+1) - \Delta V_{C1}(k) = \frac{\Delta q_3(k) - \Delta q_1(k)}{C_{fly}}. \tag{5}$$

Similar expressions can also be derived for $C_2$ and $C_3$ by analyzing their charging and discharging phases. Combining them into matrix form yields the state equation of the system:

$$\begin{bmatrix} \Delta V_{C1}(k+1) \\ \Delta V_{C2}(k+1) \\ \Delta V_{C3}(k+1) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \Delta V_{C1}(k) \\ \Delta V_{C2}(k) \\ \Delta V_{C3}(k) \end{bmatrix} + \frac{1}{C_{fly}} \begin{bmatrix} -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & -1 \\ 1 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} \Delta q_1(k) \\ \Delta q_2(k) \\ \Delta q_3(k) \\ \Delta q_4(k) \end{bmatrix}, \tag{6}$$

or denoted as

$$\Delta \boldsymbol{V_C}(k+1) = \boldsymbol{A}\Delta \boldsymbol{V_C}(k) + \boldsymbol{B}\Delta \boldsymbol{q}(k), \tag{7}$$

where $\Delta \boldsymbol{V_C}$ is the state vector; $\Delta \boldsymbol{q}$ is the input vector; $\boldsymbol{A}$ equals the identity matrix; $\boldsymbol{B}$ is defined as *charge transfer matrix* and is only dependent on capacitor connections and the value of $C_{fly}$.

Fig. 3 also implies that in each phase, the switching node voltage is a linear combination of flying capacitor voltages. For example, in phase 1 of period $k$, KVL gives

$$\Delta V_{x1}(k) = \Delta V_{in}(k) - \Delta V_{C3}(k) + \Delta V_{C1}(k). \tag{8}$$

With constant input voltage, $V_{in}$ (treatment of input impedance will be explained in section III), its disturbance dynamics, $\Delta V_{in}$, is always zero. Hence, (8) simplifies to:

$$\Delta V_{x1}(k) = -\Delta V_{C3}(k) + \Delta V_{C1}(k). \tag{9}$$

However, this relationship can be slightly more complex in some other phases. For example, at the beginning of phase 3, capacitor $C_1$ has a voltage of $\Delta V_{C1} - \Delta q_1/C_{fly}$ (since it is already discharged in phase 1), and $C_3$ has a voltage of $\Delta V_{C3} + \Delta q_1/C_{fly}$. Consequently, the initial switching node voltage can be expressed as

$$\begin{aligned}
&\Delta V_{x3}(k) \\
&= (\Delta V_{C3}(k) + \Delta q_1(k)/C_{fly}) - (\Delta V_{C1}(k) - \Delta q_1(k)/C_{fly}) \\
&= \Delta V_{C3}(k) - \Delta V_{C1}(k) + 2\Delta q_1(k)/C_{fly}.
\end{aligned} \tag{10}$$

The relationships in other phases can be obtained in similar ways. They are wrapped into a matrix expression to form the output equation of the system:

$$\begin{aligned}
\begin{bmatrix} \Delta V_{x1}(k) \\ \Delta V_{x2}(k) \\ \Delta V_{x3}(k) \\ \Delta V_{x4}(k) \end{bmatrix} &= \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} \Delta V_{C1}(k) \\ \Delta V_{C2}(k) \\ \Delta V_{C3}(k) \end{bmatrix} \\
&+ \frac{1}{C_{fly}} \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 2 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta q_1(k) \\ \Delta q_2(k) \\ \Delta q_3(k) \\ \Delta q_4(k) \end{bmatrix},
\end{aligned} \tag{11}$$

or denoted as

$$\Delta \boldsymbol{V_x}(k) = \boldsymbol{C}\Delta \boldsymbol{V_C}(k) + \boldsymbol{D}\Delta \boldsymbol{q}(k), \tag{12}$$

where $\Delta \boldsymbol{V_x}$ is the output vector; $\boldsymbol{C}$ and $\boldsymbol{D}$ are determined by capacitor connections.

Equations (7) and (12) form the state space model of the switched capacitor subsystem shown in Fig. 2. It defines the system input-output relationship, along with the dynamics of state variables.

### *B. Inductor Model*

In the closed-loop system shown in Fig. 2, the inductor is treated as a subsystem that provides input signals to the switched capacitor stage. When exploring the inductor system, the phase index is slightly adjusted for convenience of derivation: phases 1-4 in the first period remain unchanged, the 4 phases in the second period now occupy the indexes 5-8, and so on. The state variable of the inductor system is defined as the initial inductor current of each phase, $\Delta I_L$. Assuming that the output voltage ripple is negligible, $V_{out}$ is constant and therefore $\Delta V_{out}$ is always zero. Fig. 4 shows the equivalent circuit of the inductor system, where $C_{eq}$ is the equivalent capacitance of flying capacitors, and $R_{esr}$ captures the parasitic resistance of switches and the inductor.

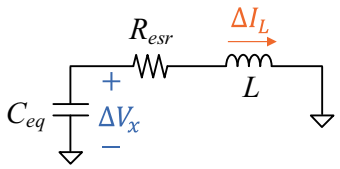


Fig. 4. Equivalent circuit of the inductor system in each phase.

During phase $n$, the inductor system is a second-order circuit with initial capacitor voltage $\Delta V_x(n)$ and initial inductor current $\Delta I_L(n)$. The transient response of inductor current in that phase is a linear combination of both initial conditions, which leads to the time-domain expression:

$$\Delta I_L(t) = f(t)\Delta I_L(n) + g(t)\Delta V_x(n), \tag{13}$$

where $f(t)$ and $g(t)$ are time-dependent coefficients obtained by solving the equivalent circuit. For their exact expressions, please refer to the appendix.

Because the inductor current is continuous across the phase transitions, the final inductor current in phase $n$ must be equal to the initial inductor current in phase $n$+1. By denoting the phase duration as $t_0$, the state equation of the inductor system can be expressed as:

$$\Delta I_L(n+1) = \Delta I_L(t)\big|_{t=t_0} = f\Delta I_L(n) + g\Delta V_x(n), \tag{14}$$

where $f$ and $g$ are abbreviations of $f(t_0)$ and $g(t_0)$ respectively. The charge transferred through the inductor during phase $n$, which is the system output, equals $\Delta I_L(t)$ integrated from $t = 0$ to $t = t_0$:

$$\begin{aligned}
\Delta q(n) &= \int_0^{t_0} \Delta I_L(t)dt \\
&= \int_0^{t_0} f(t)dt\Delta I_L(n) + \int_0^{t_0} g(t)dt\Delta V_x(n),
\end{aligned} \tag{15}$$

or denoted as

$$\Delta q(n) = F\Delta I_L(n) + G\Delta V_x(n), \tag{16}$$

where $F$ and $G$ represent the definite integrals (which are scalars) that they replace; their exact expressions are also listed in the appendix.

Equations (14) and (16) are the inductor state space model, with a time step of one phase. However, the time step of the switched capacitor model is one period. To bridge the gap, the inductor system input and output are packed into groups of 4 to form the corresponding vectors, and the state variable is accordingly redefined as the initial inductor current

of each period, which yields the unified state-space model of the inductor system:

$$\Delta I_L(k+1) = f^4 \Delta I_L(k) + g\begin{bmatrix} f^3 & f^2 & f & 1 \end{bmatrix}\begin{bmatrix} \Delta V_{x1}(k) \\ \Delta V_{x2}(k) \\ \Delta V_{x3}(k) \\ \Delta V_{x4}(k) \end{bmatrix}; \quad (17)$$

$$\begin{bmatrix} \Delta q_1(k) \\ \Delta q_2(k) \\ \Delta q_3(k) \\ \Delta q_4(k) \end{bmatrix} = F\begin{bmatrix} 1 \\ f \\ f^2 \\ f^3 \end{bmatrix}\Delta I_L(k) + \begin{bmatrix} G & 0 & 0 & 0 \\ Fg & G & 0 & 0 \\ Ffg & Fg & G & 0 \\ Ff^2g & Ffg & Fg & G \end{bmatrix}\begin{bmatrix} \Delta V_{x1}(k) \\ \Delta V_{x2}(k) \\ \Delta V_{x3}(k) \\ \Delta V_{x4}(k) \end{bmatrix}, \quad (18)$$

or denoted as:

$$\Delta I_L(k+1) = P\Delta I_L(k) + \boldsymbol{Q}\Delta \boldsymbol{V_x}(k); \quad (19)$$

$$\Delta \boldsymbol{q}(k) = \boldsymbol{R}\Delta I_L(k) + \boldsymbol{S}\Delta \boldsymbol{V_x}(k), \quad (20)$$

where the bold symbols represent the matrices (along with their coefficients) that they are replacing. Equations (19) and (20) form the state space model of the inductor subsystem shown in Fig. 2.

## III. Discussion on Natural Balancing

Balancing of an FCML converter requires all flying capacitors to have balanced voltages in steady state. Balanced operation is a valid state of the converter, but not necessarily a stable state: it depends on whether the converter is capable of compensating for disturbances around the balanced point [9]. We will analyze the effect of disturbances to explore the stability of flying capacitor voltages.

### A. Open-Loop Analysis

Assume that the 5-level FCML converter shown in Fig. 2 is originally under balanced operation. At the initial period ($k = 0$), a disturbance, $[\Delta V_{C1}(0), \Delta V_{C2}(0), \Delta V_{C3}(0)]^T$, is introduced as an initial condition. If the steady state returns to zeros, $[\Delta V_{C1}(\infty), \Delta V_{C2}(\infty), \Delta V_{C3}(\infty)]^T = [0,0,0]^T$, the balanced operation is a stable state, and the converter is naturally balanced; if the disturbance results in a non-zero steady state, the converter is not naturally balanced.

At $2/4$ conversion ratio, (6) describes the change of states over time. Adding $\Delta V_{C1}$ and $\Delta V_{C3}$ together reveals an interesting relationship:

$$\Delta V_{C1}(k+1) + \Delta V_{C3}(k+1) = \Delta V_{C1}(k) + \Delta V_{C3}(k). \quad (21)$$

Performing this expression recursively yields

$$\Delta V_{C1}(\infty) + \Delta V_{C3}(\infty) = \Delta V_{C1}(0) + \Delta V_{C3}(0), \quad (22)$$

which already indicates that $2/4$ is an imbalanced conversion ratio: if $\Delta V_{C1}(0) + \Delta V_{C3}(0) \neq 0$, at least one of their steady states will be non-zero. In other words, the steady state depends on the perturbation. This dependency directly results from the fact that the charge transfer matrix, $\boldsymbol{B}$ in (7), contains linearly dependent row vectors (it is not full-rank), so that the input effect cancels out among a subset of the flying capacitors ($C_1$ and $C_3$ in this example). Therefore, the feedback, $\Delta q$, cannot fully control flying capacitor voltages, leading to unconstrained steady state.

At other nominal conversion ratios (for example, $1/4$) where the charge transfer matrix is full-rank, [8] proved that matrix $\boldsymbol{C}$ is also full-rank. Flying capacitor voltages are fully controlled by the feedback of the inductor system, which is characterized by (19) and (20). To better visualize the actual function of the feedback, substituting (14) recursively into (16) gives:

$$\Delta q(n) = Ff^{n-1}\Delta I_L(1) + Fg\sum_{j=1}^{n-1} f^{n-1-j}\Delta V_x(j) + G\Delta V_x(n).$$

The output, $\Delta q$, is weighted sum of the input history (along with the initial condition): it is essentially a discrete-time integrator with decaying coefficient. Assuming the closed-loop system is stable due to damping effect of $R_{esr}$, the integrator drives its input, $\Delta V_x$, to zero in steady state, turning (12) into a homogeneous equation. Since the coefficient matrix, $\boldsymbol{C}$, is full-rank, a unique solution can be found: $[\Delta V_{C1}(\infty), \Delta V_{C2}(\infty), \Delta V_{C3}(\infty)]^T = [0,0,0]^T$. Therefore, the converter has zero steady state and is naturally balanced.

Generally, for an $N$+1 level FCML converter with a nominal conversion ratio of $m/N$, [3] showed that under PSPWM operation, the converter is naturally balanced if $m$ and $N$ are coprime integers. Combining with [8], this conclusion can be expanded: at nominal conversion ratios, under any valid switching scheme, *FCML converters are naturally balanced and flying capacitor voltages are controllable and observable if the charge transfer matrix $\boldsymbol{B}$ is full-rank*, where $rank(\boldsymbol{B})$ only depends on capacitor connections in each phase.

### B. Closed-Loop Analysis

The model of switched capacitor system and inductor system are derived in section II, rewritten here for reference:

$$\begin{cases} \Delta \boldsymbol{V_C}(k+1) = \boldsymbol{A}\Delta \boldsymbol{V_C}(k) + \boldsymbol{B}\Delta \boldsymbol{q}(k) \\ \Delta \boldsymbol{V_x}(k) = \boldsymbol{C}\Delta \boldsymbol{V_C}(k) + \boldsymbol{D}\Delta \boldsymbol{q}(k) \end{cases}; \quad (23)$$

$$\begin{cases} \Delta I_L(k+1) = P\Delta I_L(k) + \boldsymbol{Q}\Delta \boldsymbol{V_x}(k) \\ \Delta \boldsymbol{q}(k) = \boldsymbol{R}\Delta I_L(k) + \boldsymbol{S}\Delta \boldsymbol{V_x}(k) \end{cases}. \quad (24)$$

The switching node voltage, $\Delta \boldsymbol{V_x}$, is the switched capacitor system output and inductor system input; the charge transferred through the inductor, $\Delta \boldsymbol{q}$, is the switched capacitor system input and inductor system output. They are internal signals that describe the interaction between the subsystems (see Fig. 2). In closed-loop analysis, internal signals are canceled out to highlight characteristics of the overall system. Mathematically, solving (23) and (24) gives:

$$\begin{bmatrix} \Delta \boldsymbol{V_C}(k+1) \\ \Delta I_L(k+1) \end{bmatrix} = \boldsymbol{A_{cl}}\begin{bmatrix} \Delta \boldsymbol{V_C}(k) \\ \Delta I_L(k) \end{bmatrix}. \quad (25)$$

The closed-loop system matrix, $\boldsymbol{A_{cl}}$, characterizes the overall system, and is given by the following expression:

$$\boldsymbol{A_{cl}} = \begin{bmatrix} \boldsymbol{A + BTSC} & \boldsymbol{BTR} \\ \boldsymbol{QC + QDTSC} & \boldsymbol{P + QDTR} \end{bmatrix}$$

where $\boldsymbol{T} = (\boldsymbol{I - SD})^{-1}$, and $\boldsymbol{I}$ is the identity matrix.

Equation (25) wraps all the system dynamics into one single equation, and eigenvalues of $\boldsymbol{A_{cl}}$ determine system stability. If all the eigenvalues have a magnitude smaller than one, the system is asymptotically stable: for any initial condition, the steady state is zero, and the FCML converter is naturally balanced. If at least one eigenvalue has a magnitude greater than one, the system is unstable: for any non-zero initial condition, the steady state is unbounded, and the FCML converter is naturally imbalanced. If the largest magnitude of the eigenvalues is equal to one, the system is marginally stable: for a non-zero initial condition, the steady state is bounded but not zero, therefore the FCML converter is also imbalanced.

Among the three cases above, instability is unlikely to happen without positive feedback, and is not a concern here. But the closed-loop system can be marginally stable, and in fact, this is always the case when the charge transfer matrix $\boldsymbol{B}$ is not full-rank. To prove this, we need to investigate the matrix $\boldsymbol{A_{cl}} - \boldsymbol{I}$, where $\boldsymbol{I}$ is the identity matrix:

$$\boldsymbol{A_{cl}} - \boldsymbol{I} = \begin{bmatrix} \boldsymbol{BTSC} & \boldsymbol{BTR} \\ \boldsymbol{QC + QDTSC} & \boldsymbol{P + QDTR} - 1 \end{bmatrix}$$
$$= \begin{bmatrix} \boldsymbol{B} & \boldsymbol{0} \\ \boldsymbol{0} & 1 \end{bmatrix} \begin{bmatrix} \boldsymbol{TS} & \boldsymbol{TR} \\ \boldsymbol{Q + QDTS} & \boldsymbol{P + QDTR} - 1 \end{bmatrix} \begin{bmatrix} \boldsymbol{C} & \boldsymbol{0} \\ \boldsymbol{0} & 1 \end{bmatrix},$$

or denoted as

$$(\boldsymbol{A_{cl}} - \boldsymbol{I})_{N\times N} = \boldsymbol{B'}_{\boldsymbol{N}\times(\boldsymbol{N+1})} \boldsymbol{MC'}, \qquad (26)$$

where the subscripts show the dimensions of matrices for an $N$+1 level FCML converter. If $\boldsymbol{B}$ is not full-rank, $\boldsymbol{B'}$ is not full-rank either, meaning $rank(\boldsymbol{B'}) < N$. Since the rank of a matrix product is not greater than the rank of any factor, we have $rank(\boldsymbol{A_{cl}} - \boldsymbol{I}) < N$, which leads to $det(\boldsymbol{A_{cl}} - \boldsymbol{I}) = 0$. Therefore, when $\boldsymbol{B}$ is not full-rank, $\boldsymbol{A_{cl}}$ has an eigenvalue on the unit circle, and the closed-loop model is marginally stable, meaning the FCML converter is subject to imbalance. This is consistent with the conclusion in open-loop analysis.

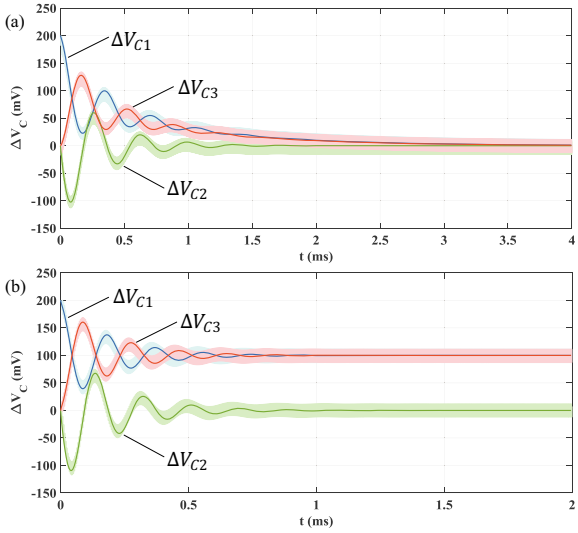


Fig. 5. Transient response of state variables at (a) 1/4 conversion ratio and (b) 2/4 conversion ratio; inductor current, $\Delta I_L$, is not shown.

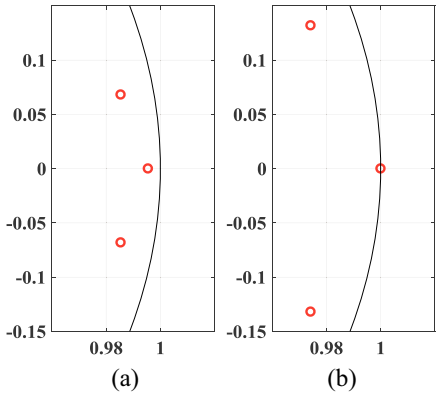


Fig. 6. Eigenvalues of $\boldsymbol{A_{cl}}$ in z-plane at (a) 1/4 conversion ratio and (b) 2/4 conversion ratio; the unit circle is marked with black for reference; the fourth eigenvalue is close to the origin thus does not appear.

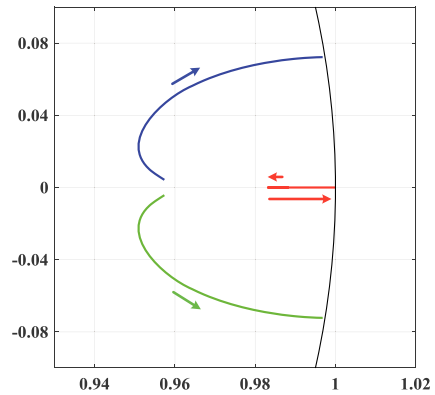

Fig. 7. Eigenvalue trajectories in z-plane at 1/4 conversion ratio when the quality factor changes from 0.1 to 100; the unit circle is marked with black for reference; the fourth eigenvalue is close to the origin thus does not appear.

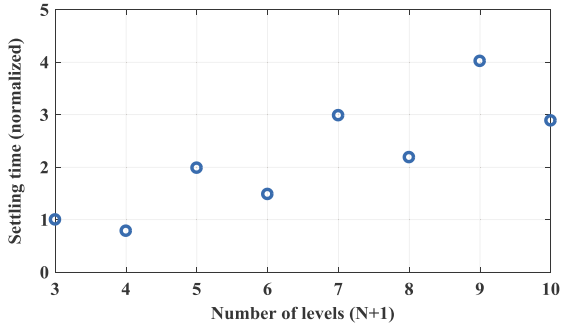


Fig. 8. Settling time of disturbances in N+1 level FCML converters at 1/N conversion ratios; the settling time is normalized to that of a 3-level converter; the phase duration is kept constant for different number of levels.

Under PSPWM operation, state-space simulation and circuit simulation are conducted on a 5-level FCML covnerter. Fig. 5 and Fig. 6 show the transient response of state variables and eigenvalues of $\boldsymbol{A_{cl}}$, at conversion ratios of $1/4$ (balanced case) and $2/4$ (imbalanced case), with the same circuit parameter. In Fig. 5, the initial condition (which models the disturbance) of $V_{C1}$ is set to 200mV, while others are zeros. Circuit simulation results are plotted with light colors (because of voltage ripple, they look like bands); state-space simulation results are plotted with darker colors. Both the steady state values and the dynamics match well. As predicted by the state-space analysis, at 1/4 conversion ratio, the charge transfer matrix $\boldsymbol{B}$ is full-rank and the magnitude of all eigenvalues are smaller than one, the closed-loop model is asymptotically stable and the converter is balanced; at 2/4 conversion ratio, the charge transfer matrix is not full-rank and one eigenvalue is on the unit circle, the closed-loop model is marginally stable and the converter is imbalanced.

With the closed-loop system model, it is possible to sweep circuit parameters and observe the change of eigenvalue locations. An example that sweeps $R_{esr}$ at 1/4 conversion ratio is shown in Fig. 7, where the quality factor, $Q$, changes from 0.1 to 100. Arrows indicate the moving direction of the corresponding eigenvalues. As $R_{esr}$ decreases (and $Q$ increases), the eigenvalues first move away from the unit circle and then move towards the unit circle, which means the balancing dynamics first accelerate and then slow down. The influence of other parameters can be explored as well.

Another interesting observation is the comparison between even and odd level FCML converters. The settling time of response to disturbances at the lowest nominal conversion ratio (where the converter is always naturally balanced) are plotted against the number of levels in Fig. 8. Even-level converters exhibits stronger rejection to disturbances than odd-level converters. The same phenomenon was observed and discussed in [4].

It is worth noticing that, in practical implementation, naturally balanced FCML converters do not necessarily operate in the balanced state. Non-idealities (such as input impedance, timing mismatch, etc.) can be modeled as disturbances on flying capacitor voltages. The state-space analysis shows that for naturally balanced FCML converters, instantaneous disturbance results in zero steady state. However, in practice, disturbances are usually continuous over time, and the steady

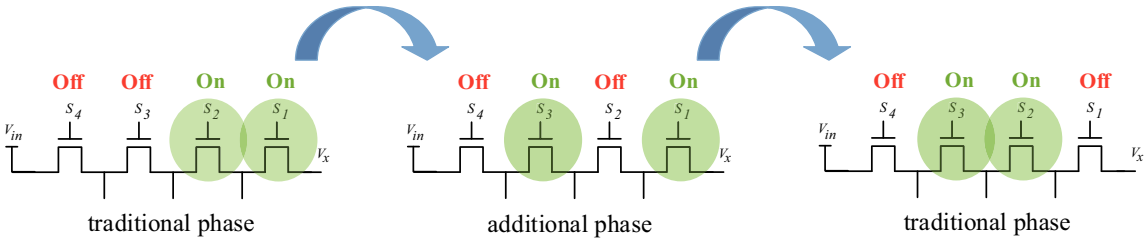


Fig. 9. An additional phase is inserted between two traditional phases.

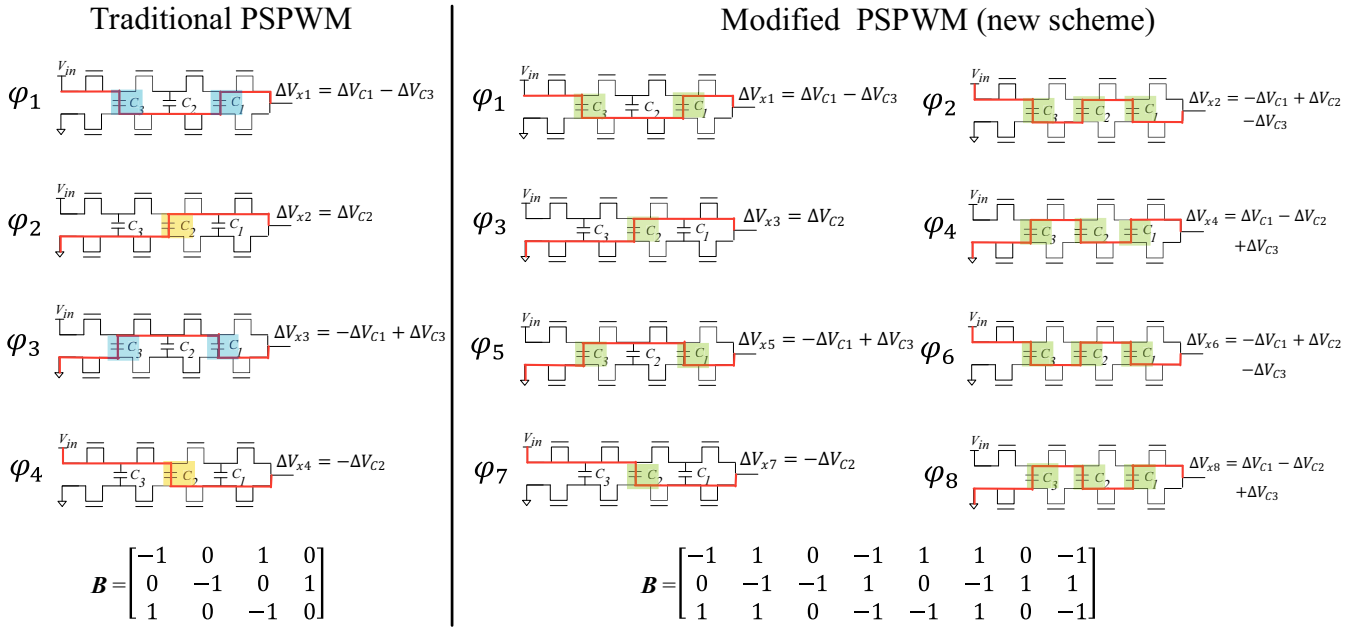


Fig. 10. Comparison of traditional PSPWM and modified PSPWM (new switching scheme) at 2/4 conversion ratio.

state is not necessarily zero. In short, *natural balancing indicates the capability to compensate for disturbances, but not immunity to disturbances.*

## IV. Switching Scheme and Experimental Results

Under traditional PSPWM operation, FCML converters are naturally imbalanced at some nominal conversion ratios (where the charge transfer matrix $\boldsymbol{B}$ is not full-rank). The analysis outlined in section III points towards a simple and direct method to rectify this imbalance issue. By modifying the switching scheme, it is possible to make $\boldsymbol{B}$ full rank, and thus naturally balance the converter. This can be done without increasing switching losses and without hardware complexity.

### A. Modified PSPWM scheme

The new switching scheme (modified PSPWM) is obtained by inserting an additional phase between every two traditional phases. For a 5-level FCML converter with 2/4 conversion ratio, Fig. 9 shows top side switches driven by the new scheme during a sample of 3 phases: in traditional PSPWM, 'on' switches are shifted together, whereas in the new scheme, they are shifted one by one. This pattern can be repeated for a full PSPWM period, yielding all of the phases shown in Fig. 10, where phase $n$ is abbreviated as $\varphi_n$, and the current flow paths are highlighted in red. In traditional PSPWM, capacitor $C_1$ and $C_3$ are always connected in a group (highlighted in blue), which leads to certain linear dependency among row vectors of matrix $\boldsymbol{B}$ (thus $\boldsymbol{B}$ is not full-rank); in the new scheme, additional phases introduce interconnections among all capacitors, so that no such 'isolated' group exists, making matrix $\boldsymbol{B}$ full-rank. According to the state-space analysis in section III, at 2/4 conversion ratio, the 5-level FCML converter is imbalanced under PSPWM operation but is naturally balanced when operated by the new switching scheme.

To compare the switching loss of these two schemes, we hold the effective switching frequency at the switching node, $f_{eff}$, as constant. The energy loss when turning one switch on and off once is denoted as $E_g$. For a traditional PSPWM period, there are 4 phases and each switch turns on and off once. The switching loss per device is: $P_{PSPWM} = E_g f_{eff}/4$. For a period in the new scheme, there are 8 phases and each switch turns on and off twice. The switching loss per device is: $P_{new} = 2E_g f_{eff}/8 = E_g f_{eff}/4$. It is clear that the new switching scheme does not introduce additional switching loss.

Past works have shown that in practical implementation, natural imbalance occurs not only at certain nominal conversion ratios, but also in their neighborhood [10]. Therefore, it is important to extend the new switching scheme to non-nominal conversion ratios, so that FCML converters can be naturally balanced at any conversion ratio. For an $N$+1 level FCML converter with a non-nominal conversion ratio of $m/N$ ($m$ is not an integer), we denote the largest integer that is smaller than $m$ as $M_f$, and the smallest integer that is greater than $m$ as $M_c$. There are $2N$ phases in a period, in which $N$ phases are the same as nominal conversion ratio $M_f/N$, and the other $N$ phases are the same as nominal conversion ratio $M_c/N$. If any nominal conversion ratio is imbalanced, the new switching scheme should be applied to the corresponding phases. If the numbers of phases do not match, the one with fewer phases should be duplicated to double that number.

### B. Experimental Validation

A 5-level FCML prototype is built to test the new switching scheme. Fig. 11 shows the printed circuit board and important parameters. In steady-state, difference between each flying capacitor voltage and its balanced value, along with the output voltage, are measured in the conversion ratio range of 0.4 to 0.6, where natural imbalance is most severe under traditional PSPWM operation. Experimental results validate the model at 2/4 conversion ratio: $C_1$ and $C_3$ are imbalanced in PSPWM operation and are balanced in Modified PSPWM operation, as shown in Fig. 12. Moreover, the new switching scheme naturally balances the converter at conversion ratios that are close to 2/4.

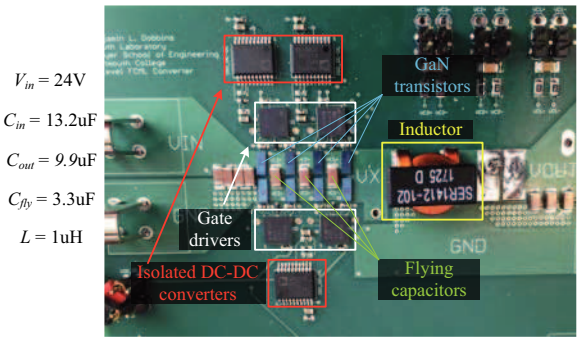


Fig. 11. Printed circuit board and important parameters of the prototype.

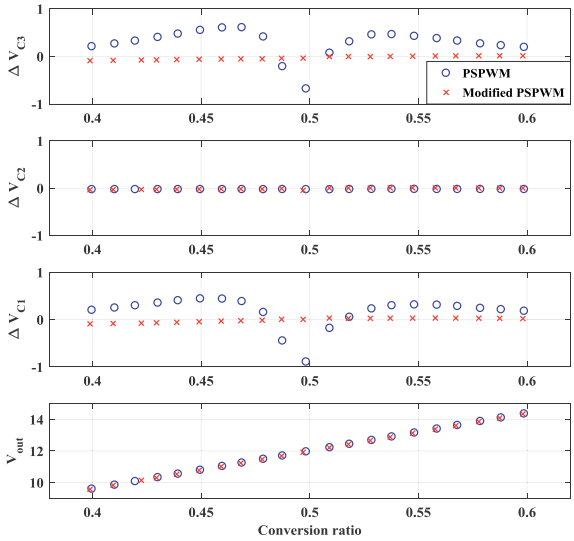


Fig. 12. Steady state values of flying capacitor voltages using traditional PSPWM and Modified PSPWM, with a load current of 200mA.

Fig. 13 shows the converter efficiency under a load current sweep using traditional and new switching schemes. Both schemes have similar efficiency at light load, which verifies

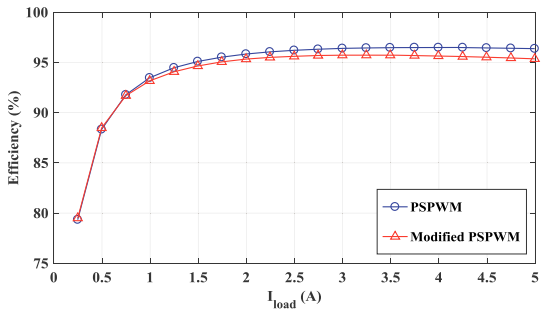


Fig. 13. Converter efficiency when operated by traditional PSPWM and Modified PSPWM (the new scheme).

that the new switching scheme does not introduce additional switching loss. However, in modified PSPWM, more flying capacitors are connected in series during additional phases, which increases conduction loss and cause an efficiency drop at heavy load. It is also observed that the converter becomes imbalanced at heavy load even under the new switching scheme. These problems can potentially be mitigated by adjusting gate drive timing (such as applying active balancing control), and remains to be further investigated.

## V. Conclusions

In this work, a state-space model is derived to explore natural balancing of FCML converters. It is shown that natural balancing depends on the rank of a matrix, which is determined only by the flying capacitor connections in each phase. Based on the model, a new switching scheme is developed to naturally balance FCML converters at any conversion ratio. The new switching scheme is verified by a 5-level FCML converter prototype.

## Appendix

Exact expressions for the inductor system model in section II are provided here. Solving the second-order circuit in Fig. 4 yields the time-domain expression:

$$\Delta I_L(t) = \frac{\omega_0 \Delta I_L(n)}{\omega_d} e^{-\alpha t} cos(\omega_d t + \theta) + \frac{\Delta V_x(n)}{\omega_d L} e^{-\alpha t} sin(\omega_d t), \quad (27)$$

where:

$$\alpha = \frac{R_{esr}}{2L}$$

is the attenuation;

$$\omega_0 = \frac{1}{\sqrt{LC_{eq}}}$$

is the natural resonant frequency;

$$\omega_d = \sqrt{{\omega_0}^2 - \alpha^2}$$

is the damped resonant frequency;

$$\theta = arcsin(\frac{\alpha}{\omega_0})$$

is the phase shift. By comparing (13) and (27), we have:

$$f(t) = \frac{\omega_0}{\omega_d} e^{-\alpha t} cos(\omega_d t + \theta); \quad (28)$$

$$g(t) = \frac{1}{\omega_d L} e^{-\alpha t} sin(\omega_d t). \quad (29)$$

Performing integration yields:

$$F = \int_0^{t_0} f(t)dt = \frac{1}{\omega_0 \omega_d}(e^{-\alpha t_0}(\omega_d sin(\omega_d t_0 + \theta)) - \alpha cos(\omega_d t_0 + \theta)) - (\omega_d sin\theta - \alpha cos\theta)); \quad (30)$$

$$G = \int_0^{t_0} g(t)dt = -\frac{C_{eq}}{\omega_d}(e^{-\alpha t_0}(\alpha sin(\omega_d t_0) + \omega_d cos(\omega_d t_0)) - \omega_d). \quad (31)$$


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