A CMOS MedRadio Transceiver With Supply-Modulated Power Saving Technique for an Implantable Brain–Machine Interface System

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***Abstract*— A MedRadio 413–419-MHz inductorless transceiver (TRX) for an implantable brain–machine interface (BMI) in a 180 nm-CMOS process is presented. Occupying 5.29 mm^2 of die area (including pad ring), this on–off keying (OOK) TRX employs a non-coherent direct-detection receiver (RX), which exhibits a measured in-band noise figure (NF) of 4.9 dB and S_{11} of −13.5 dB. An event-driven supply modulation (EDSM) technique is introduced to dramatically lower the RX power consumption. Incorporating an adaptive feedback loop, this RX consumes 42-/92-μW power from 1.8-V supply at 1/10-kbps data rates, achieving −79/−74-dBm sensitivities for 0.1% bit error rate (BER). The TX employs a current starved ring oscillator with an automatic frequency calibration loop, covering 9% supply voltage variation and 15 °C–78 °C temperature range that guarantees operation within the emission mask. The direct-modulation TX achieves 14% efficiency for a random OOK data sequence at −4-dBm output power. Wireless testing over a 350-cm distance accounting for bio-signal data transfer, multi-user coexistence, and *in vitro* phantom measurement results is demonstrated.**

***Index Terms*— Brain–machine interface (BMI), CMOS, event-driven supply modulation (EDSM), *in vitro* phantom, MedRadio band, multi-user coexistence, transceiver (TRX).**

I. Introduction

IMPLANTABLE medical devices, such as deep brain stimulators [1] or responsive neurostimulators [2], are routinely used for the treatment of neurological conditions. As technology advances, these systems are also becoming more sophisticated, and this trend will continue in the future. In addition, current brain implants will likely be re-purposed or redesigned in the future to address unmet clinical needs [3]. To fulfill their role, these future implantable systems will need to be endowed with additional features and functions. One such novel clinical application is the restoration of motor function after stroke or spinal cord injury (SCI) using brain–machine interfaces (BMIs). Generally, BMIs record, process, and decode cortical signals in real time and use this information to control external devices [4]. This enables those with paralysis to operate prostheses [5] or muscle stimulators [6] directly from the brain while bypassing the neurological injury. Current state-of-the-art invasive BMIs are mostly used in a laboratory setting, and their clinical adoption will critically depend on the ability to make them fully implantable. Despite encouraging results [7], these systems rely on external electronics and skull-protruding components, which makes them impractical, less safe, and generally unsuitable for everyday at-home use. These obstacles can be circumvented by designing a fully implantable BMI with internal electronics and no skull-protruding components.

Fig. 1 shows an example of a hypothetical implantable BMI system for restoration of walking in individuals with SCI. This system comprises a skull unit for brain signal sensing and a chest-wall unit (CWU) for signal processing. μV-level brain signals sensed by the skull unit are routed out of the head by a subcutaneous tunneling cable (similar to modern deep-brain stimulators [8]), and delivered to the CWU. The CWU processes brain signals to detect walking intentions and converts them into 1–10-kbps wireless commands for external prostheses, such as robotic exoskeletons or functional electrical stimulators. A major design challenge for this system is then to perform signal processing and wireless data transmission tasks while meeting the size, power, and magnetic resonance imaging (MRI) compatibility constraints necessary for safe human implantation. This includes trading off the power consumption of the DSP and transceiver (TRX) modules.

For example, wireless communication between the implantable devices and external computers is typically a

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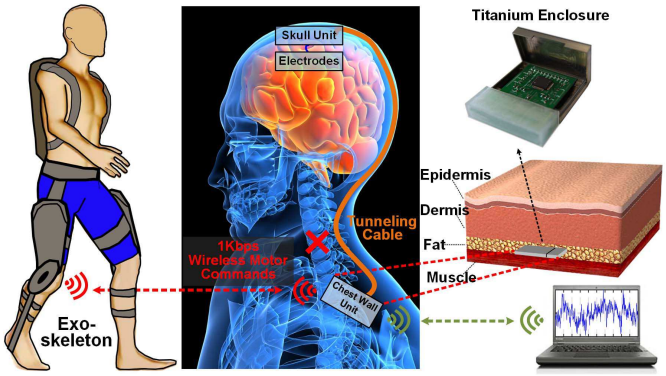


Fig. 1. Proposed fully implantable BMI system for restoration of walking, with a signal acquisition front end (skull unit) and signal processing and wireless communication modules (chest wall unit). This system bypasses the SCI and enables direct brain control of an exoskeleton.

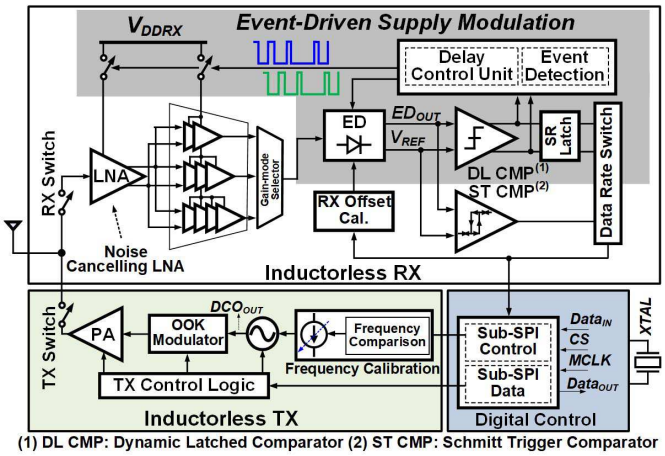


Fig. 2. Architecture of the proposed low-power OOK TRX.

power-hungry process. Therefore, minimizing the power consumption of the wireless TRX would enable allocation of a higher fraction of the overall power budget to the brain signal processing units within the CWU. Based on our preliminary estimate, the proposed CWU should consume less than 50 mW for which DSP, data converter, and other modules account for 80%–90% of total budget and with the remainder allocated to the TRX block. In addition, limited enclosure area requires small form factor for all wireless unit's constituent components including the antenna. Also, to meet the most stringent field conditions (i.e., static magnetic field strength, specific absorption rate, etc.) due to interactions with the magnetic field of MRI system, the proposed CWU shown in Fig. 1 relies on an inductorless TRX with no off-chip component except an antenna. Commercially available MRI-conditional devices use customized structures to enclose antenna to further reduce magnetic interaction and, hence, satisfy the MRI requirements for implantable systems (e.g., Medtronic W1DR01/W1SR01 [9]).

Multiple telemetry methods—such as near-field magnetic coupling, conduction through the body, and short-range RF communication—exist that establishes the link between the implanted device and external units or actuators. Human body communication (HBC defined in IEEE 802.15.6 standard) uses the human body as a channel and has emerged as a promising method for low power and relatively high data rate (>1 Mb/s) while being free from shadowing effect. However, challenges such as interference, difficulty in estimating the channel, impedance variation of skin–electrode interface, and multipath problem have to be addressed for this method to become widespread [10], [11]. IEEE 802.15.4 Bluetooth low energy (BLE), and IEEE 802.15.6 narrowband (NB) and ultrawideband (UWB) physical layers (PHYs) standards have been developed for short-range radios and cover low-power applications (e.g., wireless personal area network and wireless body area network). These standards employ duty cycling for power saving and interference mitigation. Although low power, the radios based on these standards still do not satisfy the severe power budget, heat dissipation, low emission power, and small area constraints required for an implantable BMI system such as the one shown in Fig. 1. A near-field radio for syringe-implanted sensor nodes was presented in [12] which implemented a communication protocol that eliminated the need for symbol boundary synchronization in the sensor RX. The asymmetric nature of the architecture shifts the performance burden (i.e., high-sensitivity RX and high-power TX) toward the base station [12]. The N-path uncertain-IF and dual-IF architectures proposed in [13] and [14] conduct high-Q selectivity frequency translation without the power-hungry phase-locked loop (PLL). A TX-referenced RX published in [15] improves the interference robustness and breaks the tradeoff between power, sensitivity, and linearity. A two-tone TRX using a simple envelope-detection RX and a direct-modulation TX was presented in [16].

MedRadio band (401–406 MHz) was dedicated by the Federal Communications Commission (FCC) for implantable and wearable devices, which has been expanded recently by allocating four 6-MHz bands at 413–419 MHz, 426–432 MHz, 438–444 MHz, and 451–457 MHz. Recently published MedRadio TRXs in [17]–[20] employed bulky on- or off-chip inductors for impedance matching and/or performance improvement. Contrary to aforementioned prior work, expanding on our prior work [21], this paper presents analysis and design of a CMOS low-power inductorless on–off keying (OOK) TRX for the MedRadio 413–419-MHz band intended for transferring the BMI control commands and monitoring bio-signals wirelessly. A novel event-driven supply modulation (EDSM) technique on the RX side (see Sections III and IV) and a fast startup power cycling capability on the TX side (see Section V) are utilized.

II. TRX Architecture

Fig. 2 demonstrates the proposed MedRadio TRX comprising a supply-modulated non-coherent direct-detection RX and a direct-modulation OOK TX. On the RX side, the incoming signal is strobed by a periodically activated noise-canceling low-noise amplifier (LNA) above the Nyquist rate of the baseband (BB) signal representing the BMI control commands.

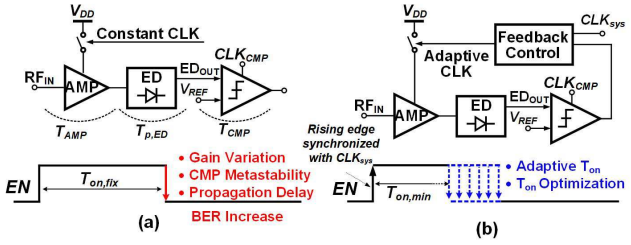


Fig. 3. (a) ED-based receiver with a fixed pulsewidth. (b) Proposed EDSM receiver with adaptive feedback control loop.

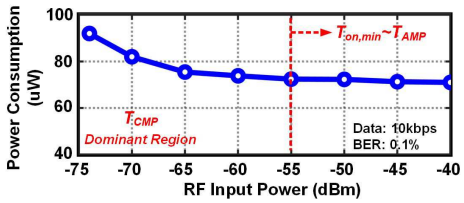


Fig. 4. Simulated RX power consumption versus the input power.

The BB signal is then recovered after passing through an envelope detector (ED) and a dynamic latched comparator, as a decision circuitry. A feedback control circuit turns off the RX amplifiers as soon as the current bit is resolved, effectively duty-cycling the RX. As will be illustrated in Section III, this approach will minimize the average power consumption with minor degradation (∼5 dB per 1 decade increase in data rate) in RX sensitivity. On the TX side, the BB data modulates the free-running digitally controlled oscillator (DCO) incorporating a fast frequency calibration loop, which allows the entire TX to be power-cycled. The OOK modulated signal is amplified by a self-biased, inverter-based power amplifier (PA) and is subsequently delivered to an off-chip antenna (for testing purpose only).

III. Asynchronous Event-Driven Supply Modulation

A conventional direct-detection RX continuously senses, amplifies, and detects the envelope (or power) of the received signal [22], [23]. Following the envelope detection, the clocked comparator generates the BB data. However, the power-hungry blocks, namely, LNA and gain stages—operating at high current levels for noise and power matching purposes—are always activated during the entire detection/comparison phase irrespective of BB signal activities. A number of duty-cycling-based power reduction techniques have been presented [24], [25] to periodically switch off power-hungry blocks with an enable signal. The average power consumption of the duty-cycled RX is approximated as

$$P_{\text{avg}} = P_T \times \left(\frac{2T_{\text{on}}}{T_b}\right) \times \text{OSR} + P_{\text{bias}} \tag{1}$$

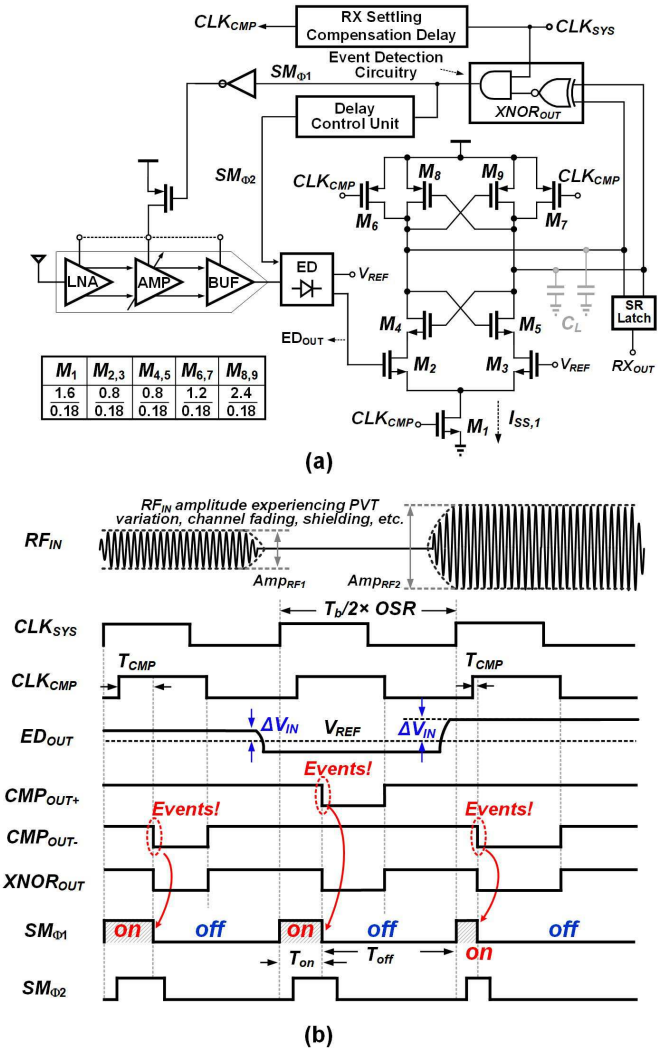
where P_T is the total power consumption of the RX core without duty-cycling technique, T_{on} represents the RX on time, T_b denotes the bit period, and OSR is the oversampling ratio. P_{bias} is the power consumption of the bias generation circuit. Clearly, the duty-cycling technique leads to significant amount of power saving if $T_{\text{on}} \ll T_b$. However, the supply switching in prior work is done at a fixed pulsewidth $T_{\text{on,fix}}$ [indicated in Fig. 3(a)] which must account for worst case conditions, i.e., lowest LNA gain, largest comparator metastability time-constant, and signal propagation delay uncertainty across process, voltage, and temperature (PVT) variation. As a result, the amount of power saving is severely limited by this non-optimal $T_{\text{on,fix}}$, which will be analyzed as follows.

To overcome the power-saving limitation due to $T_{\text{on,fix}}$ and further reduce T_{on}, we first study the parameters affecting it. T_{on} is approximately lower bounded by $T_{\text{on}} \geq T_{\text{on,min}}$ $(= T_{\text{AMP}} + T_{p,\text{ED}} + T_{\text{CMP}})$. T_{AMP} denotes the time taken for the duty-cycled amplifier to reach its stable dc-bias point at the rising edge of the enable (EN) signal shown in Fig. 3(b). $T_{p,\text{ED}}$ is the input–output propagation delay of the ED. T_{CMP} represents the time taken by the comparator to make a decision. For the dynamic comparator adopted in this design [see Fig. 5(a)], T_{CMP} is readily derived to be

$$T_{\text{CMP}} \cong \frac{2|V_{\text{THP}}|C_L}{I_{SS,1}} - \frac{C_L}{G_m}\ln(\Delta V_{\text{IN}}) \tag{2}$$

where V_{THP} indicates the PMOS threshold voltage, $I_{SS,1}$ is the tail current, M_1. C_L is the load capacitor seen at the output of the comparator. G_m represents the equivalent large-signal transconductance of each cross-coupled CMOS inverter (M_4–M_8 and M_5–M_9) realizing regenerative load of the comparator. ΔV_{IN} is the comparator's input amplitude and T_f is a fixed time which is determined by the bias current, the load capacitor, and input device parameters. T_{CMP} is the signal dependent, whereas T_{AMP} and $T_{p,\text{ED}}$ are both functions of PVT and may vary from chip to chip. Fig. 4 displays the simulated RX power consumption versus the RF input power. From Fig. 4, T_{CMP} will become a major contributor to the power-saving feature as the input power decreases below a certain level (e.g.,−55 dBm). In addition, T_{AMP} can constitute an increasingly larger portion of T_{on}, eventually limiting the functionality of the EDSM-based RX to data rates below 0.5 Mbps. In this case, techniques such as bias pre-charge should be used in the amplifiers to minimize T_{AMP} and $T_{p,\text{ED}}$.

The functional block diagram of the EDSM-based RX is depicted in Fig. 3(b) where an adaptive feedback control loop (details in Section IV) is employed to guarantee duty-cycling at $T_{\text{on}} = T_{\text{on,min}}$. Similar to the conventional architecture, upon envelope detection and the BB data recovery, the feedback control unit will capture the comparison result and generates the control pulses to turn off the power-hungry blocks, thereby lowering the average power consumption. Unlike the duty-cycled RX architectures with constant on time [Fig. 3(a)], the EDSM technique generates control pulses whose pulsewidths vary with $ED_{\text{out}} - V_{\text{ref}}$ at the comparator inputs. More precisely, the falling edge of these pulses is automatically adjusted depending on the RF signal power, the amplifier gain, and the envelope detection responsivity across PVT variation as soon as the comparator decision has been made [Fig. 3(b)]. In summary, this technique optimizes



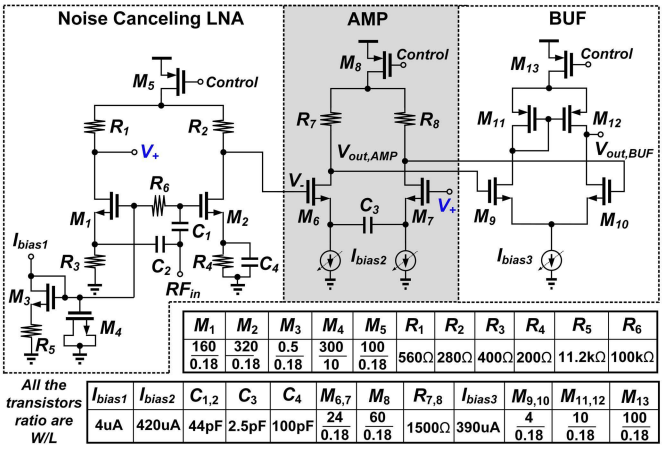
M_1	$M_{2,3}$	$M_{4,5}$	$M_{6,7}$	$M_{8,9}$
1.6/0.18	0.8/0.18	0.8/0.18	1.2/0.18	2.4/0.18

Fig. 5. (a) Event-driven supply-modulated RX schematic. (b) Timing diagram of EDSM RX.

the turn-off edge of EN signal to minimize T_{on}, thereby achieving the lowest power consumption.

IV. Receiver Implementation

The EDSM RX architecture is shown in Fig. 5(a). An event detection circuitry and a delay control unit generate and adjust variable duty-cycle power-switching pulses $SM_{\phi 1}$ for amplifiers and settling time accelerating pulses $SM_{\phi 2}$ for the ED. The system clock (CLK_{SYS}) is provided by an external source [a crystal oscillator (XTAL) in this design]. The external source will be provided by a microcontroller, once this TRX is integrated with the CWU. Running at Nyquist rate of the BB signal, CLK_{SYS} periodically turns on the LNA to strobe the received signal. A delayed version of CLK_{SYS}, CLK_{CMP}, triggers the clocked comparator and marks an "event," T_{CMP} seconds after its positive edge [*cf.* Fig. 5(b)]. During the event interval, the outputs are captured in an SR latch and are also fed to the event detection circuitry. Enabled by CLK_{SYS}, the event detection circuit generates the falling edges of $SM_{\phi 1}$ once it senses an event, and subsequently



M_1	M_2	M_3	M_4	M_5	R_1	R_2	R_3	R_4	R_5	R_6
160/0.18	320/0.18	0.5/0.18	300/10	100/0.18	560Ω	280Ω	400Ω	200Ω	11.2kΩ	100kΩ

All the transistors ratio are W/L	I_{bias1}	I_{bias2}	$C_{1,2}$	C_3	C_4	$M_{6,7}$	M_8	$R_{7,8}$	I_{bias3}	$M_{9,10}$	$M_{11,12}$	M_{13}
	4uA	420uA	44pF	2.5pF	100pF	24/0.18	60/0.18	1500Ω	390uA	4/0.18	10/0.18	100/0.18

Fig. 6. Schematic of noise-canceling LNA, capacitively degenerated cascaded gain stage unit and differential to single-ended buffer.

turns off the power-hungry LNA and amplifiers until the next strobing edge (set by the positive edge of CLK_{SYS}).

Although the linearity requirement of a direct-detection OOK RX is relaxed, its noise performance deserves attention. The noise analysis of a direct detection RX is more involved as the inherent nonlinearity of the ED causes a whole host of issues, such as the noise self-mixing phenomenon. Although the commonly used noise-equivalent power (NEP) provides a more accurate evaluation of an ED's noise performance, especially at high frequencies, relating it to the overall noise figure (NF) of the RX is not straightforward. We thus utilize the conversion gain (see Section IV-B) to characterize noise and signal frequency translations in an ED. The RF noise at the ED input will be translated to low frequency at the output through its conversion gain. On the other hand, the low-frequency noise within the ED bandwidth is amplified by a large and linear dc gain. The RX chain's NF is derived as follows:

$$NF_{RX} = NF_{\text{amp}} + \frac{\overline{V_{n,\text{ED}}^2} + \overline{V_{n,LF}^2} A_{\text{ED,dc}}^2}{4kTR_s A_V^2 A_{\text{ED}}^2} \tag{3}$$

where $\overline{V_{n,LF}^2}$ and $\overline{V_{n,ED}^2}$ are the low-frequency noise power at the ED input and the noise contribution of the ED, respectively. NF_{amp} is the NF of the amplification chain, A_V is the voltage gain of the entire amplification chain, and $A_{\text{ED,dc}} = V_{o,dc}/V_{\text{in,dc}}$ and $A_{\text{ED}} = V_{o,\text{dc}}/V_{\text{in,RF}}$ are the dc and conversion gains of the ED, respectively.

A. Noise-Canceling LNA and Gain Stages

Fig. 5 shows the overall RX front end consisting of a noise-canceling LNA, cascaded gain stage unit(s), differential to single-ended buffers, and a gain-mode selector. To cover an adequate TX–RX link range, three distinct parallel paths accommodating low, medium, and high gain modes are considered in this design. The use of three gain paths instead of a variable gain amplifier (VGA) allows for noise and power optimization of devices in each path distinctly, resulting in better power efficiency [26]. The gain mode can be selected through a digital automatic gain control in the back-end processor (an off-chip microcontroller). Fig. 6 shows the LNA schematic,

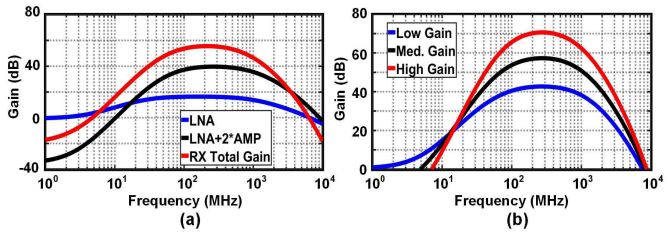


Fig. 7. (a) Simulated gain of each stage in the receiver chain. (b) Simulated gain curves of receiver in different gain modes.

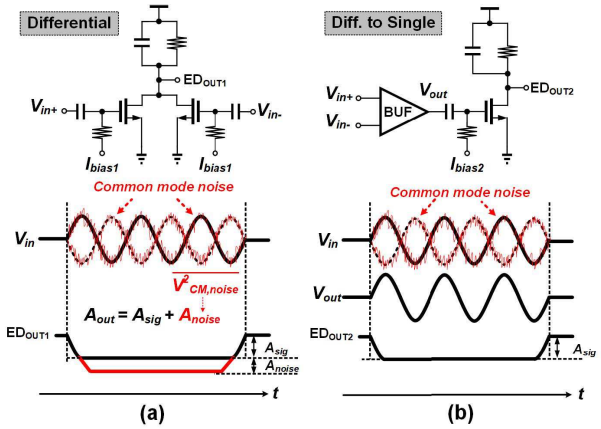
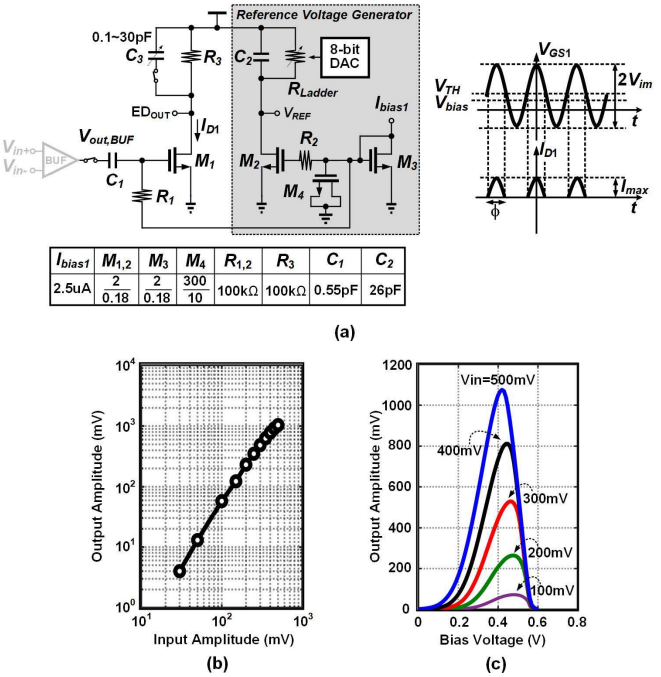


Fig. 8. Output voltage level with input signal with common-mode noise in (a) active differential architecture and (b) differential-to-single first approach.



I_{bias1}	$M_{1,2}$	M_3	M_4	$R_{1,2}$	R_3	C_1	C_2
2.5uA	2/0.18	2/0.18	300/10	100kΩ	100kΩ	0.55pF	26pF

Fig. 9. (a) Schematic of the proposed ED. (b) Simulated ED output amplitude with different input amplitudes. (c) Simulated output dc voltage versus input bias voltage.

which is based on [27]. The common-gate stage M_1 provides a resistive 50-Ω matching to the antenna impedance (R_s). Furthermore, the common-gate and common-source branches have been biased to have identical output common-mode operation. The noise contribution of M_1 is nullified if $g_{m1}R_1 = g_{m2}R_2$. This LNA's NF is readily derived to be

$$NF_{\text{LNA}} = 1 + \frac{R_s}{R_3} + \gamma\frac{R_2}{R_1} + \frac{R_s}{R_1} + \frac{R_sR_2}{R_1^2} \tag{4}$$

where γ is the MOS thermal noise coefficient. The LNA is followed by a capacitively degenerated differential amplifier and a differential to single-ended buffer. The simulated gain plots of the RX front end, the LNA, and the amplification stage for the medium-gain mode are shown in Fig. 7(a). Fig. 7(b) depicts the simulated gain plot of the RX front end under different gain modes. The RX provides 30 dB (from 40 to 70 dB) gain adjustment range at 416 MHz.

B. Envelope Detector and Offset Calibration

The active differential-input envelope (power) detectors [28], [29] achieve high responsivity at the expense of common-mode noise accumulation. Fig. 8(a) shows an active differential-input push-push ED. The ED output is the sum of average signal and noise powers (V_{in}^2 and $\overline{V_{CM,\text{noise}}^2}$), inducing an unwanted rms voltage drop, A_{noise}, to the output. Fig. 8(b) shows a common-source-based single-ended ED. This detector is preceded by the last-stage differential to single-ended buffer in Fig. 6, which mitigates the common-mode noise accumulation. Fig. 9(a) shows the schematic of the ED used in this design. Assuming the long-channel MOS model and filtering of fundamental and high-order harmonics of the input, the output voltage of this ED is expressed as

$$V_{o,\text{dc}} = ED_{\text{OUT}} - V_{\text{REF}} = \frac{1}{4}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 R_3 V_{\text{im}}^2 \tag{5}$$

where V_{im} denotes the RF input amplitude. At MedRadio frequencies, the power gain is abundant, and thus the RF blocks are directly cascaded with no inter-stage matching network. This implies that the ED's conversion gain, A_{ED}, provides more insight about the ED performance rather than its responsivity $\Re$ ($= V_{o,\text{dc}}/P_{\text{in,RF}}$)

$$A_{\text{ED}} = \frac{1}{4}g_{m1}R_3\frac{V_{\text{im}}}{V_{\text{OD}}} = \frac{1}{4}A_{\text{ED,dc}}\frac{V_{\text{im}}}{V_{\text{OD}}} \tag{6}$$

where V_{OD} and g_{m1} are the overdrive voltage and transconductance of transistor M_1 in the circuit shown in Fig. 9(a). The simulated output versus input amplitude of this detector is shown in Fig. 9(b), which follows the anticipated square-law transfer characteristic.

Fig. 9(a) shows the ED's input voltage and drain current (approximated by periodic rectified cosine function) waveforms. Maximizing the second-harmonic current will maximize the conversion gain. Using the analytical study in [30], the second-harmonic current in terms of the peak drain current $I_{\max}$ and conduction angle ϕ ($= 2\cos^{-1}(V_{\text{TH}} - V_{\text{bias}}/V_{\text{im}})$) is obtained:

$$I_2 = I_{\max}\frac{2\sin^3\frac{\phi}{2}}{3\pi\left(1-\cos\frac{\phi}{2}\right)} \tag{7}$$

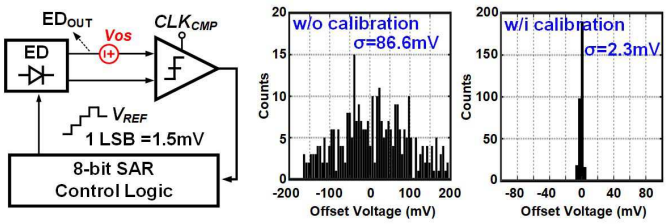


Fig. 10. Offset calibration system and Monte Carlo simulation results.

where I_2 is maximized for $\phi = \pi$, resulting in $V_{\text{bias,opt}} = V_{\text{TH}}$. This means that the ED should operate as a deep class-AB stage to maximize conversion gain, and thus relax the sensitivity constraints of the following comparator. Fig. 9(b) shows the simulated ED output amplitude with different input amplitudes. Fig. 9(c) shows the simulated output dc voltage versus input bias voltage of the ED for five different values of the input amplitude. As shown in Fig. 9(c), biasing transistor M_1 around its threshold voltage ($\approx$0.45 V) will maximize the conversion gain.

The ouput thermal noise of the ED is derived as follows:

$$\overline{V_{n,ED}^2} = 4kTR_3(1 + \gamma g_{m1} R_3). \tag{8}$$

As mentioned before, the undesired low-frequency noise in the passband of the ED is amplified by $A_{\text{ED,dc}}$.

It is worth noting that the single-ended structure in Fig. 9(a) is sensitive to the offset of the following comparator. To overcome this problem, an 8-bit offset calibration circuit incorporating a successive approximation register (SAR) feedback loop is utilized (see Fig. 10). Based on the comparator output logic level, the SAR control logic determines the output of the 8-bit digital-to-analog converter (DAC) to compensate for the input-referred offset of the dynamic comparator, capturing up to ±190-mV input-referred comparator offset within 0.3 ms. Fig. 10 shows the comparison of the statistical input-referred offset voltages of the comparator with and without this calibration scheme using Monte Carlo simulation. From the Monte Carlo simulation with 300 different samples, the result shows a 38-fold improvement (i.e., σ is reduced from 86.6 to 2.3 mV).

C. Settling Time Acceleration Switch

The amount of power saving in this RX is directly dependent on its ability to function properly within extremely short T_{on}'s. However, since the EDSM scheme turns amplifier stages on and off in every clock cycle, the voltage level at the output of the ED slews up too slowly to reach its default value, causing the comparison error at the comparator. Depicted in Fig. 11(a), the charging of the decoupling capacitor C_1 during the off-to-on dc-bias transition at the output of the buffer would induce a glitch at the gate of M_1, causing a large transient voltage drop at the output. Fig. 11(b) shows the ED incorporating two settling time acceleration switches SW_1 and SW_2 to shorten the settling time. To hold the charge across C_1 constant, the delay control unit applies a delayed version of $SM_{\phi 1}$ to SW_1 and SW_2. This avoids the voltage change at the gate–drain of M_1 during the control-signal transition, and thus considerably reduces the ED settling time.

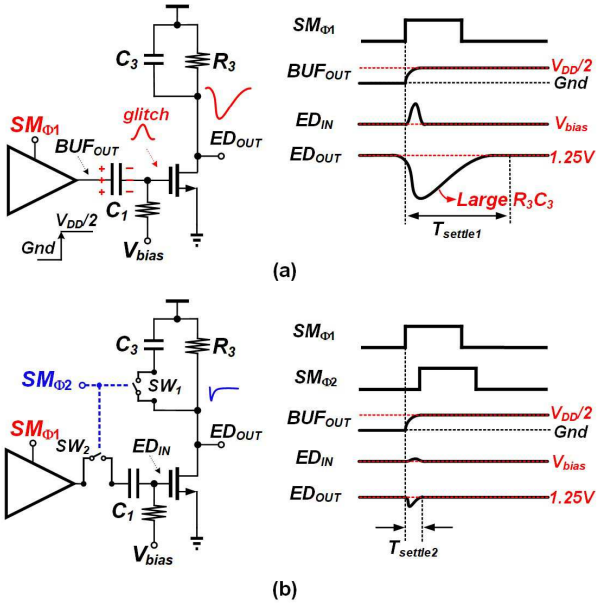


Fig. 11. Settling time of (a) conventional ED and (b) proposed ED with acceleration switch.

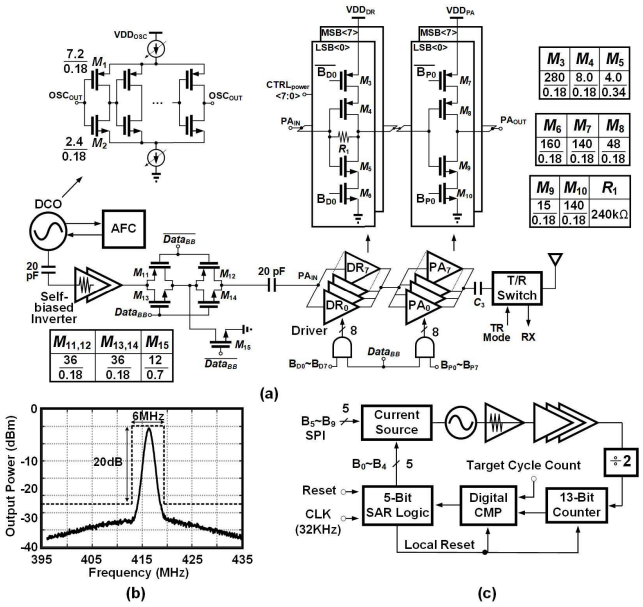


Fig. 12. (a) Schematic of the proposed direct-modulation transmitter. (b) Measured TX output power spectrum. (c) AFC block diagram.

V. Transmitter Implementation

A. Direct-Modulation Transmitter

The MedRadio band at 413–419 MHz relaxes carrier frequency stability requirement, particularly for constant-amplitude modulation schemes. As shown in Fig. 12(a), the proposed TX chain is comprised of a free-running DCO with automatic frequency calibration (AFC), OOK-modulating T-switch, and power configurable inverter-based driver and PA circuits. Fast startup time of the DCO allows for the whole TX to be power-cycled, which not only saves power but also avoids unnecessary power emission

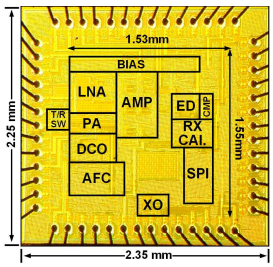


Fig. 13. Chip micrograph with main circuit blocks labeled.

when transmitting 0 s. The entire PA circuit following the DCO consists of a self-biased inverter followed by a tapered chain of eight-parallel inverter-based drivers and the PA, all biased at half-V_{DD}. The TX output power can be configured from −4 to 4.5 dBm using 8-bit driver and PA switches. Fig. 12(b) shows the measured TX power spectrum in the continuous-wave (CW) operation. With the design parameter values listed in Fig. 12(a), the T/R switch shows −1.2-dB insertion loss at −4-dBm output power.

B. Current-Starved Ring Oscillator With AFC Loop

To achieve low-power operation, a five-stage current-starved ring oscillator with digital AFC [31] is designed [Fig. 12(c)]. The oscillation frequency, f_{osc}, is controlled by 5-bit coarse- and 5-bit fine-tuned current mirrors from the serial peripheral interface (SPI) and the AFC loop, respectively, to compensate for PVT variations. Within the AFC block, the 13-bit counter computes the binary representation of divide-by-two oscillation frequency by counting its cycles over the 32.768-kHz reference clock period from a Pierce XTAL (shared by the RX). The result is compared with the target cycle count N_{CYC}, where $N_{CYC} = f_{osc}/(2f_{XTAL})$, and fed to an SAR logic to adjust the oscillator current. The tuning range is $\Delta f = 2^B$ LSB, where LSB is the fine-tuning resolution (2.5 MHz in this paper) and B is the number of control bits in SAR algorithm (5 in this paper). The calibration algorithm allocates one clock period for cycle counting, one for comparison, and one for internal reset. Therefore, the total calibration time T_{cal} is derived as $T_{cal} = 3 \times B/f_{XTAL}$. For our application, this AFC-backed DCO was implemented to achieve fine-tuning across 80-MHz frequency range within an estimated 0.47-ms calibration time. It is possible to further extend the frequency operation range by increasing the total number of control bits in the calibration system at the expense of a longer calibration time, a larger area, and additional power consumption.

VI. Experimental Results

Designed and fabricated in a 180-nm CMOS technology, this TRX occupies 2.35 × 2.25 mm^2 of die area including pads (Fig. 13). The functionality of the TRX was verified by both electrical and *in vitro* phantom measurements. The system-level measurement includes wireless testing for TX–RX distances varying from 25 to 350 cm as well as wireless transferring of pre-recorded bio-signals. In addition, coexistence testing in a multi-user environment was conducted.

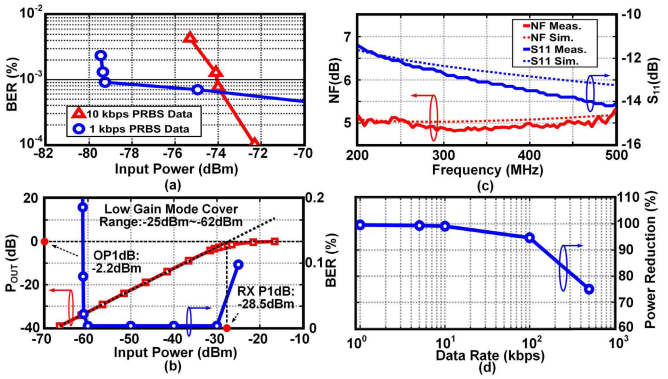


Fig. 14. RX electrical measurement results. (a) Measured BER with different data rate. (b) Linearity and BER measurement in low-gain mode. (c) Measured S11 and NF. (d) Input data rate versus power saving percentage.

TABLE I
Measured TRX Power Consumption Breakdown

Block	Before EDSM	After EDSM
LNA	5.8 mW	17.3 μW
AMPs	3.8 mW	9.2 μW
BUF+ED	0.6 mW	9.8 μW
CMP	4.2 μW	4.2 μW
Total	10.2 mW	42 μW

Block	OOK Mode
PA	1.69 mW
Driver	0.7 mW
VCO	0.42 mW

A. Receiver Electrical Measurements

Fig. 14(a) shows the measured bit error rate (BER) at 1- and 10-kbps data rates using PN15 data sequence at 1.5-V supply voltage. The BER stays below 0.1% for the input power larger than −79 and −74 dBm at 1- and 10-kbps data rates in the high-gain mode, respectively. Link-budget calculation reveals that to maintain the wireless operation at BERs below 0.1% over short distances down to 25 cm, the RX should tolerate a maximum input power larger than −28.8 dBm. Fig. 14(b) shows the measured transfer characteristic and BER versus input power under the RX's low-gain mode. The measured P_{1dB} is −28.5 dBm. Moreover, BER stays below 0.1% for input powers from −62 to −25 dBm, resulting in an overall dynamic range from −79 to −25 dBm across all gain modes. Fig. 14(c) shows both simulated and measured NF and S_{11} versus frequency. The EDSM RX achieves −13.5-dB S_{11} and 4.9-dB NF at 416 MHz, respectively, without any on-/off-chip inductor.

Table I shows the measured power consumption of each RX block before and after applying EDSM technique. The EDSM technique is capable of reducing the RX power by 99.6% to 42 μW at 1 kbps and by 99.1% to 92 μW at 10 kbps. Fig. 14(d) demonstrates the power reduction percentage as a function of the data rate, showing above 90% power reduction at data rates below 100 kbps.

B. Transmitter Electrical Measurements

Fig. 15(a) shows both measured and simulated overall TX efficiency versus output power for OOK modulated signal. The TX output power varies from −4 to 4.5 dBm with efficiency varying from 14% to 36%. In the CW mode, the efficiency

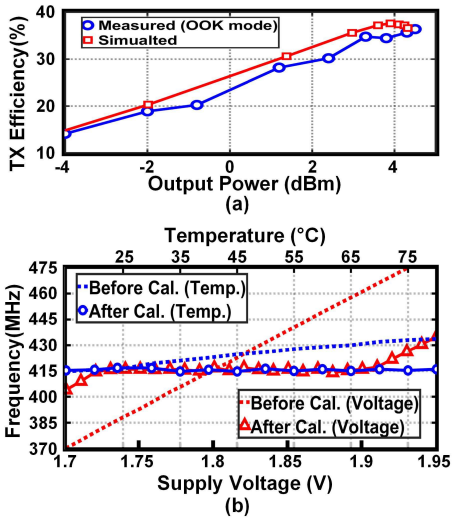


Fig. 15. (a) TX efficiency versus output power. (b) Frequency variation before and after using AFC.

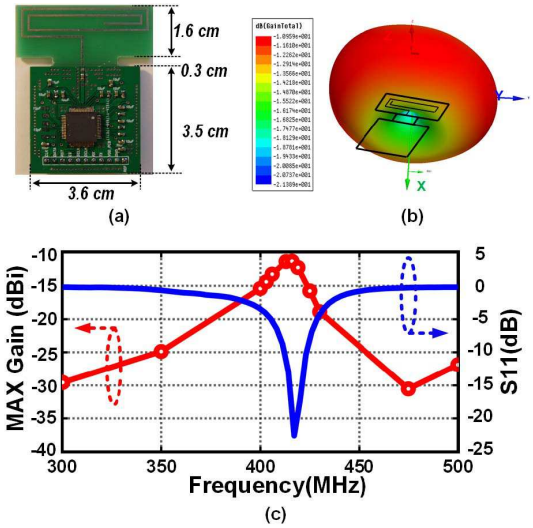


Fig. 16. (a) PCB including an on-board loop antenna and thin quad flat package (TQFP) packaged IC. (b) Simulated antenna radiation pattern. (c) Measured antenna gain and S_{11} versus frequency.

varies from 7% to 18%, since for half the time, the data are 0, and the TX is powered off. TX power breakdown in the OOK transmission mode is shown in Table I. The AFC periodically monitors the TX carrier frequency. The frequency-drift tolerance is significantly improved from 19% down to 0.24% across 1.73–1.9-V supply interval and from 4.6% down to 0.3% across 15–78 °C temperature range [*cf.* Fig. 15(b)].

C. Wireless Connection Measurement Setup and Results

To test wireless connectivity, a 416-MHz printed circuit board (PCB) loop antenna was designed and fabricated [Fig. 16(a)]. Fig. 16(b) and (c) demonstrate the simulated radiation pattern at 416 MHz and the measured antenna gain and S_{11} versus frequency, respectively. As is clear from Fig. 16(c), RF band selectivity is partially provided

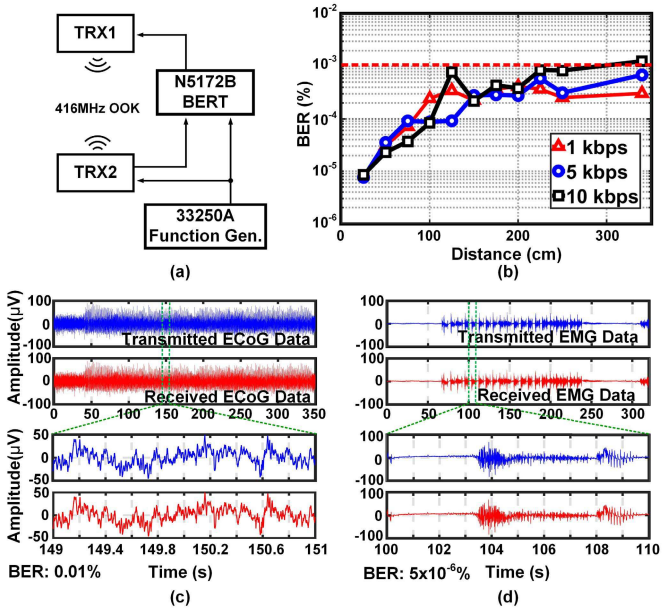


Fig. 17. (a) Setup for wireless connection measurement. (b) Measured BER with different TX-to-RX distances. The transmitted and received (c) ECoG signal and (d) EMG signal.

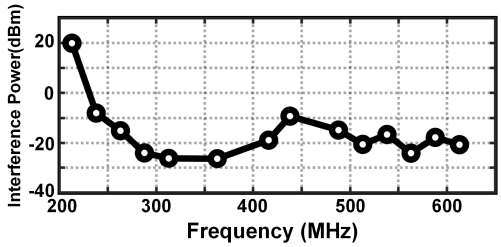


Fig. 18. Measured interference power causing BER higher than 0.1%.

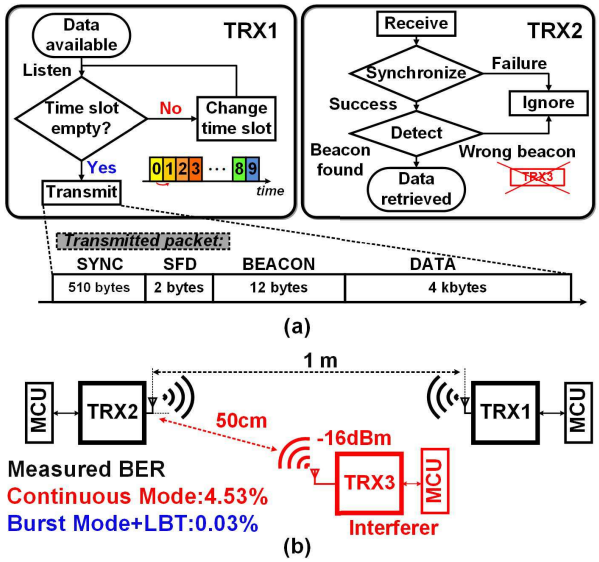


Fig. 19. (a) Flowchart of LBT protocol adopted in this paper. (b) Coexistence test setup.

by the antenna. With an emission power of −16 dBm from TX, an antenna gain of −12 dBi, and considering a 35-dB path loss across a 3-m distance at 416 MHz, the RX sensitivity is smaller than −63 dBm. Fig. 17(a)

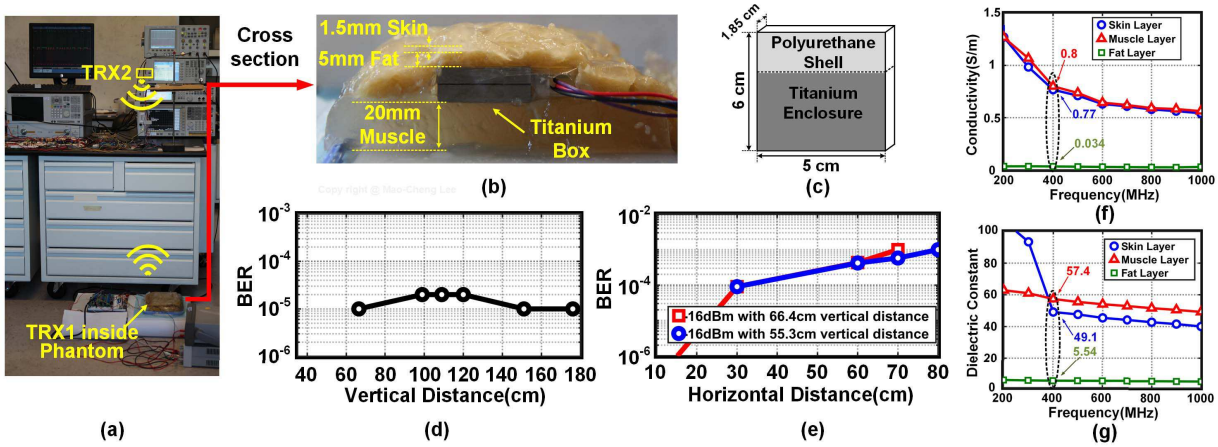


Fig. 20. (a) *in vitro* phantom measurement setup. (b) Cross section of the phantom material. (c) Dimension of titanium box and plastic cap. (d) Measured BER results with different vertical distances. (e) Measured BER results with different horizontal distances. (f) Phantom layers conductivity versus frequency. (g) Phantom layers dielectric constant versus frequency.

TABLE II
PERFORMANCE COMPARISON

Reference	ISSCC 2011 [35]	JSSC 2012 [16]	ISSCC 2014 [17]	TMTT 2014 [18]	TCAS-I 2016 [19]	JSSC 2016 [13]	JSSC 2016 [15]	This Work
Process (nm)	130	90	40	180	180	65	65	180
Carrier Freq. (MHz)	403	915	402∼405 / 420∼450	403/433	402∼405	2400	915	413∼419
Supply Voltage (V)	1	1	1	1.2	0.45	0.5	1	1.5
Architecture	Low-IF	2-Tones	Zero-IF	Direct Conv.	Low-IF	Dual-IF	TX-referenced	EDSM
Modulation	FSK	OOK	GMSK/DBPSK	ASK	OOK/FSK	OOK	BPSK	OOK
Inductor Type	Off-Chip	On-Chip	Off-Chip	Off-Chip	On-Chip	Off-Chip	Off-Chip	None
Data Rate (kbps)	200	10	11.7/562/4500	10	50/120	10	10	1/10
Sensitivity (dBm)	–70/–90	–56/–83	–112/–93/–83	–72/–73	–55/–53.5	–97	–76	–79/–74
Power	44/120 μW	63[a]/120[a] μW	2.19 mW	2.19 mW	352 μW	99 μW	135 μW	42/92 μW

[a]Excluding FPGA and IF clock generation.

shows the wireless testing setup. With TX-RX distances of 25–350 cm and for 1–10-kbps data rates, the measured BER always remains <0.1% [Fig. 17(b)]. The other wireless testing of the TRX is established by transferring pre-recorded electrocorticogram (ECoG) and electromyogram (EMG) signals at a 1-m distance. The transmitted and received time-domain plots of ECoG and EMG signals with BER below 0.01% and 5×10^{-6}% are shown in Fig. 17(c) and (d), respectively.

D. Multi-User Coexistence and Interference Testing

It is commonly known that the path loss and wireless signal energy absorption of human tissue increase with frequency. For example, human tissue (composed of 2-cm skin and fat) causes ∼63-dB attenuation for 2.4-GHz frequency band of standards such as wireless body area network (WBAN), Bluetooth, and IEEE802.11b/g [32]. In addition, accounting for 26-dB free-space path loss over 20-cm distance and less than −30-dB antenna gain, the received signal falls below RX sensitivity. Another major issue that BMI systems encounter is the interference between multiple MedRadio band users operating in the vicinity of one another. Fig. 18 shows the measured interference power over a wide frequency range that causes a BER higher than 0.1%. Compared to other architectures with high-Q internal/external passive components, this inductorless design exhibits a lower interference tolerance. To address this issue, we notice that MedRadio has limited the transmission time of TXs to 0.1% during a specific period. This notion was utilized to implement a listen-before-talk (LBT) protocol with the TRX operating in the burst-mode data transfer [*cf.* Fig. 19(a)]. This protocol advances through 10 time-slots in search of an available slot in the presence of an interferer, TRX3, for exclusive pairing of TRX1 and TRX2. A typical coexistence scenario is demonstrated in Fig. 19(b), where the TRX3-TRX2 distance is shorter than the TRX1-TRX2 distance by 0.5 m. This protocol improves BER from 4.53% (continuous mode) down to 0.03% (LBT). Although not implemented here, a frequency-domain LBT protocol can also be adopted as envisioned in the MedRadio standard. This is possible due to the wideband operation and large tuning range of this TRX. For the BMI application targeted in this design, wireless communication is primarily intended for transferring a limited number of commands, thus the BER degradation due to the interferers can be further reduced in the back-end processor by introducing redundancy in the command data package.

E. In Vitro Phantom Measurements

Fig. 20(a) and (b) shows the *in vitro* wireless connection setup and cross section of the phantom material, respectively.

TABLE III
TRANSMITTER PERFORMANCE COMPARISON

Reference	ISSCC 2014 [17]	TMTT 2014 [18]	JSSC 2009 [20]	This Work
Process (nm)	40	180	180	180
Carrier Freq. (MHz)	402∼405 420∼450	403	403	413∼419
Supply (V)	1	1.2	1.8	1.8
Architecture	Polar/Direct Mod.	Direct Mod.	Direct Mod.	Direct Mod.
Modulation	GMSK / DBPSK	OOK / OQPSK	FSK	OOK
Inductor Type	Off-Chip	Off-Chip	On-Chip	None
Output Power (dBm)	–10/–17	–20.9/–17	–20∼0	–4∼4.5
Data Rate (kbps)	11/4500	100/1000	50	1/10
Efficiency	NA	NA	33%[a] @-5 dBm	14%(OOK) 7%(CW)
Power (mW)	2.27/2.28	3.32	4.9	2.8[b] 5.6[c]

[a]PA only. [b]With -4 dBm output power in OOK mode. [c]With -4 dBm output power in CW mode.

The dimensions of titanium enclosure and plastic cap are shown in Fig. 20(c). A phantom composed of three layers, emulating the conductivity, permittivity, and thickness of human skin, fat, and muscle in the chest area [33], [34], is used to emulate the signal attenuation through human tissue. The measured conductivity of skin, fat, and muscle layers is 0.77, 0.034, and 0.8 S/m, respectively. The measured permittivity of each corresponding layer is 49.1, 5.54, and 57.4, as indicated in Fig. 20(f) and (g). Wireless connectivity was evaluated by positioning TX and RX at various horizontal and vertical distances. The BER remains <0.1% for a maximum vertical distance of 1.8 m. Similarly, the BER remains <0.1% for a maximum horizontal distance of 0.8 m, while the position of TRX2 is fixed [as shown in Fig. 20(d) and (e)].

Tables II and III show the comparison of the performance of the proposed TRX with the prior art. The non-coherent EDSM RX achieves −79/–74-dBm sensitivity and dissipates 42/92 μW at 1/10 kbps, respectively. The TX reaches 14% global efficiency at −4-dBm output power with 9.5-dB tuning range.

VII. CONCLUSION

A low-power MedRadio OOK TRX in 180-nm CMOS was presented. An EDSM technique was introduced to dramatically lower the RX power consumption. Analysis has been done to qualitatively explain the EDSM operation, and to evaluate the noise of the RX and ED properties on the overall performance. A power-cycled TX including a free running oscillator with AFC is demonstrated. The wireless data transfer, interference, multi-user coexistence testing, and *in vitro* phantom measurements also revealed that the TRX can serve as a basis of highly integrated and robust wireless chip, providing a solution for low-power TRX design for an implantable BMI system.

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